

.REM 8

IDENTIFICATION

PRODUCT CODE: AC-T006B-MC
PRODUCT NAME: CVDCB0 MDE/T-11 TARGET EMUL DIAG
PRODUCT DATE: APRIL 1982
MAINTAINER: DIAGNOSTIC ENGINEERING

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REVISION HISTORY

REVISION -----	DATE ----	REASONS -----
A	SEPTEMBER 1981	FIRST RELEASE
B	APRIL 1982	FIXED PROBLEM THAT ALLOWED BOTH THE SIGNAL COLB L AND DBLB L TO BE ENABLED AT THE SAME TIME.

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1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THE CDS-11 TARGET EMULATOR DIAGNOSTIC WILL TEST ALL THE LOGIC ON THE TARGET EMULATOR MODULE AND THE 'POD' THAT IS TESTABLE WITHOUT THE ADDITION OF OTHER CDS MODULES. ALL DATA PATHS AND REGISTERS WITHIN THE TARGET EMULATOR MODULE ARE TESTED. HOWEVER, THE OUTPUT AND INPUT SIGNALS TO AND FROM THE TARGET SYSTEM ARE NOT TESTED. LIMITED TESTING OF THE SYSTEM BUS IS PERFORMED. THE PROGRAM ALSO CHECKS THAT THE TARGET EMULATOR MODULE CAN GENERATE INTERRUPTS TO THE LSI-11. THE T-11 CHIP WILL BE ENABLED IN THE LAST PART OF THIS DIAGNOSTIC, HOWEVER, ONLY LIMITED TESTING OF THE T-11 WILL BE PERFORMED.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT. THIS PROGRAM CAN BE USED WITH XXDP+, ACT, APT, SLIDE AND PAPER TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM HAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER, THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE AND DISCONNECT FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS PROGRAM.

1.2 SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. CDS-11 BACKPLANE AND CABLES
5. TARGET EMULATOR MODULE(S) (M8742)
6. T-11 POD(S)
7. MXV11 MODULE AND CDS-11 ROMS
8. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
9. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3 RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE "?" IN CHQUS INDICATES THE REVISION LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE REVISION LEVEL WAS 'E').

1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

1.5 ASSUMPTIONS

2.0 OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES.
FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1 COMMANDS

THERE ARE ELEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES (SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

COMMAND	EFFECT
START	START THE DIAGNOSTIC FROM AN INITIAL STATE
RESTART	START THE DIAGNOSTIC WITHOUT INITIALIZING
CONTINUE	CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
PROCEED	CONTINUE FROM AN ERROR HALT
EXIT	RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY!)
ADD	ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE CONSIDERED TO BE ACTIVE AT START TIME)
DROP	DEACTIVATE A UNIT
PRINT	PRINT STATISTICAL INFORMATION (IF IMPLEMENTED BY THE DIAGNOSTIC - SECTION 4.0)
DISPLAY	TYPE A LIST OF ALL DEVICE INFORMATION
FLAGS	TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
ZFLAGS	CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO YOU MAY, FOR EXAMPLE, TYPE "STA" INSTEAD OF "START".

2.2 SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION. THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH. IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY 'DDDD'.

SWITCH	EFFECT
/TESTS:LIST	EXECUTE ONLY THOSE TESTS SPECIFIED IN THE LIST. LIST IS A STRING OF TEST NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10. THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
/PASS:DDDD	EXECUTE DDDD PASSES (DDDD = 1 TO 64000)
/FLAGS:FLGS	SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED IN SECTION 2.3.
/EOP:DDDD	REPORT END OF PASS MESSAGE AFTER EVERY DDDD PASSES ONLY. (DDDD = 1 TO 64000)
/UNITS:LIST	TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED IN THE LIST. LIST EXAMPLE - /UNITS:0:5:10-12 USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)

EXAMPLE OF SWITCH USAGE:

START/TESTS:1-5/PASS:1000/EOP:100

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY, FOR EXAMPLE, TYPE '/TES:1-5' INSTEAD OF '/TESTS:1-5'.

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH COMMAND.

	TESTS	PASS	FLAGS	EOP	UNITS
START	X	X	X	X	X
RESTART	X	X	X	X	X
CONTINUE		X	X	X	
PROCEED			X		
DROP					X
ADD					X
PRINT					
DISPLAY					X
FLAGS					
ZFLAGS					
EXIT					

2.3 FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS, NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

FLAG	EFFECT
HOE	HALT ON ERROR - CONTROL IS RETURNED TO RUNTIME SERVICES COMMAND MODE
LOE	LOOP ON ERROR
IER*	INHIBIT ALL ERROR REPORTS
IBE*	INHIBIT ALL ERROR REPORTS EXCEPT FIRST LEVEL (FIRST LEVEL CONTAINS ERROR TYPE, NUMBER, PC, TEST AND UNIT)
IXE*	INHIBIT EXTENDED ERROR REPORTS (THOSE CALLED BY PRINTX MACRO'S)
PRI	DIRECT MESSAGES TO LINE PRINTER
PNT	PRINT TEST NUMBER AS TEST EXECUTES
BOE	'BELL' ON ERROR
UAM	UNATTENDED MODE (NO MANUAL INTERVENTION)
ISR	INHIBIT STATISTICAL REPORTS (DOES NOT APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT STATISTICAL REPORTING)
IDR	INHIBIT PROGRAM DROPPING OF UNITS
ADR	EXECUTE AUTODROP CODE
LOT	LOOP ON TEST

EVL EXECUTE EVALUATION (ON DIAGNOSTICS WHICH
HAVE EVALUATION SUPPORT)

*ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE, TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS AND TYPE A 'BELL' ON ERROR, YOU MAY USE THE FOLLOWING STRING:

/FLAGS:LOE:IER:BOE

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?" YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING QUESTIONS FOR EACH UNIT.

CSR ADDRESS:
VECTOR ADDRESS:
DEVICE NUMBER:

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE PARAMETERS. THESE PARAMETERS WILL GOVERN SOME DIAGNOSTIC SPECIFIC OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?" IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING "Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT.

THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 0<CR>
Q-FACTOR (O) 0 ? 1<CR>

UNIT 2
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 1<CR>
Q-FACTOR (O) 1 ? 0<CR>

UNIT 3
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 2<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 4
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 3<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 5
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 4<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 6
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 5<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 7
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 6<CR>
Q-FACTOR (O) 0 ? 1<CR>

UNIT 8
CSR ADDRESS (O) 160000<CR>
SUB-DEVICE # (O) ? 7<CR>
Q-FACTOR (O) 1 ? <CR>

NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING MULTIPLE UNITS!

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER.

LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION FEATURE.

```
# UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 0,1<CR>
Q-FACTOR (O) 0 ? 1,0<CR>

UNIT 3
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 2-5<CR>
Q-FACTOR (O) 0 ? 0<CR>

UNIT 7
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 6,7<CR>
Q-FACTOR (O) 0 ? 1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE "-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES 2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS SHOWN BELOW.

```
# UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 0-7<CR>
Q-FACTOR (O) 0 ? 0,1,0,....,1,1<CR>
```

AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE AND DISCONNECTED FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS DIAGNOSTIC.

TO START-UP THIS PROGRAM:

1. BOOT XXDP+
2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.
3. TYPE 'R NAME', WHERE NAME IS THE NAME OF THE BIN OR BIC FILE FOR THIS PROGRAM
4. TYPE 'START'
5. ANSWER THE 'CHANGE HW' QUESTION WITH 'Y'
6. ANSWER ALL THE HARDWARE QUESTIONS
7. ANSWER THE 'CHANGE SW' QUESTION WITH 'N'

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES ARE ALWAYS PRINTED UNLESS THE 'IER' FLAG IS SET (SECTION 2.3). THE GENERAL ERROR MESSAGE IS OF THE FORM:

NAME TYPE NUMBER ON UNIT NUMBER TST NUMBER PC:XXXXXX
ERROR MESSAGE

WHERE: NAME = DIAGNOSTIC NAME
TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
NUMBER = ERROR NUMBER
UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS THE 'IER' OR 'IBE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS PRINTED UNLESS THE 'IER', 'IBE' OR 'IXE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

WHEN AN ERROR IS REPORTED ON THE CONSOLE TERMINAL, THE USER SHOULD REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED AT THE TIME THE ERROR WAS DETECTED. THE 'PC' REPORTED IN THE ERROR MESSAGE INDICATES THE ADDRESS OF THE ERROR CALL. EACH STEP OF A TEST

IS DESCRIBED IN DETAIL TO HELP THE USER UNDERSTAND THE TEST SEQUENCE. ONCE UNDERSTANDING THE TEST SEQUENCE, THE USER SHOULD BE ABLE TO DETERMINE THE FAULT OR FAULTS WHICH COULD CAUSE THE ERROR.

THE ERROR PRINTOUTS WILL USE THE FOLLOWING WORDS TO INDICATE ERROR INFORMATION. A DESCRIPTION OF THE WORDS PRINTED OUT ARE AS FOLLOWS:

REG: ONE OF THE TARGET EMULATOR MODULE'S CONTROL REGISTERS
LOAD: DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR
EXPECTED DATA TO BE IN CONTROL REGISTER ON A READ
READ: DATA THAT WAS READ FROM THE CONTROL REGISTER
GOOD: EXPECTED CONTROL REGISTER DATA
BAD: DATA 'READ' FROM THE CONTROL REGISTER
XXXXXX: SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

THERE ARE FIVE ERROR NUMBERS ASSOCIATED WITH THIS DIAGNOSTIC. THE ERROR NUMBERS AND THEIR MEANINGS ARE DESCRIBED BELOW:

ERROR NUMBER 1 - ERROR DETECTED CHECKING CONTROL REGISTER 0
ERROR NUMBER 2 - ERROR DETECTED CHECKING CONTROL REGISTER 2
ERROR NUMBER 3 - ERROR DETECTED CHECKING CONTROL REGISTER 4
ERROR NUMBER 4 - ERROR DETECTED CHECKING CONTROL REGISTER 6
ERROR NUMBER 5 - ERROR DETECTED TRYING TO RUN THE T-11 CHIP

EXAMPLES OF EACH TYPE OF CONTROL REGISTER ERROR PRINTOUT ARE SHOWN BELOW:

** CONTROL REGISTER 0 ERROR MESSAGES **

CVDC DVC FTL ERR 00001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
GDAL 15:0 REG ERROR
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX

THE ABOVE ERROR MESSAGE WILL BE PRINTED OUT FOR ALL CONTROL REGISTER 0 ERRORS EXCEPT THOSE ERRORS DETECTED WHILE TESTING THE TARGET EMULATOR INTERRUPT LOGIC. IF AN ERROR WAS DETECTED WHILE CHECKING THE TARGET EMULATOR INTERRUPT LOGIC, THE ABOVE ERROR MESSAGE WILL BE REPORTED, HOWEVER, THE MESSAGE "GDAL 15:0 REG ERROR" WILL BE REPLACED WITH EITHER "UNEXPECTED INTERRUPT OCCURED" OR "FAILED TO INTERRUPT". THE INFORMATION PRINTED OUT FOR CONTROL REGISTER 0 MAY HELP THE USER IN DETERMINING THE ERROR, HOWEVER, THE GOOD AND BAD DATA MAY BE THE SAME, THEREFORE REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED AT THE TIME THE ERROR OCCURED.

TIME OUT ERROR ADDRESSING CONTROL REG 0

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

** CONTROL REGISTER 2 ERROR MESSAGE **

CVDC DVC FTL ERR 00002 ON UNIT 00 TST 004 SUB 000 PC: XXXXXX
ADAL 15:0 REG ERROR
CONTROL REG 2 ERROR
REG2 = LOAD: XXXXXX READ: XXXXXX

THE ABOVE ERROR MESSAGE WILL BE PRINTED FOR ALL CONTROL REGISTER 2 ERRORS EXCEPT A TIME OUT ERROR.

TIME OUT ERROR ADDRESSING CONTROL REG 2

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 2 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

** CONTROL REGISTER 4 ERROR MESSAGE **

CVDC DVC FTL ERR 00003 ON UNIT 00 TST 006 SUB 000 PC: XXXXXX
VDAL 7:0 OR PAUSE STATE MACHINE ERROR
CONTROL REG 4 ERROR
REG4 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX

THE ABOVE ERROR MESSAGE WILL BE REPORTED FOR ALL CONTROL REGISTER 4 ERRORS EXCEPT A TIME OUT ERROR.

TIME OUT ERROR ADDRESSING CONTROL REG 4

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 4 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

** CONTROL REGISTER 6 ERROR MESSAGE **

THERE ARE THREE TYPES OF ERROR MESSAGES THAT ARE REPORTED FOR CONTROL REGISTER 6 ERRORS WHICH ARE SHOWN BELOW.

CVDC DVC FTL ERR 00004 ON UNIT 00 TST 008 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

CVDC DVC FTL ERR 00004 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

CVDC DVC FTL ERR 00005 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

IN THE ABOVE ERRORS, REFER TO THE LINE INDICATING 'REG6 =' FOR CONTROL REGISTER 6 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMATION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THOSE REGISTERS PREVIOUS TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP.

IF THE NUMBER REPORTED FOR 'DVC FTL ERR' WAS 00005, THEN THE ERROR OCCURED AS A RESULT OF THE PROGRAM TRYING TO TEST THE T-11 CHIP.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORTS WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

HDAL 15:0 REG ERROR
MR 15:0 REG ERROR
FDAL 7:0 REG ERROR
EOAI 7:0 OR FDAL 7:0 REG ERROR
DIAG ADDR 15:0 REG ERROR
FORCE JUMP ADDRESS READBACK REG ERROR
INSTR REG TO EODAL BUS READBACK ERROR
MODE REG TO EODAL BUS READBACK ERROR
FORCE JUMP ADDRESS REG TO EODAL BUS READBACK ERROR
CTL 7:0 OR FDAL 7:0 REG ERROR
MODE REG TO EIDAL BUS READBACK ERROR
MODE REG TO TARGET MODE REG ERROR
MODE REG TO ADDRESS BUS READBACK ERROR
OLD FJA TO EIDAL BUS ERROR
OLD FJA TO ADDRESS BUS ERROR
OLD FJA TO TDAL LATCH EIDAL BUS ERROR
TDAL LATCH TO EIDAL TO DATA TO EODAL BUS ERROR
FDAL REG TO EODAL BUS ERROR
FDAL REG TO EODAL BUS TO EIDAL BUS ERROR
PAUSE STATE NOT ENTERED WHEN T-11 IS POWERED UP
FORCE JUMP ADDRESS NOT = EXPECTED T-11 START-RESTART ADDRESS

TIME OUT ERROR ADDRESSING CONTROL REG 6

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED. THE 'EOP' SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLES

CONTROL REGISTER 0 (163010) - GDAL REGISTER

15 GDAL15 BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. TARGET EMULATOR DEVICE TYPE EQU.'S 0 (0000)

BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8.

14 GDAL14 ALWAYS A 0 ON READ
13 GDAL13 ALWAYS A 0 ON READ

12 GDAL12 ALWAYS A 0 ON READ

BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF THE TARGET EMULATOR. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

11 GDAL11 DEVICE NUMBER/TYPE
10 GDAL10 DEVICE NUMBER/TYPE
9 GDAL9 DEVICE NUMBER/TYPE
8 GDAL8 DEVICE NUMBER/TYPE
7 GDAL7 SINGLE STEP BREAK INDICATOR (READ ONLY)
6 GDAL6 TIMEOUT BREAK INDICATOR (READ ONLY)
5 GDAL5 MEMORY SIMULATOR BREAK INDICATOR (READ ONLY)
4 GDAL4 STATE ANALYZER BREAK INDICATOR (READ ONLY)
3 GDAL3 TARGET EMULATOR INTERRUPT ENABLE (R/W)
2 GDAL2 POINTER FOR EXTENDED REGISTER SELECT (R/W)
1 GDAL1 POINTER FOR EXTENDED REGISTER SELECT (R/W)
0 GDALO POINTER FOR EXTENDED REGISTER SELECT (R/W)

EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0

GDAL2	GDAL1	GDALO	REGISTER SELECTED VIA R/W TO CONTROL REGISTER 6
0	0	0	WRITE DIAGNOSTIC ADDRESS REGISTER READBACK OF ADDRESS BUS
0	0	1	WRITE NEW FORCE JUMP ADDRESS REGISTER READBACK OF FORCE JUMP ADDRESS READBACK REG
0	1	0	WRITE FDAL AND EOAI REGISTER READBACK OF FDAL/EOAI OR FDAL/CTL REG
0	1	1	R/W HDAL REGISTER
1	0	0	R/W MODE REGISTER
1	0	1	READBACK OF TARGET MODE REGISTER
1	1	0	READBACK OF EIDAL BUS
1	1	1	READBACK OF EODAL BUS

CONTROL REGISTER 2 (163012) - ADAL REGISTER

15 ADAL15 SELECT COLUMN AI FOR STATE ANALYZER (1)
14 ADAL14 SELECT ROW/COLUMN AI FOR STATE ANALYZER (1)
13 ADAL13 SELECT SERVICE AI FOR STATE ANALYZER (0)
13 ADAL13 ENABLE SERVICE FROM TARGET EMULATOR (1)
13 ADAL13 ENABLE SERVICE FROM THE TARGET (0)
12 ADAL12 ENABLE MODE FROM TARGET EMULATOR (1)
12 ADAL12 ENABLE MODE FROM THE TARGET (0)
11 ADAL11 DISABLE SERVICE TO THE TARGET (1)
11 ADAL11 ENABLE SERVICE TO THE TARGET (0)
10 ADAL10 MASTER SWITCH
9 ADAL9 ENABLE STATE ANALYZER CLOCKS (1)
8 ADAL8 ENABLE TIMEOUT BREAK (1)
8 ADAL8 DISABLE TIMEOUT BREAK (0)
7 ADAL7 ENABLE REFRESH TO STATE ANALYZER (1)
7 ADAL7 DISBALE REFRESH TO STATE ANALYZER (0)
6 ADAL6 SPARE
5 ADAL5 ENABLE SINGLE STEP BREAK (1)
5 ADAL5 DISABLE SINGLE STEP BREAK (0)

- 4 ADAL4 ENABLE PAUSE STATE TO RUN MODE (1)
ENABLE PAUSE STATE TO PAUSE MODE (0)
- 3 ADAL3 POWER UP FROM TARGET (1)
- 2 ADAL2 POWER UP FROM TARGET EMULATOR
- 1 ADAL1 SELECT TARGET EMULATOR CRYSTAL CLOCK (1)
SELECT CLOCK FROM THE STATE ANALYZER (0)
- 0 ADAL0 RESET BREAK LOGIC - ZEROES BREAK LATCH FLIP-FLOP, SINGLE
STEP BREAK FLIP-FLOP AND MEMORY SIMULATOR BREAK LATCH
FLIP-FLOP

CONTROL REGISTER 4 (163014) - VDAL REGISTER

- 15 VDAL15 TNFJ H - TAKE NEW FORCE JUMP ADDRESS F/F (READ)
- 14 VDAL14 EP8N H - 8 BIT ADDRESS HB F/F (READ)
- 13 VDAL13 EP8G H - 8 BIT ADDRESS LB F/F (READ)
- 12 VDAL12 EP8F H - 8 BIT INSTRUCTION HB F/F (READ)
- 11 VDAL11 EPFN H - 16 BIT ADDRESS F/F (READ)
- 10 VDAL10 EPSF H - PAUSE STATE SYNC F/F (READ)
- 9 VDAL9 PSMW H - PAUSE STATE WORKING F/F (READ)
- 8 VDAL8 OUTNEW H - GET NEW ADDRESS F/F (READ)
- 7 VDAL7 DIAGNOSTIC FETCT H (READ/WRITE)
- 6 VDAL6 MSDI H - DATA IN LOGIC LEVEL (READ)
- 5 VDAL5 BTS1 H -
- 4 VDAL4 EDEOC H - LOGIC LEVEL OF STATE ANALYZER CLOCK (READ)
- 3 VDAL3 READ H - LOGIC LEVEL OF REAT H (READ)
- 2 VDAL2 DIAGNOSTIC RESET OF THE TARGET EMULATOR MODULE AND
CLOCKS THE TAI AND TDAL LATCHES (READ/WRITE)
- 1 VDAL1 SPARE (READ/WRITE)
- 0 VDAL0 ENABLE TAI AND TDAL READBACK FROM POD (READ/WRITE)

CONTROL REGISTER 6 (163016) - FDAL REIGSTER (EOAI/CTL ON FDAL 15:8)

- 7 FDAL7 INTERRUPT VECTOR
- 6 FDAL6 INTERRUPT VECTOR
- 5 FDAL5 INTERRUPT VECTOR
- 4 FDAL4 INTERRUPT VECTOR
- 3 FDAL3 INTERRUPT VECTOR
- 2 FDAL2 INTERRUPT VECTOR
- 1 FDAL1 SPARE
- 0 FDAL0 SELECT EOAI REG TO BE READBACK ON FDAL BITS 15:8 (1)
SELECT CTL REG TO BE READBACK ON FDAL BITS 15:8 (0)

CONTROL REGISTER 6 (163016) - HDAL REGISTER - DIAGNOSTIC CONTROL BITS

- 15 HDAL15 DIAGNOSTIC CONTROL OF PPI L WHEN HDAL2 EQUALS A ONE
- 14 HDAL14 DIAGNOSTIC CONTROL OF EIDAL17 H WHEN HDAL2 EQUALS A ONE
- 13 HDAL13 DIAGNOSTIC CONTROL OF PCAS H WHEN HDAL2 EQUALS A ONE
- 12 HDAL12 DIAGNOSTIC CONTROL OF PRAS H WHEN HDAL2 EQUALS A ONE
- 11 HDAL11 DIAGNOSTIC CONTROL OF EIDAL16 H WHEN HDAL2 EQUALS A ONE
- 10 HDAL10 SPARE
- 9 HDAL9 ENABLE DIAGNOSTIC ADDRESS REGISTER TO ADDRESS BUS
- 8 HDAL8 DIAGNOSTIC CONTROL OF CREADY L WHEN HDAL2 EQUALS A ONE
- 7 HDAL7 DIAGNOSTIC CONTROL OF PBCLR H WHEN HDAL2 EQUALS A ONE
- 6 HDAL6 DIAGNOSTIC CONTROL OF PSEL1 L WHEN HDAL2 EQUALS A ONE
- 5 HDAL5 DIAGNOSTIC CONTROL OF PSELO L WHEN HDAL2 EQUALS A ONE
- 4 HDAL4 DIAGNOSTIC CONTROL OF PR/WHB L WHEN HDAL2 EQUALS A ONE

3 HDAL3 DIAGNOSTIC CONTROL OF PR/WLB L WHEN HDAL2 EQUALS A ONE
2 HDAL2 ENABLES PROGRAM TO GENERATE T-11 SIGNALS LISTED IN HDAL (1)
ENABLES T-11 TO GENERATE T-11 SIGNALS LISTED IN HDAL (0)
1 HDAL1 SPARE
0 HDALO DIAGNOSTIC CONTROL OF MSDI H WHEN HDAL2 EQUALS A ONE

CONTROL REGISTER 6 (163016) - MODE REGISTER

15 MR15 T-11 START/RESTART ADDRESS SELECT
14 MR14 T-11 START/RESTART ADDRESS SELECT
13 MR13 T-11 START/RESTART ADDRESS SELECT
12 MR12 T-11 USER MODE (1)
T-11 TESTER MODE (0)
11 MR11 SELECT 8 BIT BUS (1)
SELECT 16 BIT BUS (0)
10 MR10 T-11 DYNAMIC MODE ONLY - SELECTS 4K/16K (1)
T-11 DYNAMIC MODE ONLY - SELECTS 64K (0)
9 MR9 T-11 STATIC MEMORY SELECT (1)
T-11 DYNAMIC MEMORY SELECT (0)
8 MR8 T-11 DELAYED READ/WRITE SELECT (1)
T-11 NROMAL READ/WRITE SLLLECT (0)
7 MR7 NOT DEFINED
6 MR6 NOT DEFINED
5 MR5 NOT DEFINED
4 MR4 NOT DEFINED
3 MR3 NOT DEFINED
2 MR2 NOT DEFINED
1 MR1 T-11 STANDARD MICROCYCLE (1)
T-11 LONG MICROCYCLE (0)
0 MR0 T-11 PROCESSOR CLOCK (1)
T-11 CONSTANT CLOCK (0)

6.0 TEST SUMMARIES

TEST 1:

THIS TEST WILL CHECK THAT THE TARGET EMULATOR MODULE CAN BE SELECTED AND INITIALIZED TO A KNOWN STATE. THE TEST DESCRIBED BELOW WILL BE EXECUTED AT THE BEGINNING OF EACH TEST TO PUT THE TARGET EMULATOR MODULE IN A KNOWN STATE.

THE TEST WILL LOAD AND CHECK THAT THE DEVICE NUMBER CAN BE LOADED INTO AND READ FROM CONTROL REGISTER 0. ALL THE READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. THE TEST WILL CHECK THAT THE TARGET EMULATOR DEVICE TYPE CAN BE READ BY SETTING CONTROL REGISTER 0 BIT 15 TO A ONE AND THEN READING CONTROL REGISTER 0. THE TEST WILL SET CONTROL REGISTER BIT 15 TO A ZERO AND BITS 1 AND 0 TO ONES. BIT15 ON A ZERO WILL ENABLE THE DEVICE NUMBER TO BE READ AGAIN. BITS 1 AND 0 SET TO ONES WILL CAUSE THE HDAL REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. THE TEST WILL NOW LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL2 SET TO A ONE AND ALL OTHER HDAL BITS CLEARED. HDAL2 SET TO A ONE WILL ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS USING HDAL REGISTER BITS. THE TEST WILL NOW SET CONTROL REGISTER 0 BITS 1 AND 0 TO ZEROES AND SET BIT 2 TO A ONE. CONTROL REGISTER 0 BIT 2 ON A ONE WILL CAUSE THE MODE REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. THE TEST WILL LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL CAUSE 16 BIT ADDRESS MODE TO BE SELECTED. THE TEST WILL SET ADAL REGISTER BIT 0 TO A ONE AND THEN ZERO. ALL

OTHER ADAL REGISTER BITS WILL BE LOADED AND CHECKED FOR ZEROES. ADALO BEING SET TO A ONE WILL CLEAR THE BREAK LATCH FLIP-FLOP, THE SINGLE STEP BREAK FLIP-FLOP, AND THE MEMORY SIMULATOR BREAK FLIP-FLOP. ADAL REGISTER BIT 2 ON A ZERO WILL CAUSE THE T-11 TO BE TURNED OFF. THE TEST WILL THEN READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT ALL THE BREAK INDICATOR BITS ARE CLEARED. THE TEST WILL NOW SET VDAL REGISTER BIT 2 TO A ONE AND THEN A ZERO. ALL OTHER VDAL READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. VDAL REGISTER BIT 2 ON A ONE WILL CAUSE ALL THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE, EXCEPT THOSE INITIALIZED BY ADALO, TO BE SET TO A KNOWN STATE.

TEST 2:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS, GDAL 3:0, CAN BE SET TO ALL ONES (17), AND THEN SET TO ALL ZEROES. THE READ ONLY BITS, GDAL7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 3:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS GDAL 3:0, CAN BE LOADED WITH ONES AND ZEROES (12) AND THEN LOADED WITH ZEROES AND ONES (5). THE READ ONLY BITS GDAL 7:4 ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 4:

THIS TEST WILL CHECK CONTROL REGISTER 0 R/W BITS USING A BINARY COUNT PATTERN. THE PATTERN WILL START INITIALLY AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN EQUALS 17. THE READ ONLY BITS, GDAL 7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 5:

THIS TEST WILL CHECK THAT CONTROL REGISTER 2 BITS ADAL 15:0 CAN BE SET TO ALL ONES (177777) AND THEN ALL ZEROES (000000).

TEST 6:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:0 WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 7:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND INCREMENT TO 377 BY AN INCREMENT OF ONE.

TEST 8:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:8 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED.

TEST 9:

THIS TEST WILL CHECK THAT CONTROL REGISTER 4 READ/WRITE BITS VDAL7, VDAL2, VDAL1 AND VDALO CAN BE SET AND CLEARED. THE TEST WILL CHECK THESE BITS

USING A DECREMENTING BINARY COUNT PATTERN. THE READ ONLY BITS WILL BE CHECKED TO BE ZEROES DURING THIS TEST. READ ONLY BITS VDAL 15:8 SHOULD BE ZERO AS A RESULT OF VDAL2 H BEING SET TO A ONE DURING THIS TEST. READ ONLY BITS 6:3 SHOULD BE A ZERO AS A RESULT OF ADAL BIT 10 BEING A ZERO. THE ADAL REGISTER WAS CLEARED IN THE ABOVE ROUTINE "INITTE".

TEST 10:

THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE SET TO ALL ONES (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE DATA ON THE WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.

TEST 11:

THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE LOADED WITH AN ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525). TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.

TEST 12:

THIS TEST WILL CHECK THE LOW BYTE OF THE HDAL REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED ARE HDAL BITS 7:0. TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

TEST 13:

THIS TEST WILL CHECK THE HIGH BYTE OF THE HDAL REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED ARE HDAL BITS 15:8. TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

TEST 14:

THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE SET TO ALL ONES (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE MODE REGISTER, THE

TEST WILL SET GDAL2 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, PULSES WILL BE OCCUR ON THE SIGNALS WPT4 LB H AND WPT4 HB H. THESE PULSE WILL CAUSE THE DATA ON THE WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L. THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK

TEST 15:

THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE LOADED WITH AN ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525). TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 IN THE LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN REG 0, PULSES WILL OCCUR ON THE SIGNALS WPT4 LB H AND WPT4 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L. THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK.

TEST 16:

THIS TEST WILL CHECK THE LOW BYTE OF THE MODE REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED ARE MR BITS 7:0. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1 IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.

TEST 17:

THIS TEST WILL CHECK THE HIGH BYTE OF THE MODE REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED ARE MR BITS 15:8. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1 IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.

TEST 18:

THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE SET TO ALL ONES (377) AND THEN TO ALL ZEROES (000). TO SELECT THE FDAL REGISTER, THE TEST WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER, WILL BE IGNORED DURING THIS TEST.

TEST 19:

THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (125). TO SELECT THE FDAL REGISTER, THE TEST WILL SET THE SIGNAL

GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER, WILL BE IGNORED DURING THIS TEST.

TEST20:

THIS TEST WILL CHECK FDAL REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE FDAL REGISTER. TO SELECT THE FDAL REGISTER, THE TEST WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE FDAL REG VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE FDAL REG VIA THE SIGNAL RPT2 L.

TEST 21:

THIS TEST WILL CHECK EOAI REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL A PATTERN OF ALL ONES HAS BEEN LOADED INTO THE EOAI REGISTER AND CHECKED. THE EOAI REGISTER IS THE HIGH BYTE OF THE FDAL REGISTER. DATA IS LOADED INTO THE EOAI REGISTER VIA THE SIGNAL WPT2 HB H WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS SELECTED VIA GDAL BITS 2:0. TO READ THE EOAI BUS, THE PROGRAM WILL SET FDALO H TO A ONE TO SELECT THE EOAI BUS TO BE READ INSTEAD OF THE CTL BUS. THE EOAI BUS IS READ BACK TO THE LSI-11 VIA THE SIGNAL RAT2 L WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS SELECTED.

TEST 22:

THIS TEST WILL CHECK THAT THE DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN BE LOADED WITH ALL ONES (177777) AND THEN ALL ZEROES (000000).

TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 23:

THIS TEST WILL CHECK THAT THE DAIGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATERRN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL

SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 24:

THIS TEST WILL CHECK THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS ADDR 7:0. THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED WITH ZEROES DURING THIS TEST.

TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 25:

THIS TEST WILL CHECK THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:8. THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED WITH ZEROES DURING THIS TEST.

TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 26:

THIS TEST WILL CHECK THAT THE MODE REGISTER CAN BE READBACK ON THE EODAL BUS. THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING PATTERNS: 125252,052525,

177400, 000377, 177777, AND 000000. FOR EACH PATTERN LOADED THE TEST WILL ENABLE THE MODE REGISTER ONTO THE EODAL BUS AND READ AND CHECK THE EODAL BUS FOR THE CORRECT MODE REGISTER PATTERN. THE MODE REGISTER WILL BE ENABLED TO THE EODAL BUS WHEN ADAL12 H IS SET TO A ONE AND THE SIGNAL XBCLR H IS ASSERTED HIGH.

TEST 27:

THIS TEST WILL CHECK THE FORCE JUMP ADDRESS READBAC REGISTER WITH THE FOLLOWING DATA PATTERNS 125252, 052525, 177400, 000377, 177777, AND 000000. THE DIAGNOSTIC ADDRESS REGISTER WILL PROVIDE THE DATA ON THE ADDRESS BUS TO THE FORCE JUMP ADDRESS REGISTER AND FORCE JUMP ADDRESS READBAC REGISTER.

TEST 28:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP-FLOPS, PAUSE STATE WORKING, AND PAUSE STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADALO H WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK AND ADALO H ON A ONE WILL CLEAR THE BREAK LOGIC, THUS SETTING THE SIGNAL BRK H TO A ZERO.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, AND 000000. THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED ON THE ADDRESS BUS DURING THIS TEST.

TEST 29:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADALO H WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK AND ADALO H ON A ONE WILL CLEAR THE BREAK LOGIC, THUS SETTING THE SIGNAL BRK H TO A ZERO.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, AND 000000. THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED AT THE BEGINNING OF THE TEST.

TEST 30:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 'RUN' AND 16 BIT ADDRESS MODE. WHEN THE PAUSE STATE MACHINE IS SETUP IN 'RUN' MODE VIA ADAL4 H ON A ONE AND A PULSE ON THE SIGNAL XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDITON IS RECEIVED ON THE SIGNAL 'BRK H'. THIS TEST WILL USE THE

TIMEOUT BREAK ONE SHOT TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN NO BREAK CONDITION IS RECEIVED AND THAT IT IS ENTERED WHEN A BREAK CONDITION IS RECEIVED. THE TEST WILL CHECK ALL THE PAUSE STATE LOGIC ASSOCIATED WITH THE SIGNAL 'BRK H'. THE TEST WILL CHECK THAT THE SIGNAL 'TOBRK H' IS SET IN CONTROL REGISTER 0 WHEN THE TIME OUT BREAK ONE SHOT IS NOT BEING FIRED AND THAT IT IS NOT SET WHEN THE TIME OUT BREAK ONE SHOT IS BEING FIRED.

TEST 31:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 'RUN' AND 16 BIT ADDRESS MODE. WHEN THE PAUSE STATE MACHINE IS SETUP IN 'RUN' MODE VIA ADAL4 H ON A ONE AND A PULSE ON XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDITION IS RECEIVED ON THE SIGNAL 'BRK H'. THIS TEST WILL USE THE SINGLE STEP BREAK FLIP-FLOP TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN THE SINGLE STEP BREAK FLIP-FLOP IS CLEARED AND THAT IT CAN BE ENTERED WHEN THE SINGLE STEP BREAK FLIP-FLOP IS SET TO A ONE. THE TEST WILL CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP ONCE SET, WILL REMAIN LATCHED TO THE SET STATE UNTIL CLEARED BY A PULSE BEING ISSUED ON THE SIGNAL 'BRKRES L'. THE TEST WILL SET THE PAUSE STATE MACHINE FLIP-FLOP'S: PAUSE STATE WORKING, PAUSE STATE SYNC AND 16 BIT ADDRESS VIA THE SIGNALS XRAS H AND XCAS H. ONCE ALL THESE FLIP-FLOPS ARE SET TO THE ONE STATE, THE TEST WILL CHECK THAT THEY CAN BE CLEARED BY ISSUING A PULSE ON THE SIGNAL 'INVD L'.

TEST 32:

THIS TEST WILL CHECK THAT THE EDFET FLIP-FLOP CAN BE CLEARED WHEN A PULSE IS ISSUED OF THE SIGNAL XPI L. THE TEST WILL SET ADAL4 H TO A ZERO TO CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN A PULSE IS ISSUED ON THE SIGNAL XRAS H. THE TEST WILL SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE. THE TEST WILL THEN PULSE XRAS H TO SET THE EDFET FLIP-FLOP TO A ONE AND TO SET THE PAUSE MODE FLIP-FLOP TO THE PAUSE MODE. WHEN EDFET FLIP-FLOP IS SET TO A ONE AND THE PAUSE MODE FLIP-FLOP IS SET TO THE PAUSE MODE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE TEST WILL NOW PULSE THE SIGNAL XPI L TO CLEAR THE EDFET FLIP-FLOP. WHEN THE EDFET FLIP-FLOP IS CLEARED, THE SIGNAL PB H WILL BE ASSERTED LOW. THE SIGNAL PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE WORKING FLIP-FLOP. THE TEST WILL NOW PULSE THE SIGNAL XCAS H. WHEN A PULSE IS ISSUED ON THE SIGNAL XCAS H AND THE SIGNAL PB H IS ASSERTED LOW, THE PAUSE STATE SYNC FLIP-FLOP WILL BE CLOCKED TO A ZERO. THE SIGNAL XCAS H WILL ALSO CLOCK THE PAUSE STATE WORKING FLIP-FLOP TO A ONE.

TEST 33:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE PAUSE STATE WORKING FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADALO H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS MODE. THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000. THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED TO THE ADDRESS BUS DURING THIS TEST.

TEST 34:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADALO H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS MODE. THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000. THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED WITH THE DATA AT THE BEGINNING OF THE TEST.

TEST 35:

THIS TEST WILL CHECK THAT THE PAUSE STATE MACHINE FLIP - FLOPS, PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB, AND 8 BIT ADDRESS HB, CAN BE CLEARED WHEN THE SIGNAL VDAL2 H IS ASSERTED HIGH. ALL THE ABOVE FLIP-FLOPS ARE SET TO A ONE BY SETTING THE SIGNAL FETCT H TO A ONE, SETTING THE SIGNAL ADAL4 H TO A ZERO, AND PULSING THE SIGNALS XRAS H AND XCAS H. ONCE ALL THE FLIP-FLOPS ARE SET TO ONES, THE TEST WILL SET THE SIGNAL VDAL2 H AND CHECK THAT ALL THE PAUSE STATE MACHINE FLIP-FLOPS CLEARED.

TEST 36:

THIS TEST WILL CHECK THAT THE EOAI REGISTER BITS 7:0 CAN BE LOADED AND READ BACK CORRECTLY. THE TEST WILL ALSO CHECK THE DATA PATH TO BE CONNECTED AND FUNCTIONING PROPERLY FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE TEST WILL CHECK THE DATA PATH FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE TAI BUS, TO THE TAI DIAGNOSTIC LATCH, AND BACK FROM THE TAI DIAGNOSTIC LATCH TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE DATA PATTERN USED DURING THIS TEST WILL BE AN INCREMENTING BINARY COUNT PATTERN. THE DATA READBACK FROM THE CTL REGISTER WILL BE THE ONES COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER.

TEST 37:

THIS TEST WILL CHECK THE DATA PATH FROM THE MODE REGISTER TO THE ADDRESS BUS.

TO DO THIS, THE TEST WILL ENABLE THE DATA PATH FROM THE MODE REGISTER TO THE EODAL BUS, TO THE CDAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS. THIS IS DONE BY SETTING XBCLR H AND PBCLR H TO THE HIGH STATE AND BY SETTING ADAL12 H AND ADAL10 H TO ONES. THE TARGET MODE READBACK REGISTER WILL ALSO BE CHECKED TO HAVE BEEN LOADED WITH THE EIDAL BUS DATA WHEN THE SIGNAL XBCLR L IS SET TO THE HIGH STATE FROM THE LOW STATE. THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING DATA PATTERNS, 146063, 031714, 125252, 052525, 177777 AND 000000. FOR EACH DATA PATTERN LOADED, THE PROGRAM WILL CHECK THE DATA TO BE PRESENT ON THE THE EODAL BUS, THE EIDAL BUS, AND THE ADDRESS BUS. THE TEST WILL ALSO CHECK THAT EACH PATTERN CAN BE LOADED INTO THE TARGET MODE READBACK REGISTER.

TEST 38:

THIS TEST WILL CHECK THE DATA PATH FROM THE DIAGNOSTIC ADDRESS REGISTER TO THE OLD FORCE JUMP ADDRESS REGISTER, TO THE EODAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS. THIS PART OF THE TEST USES THE PAUSE STATE MACHINE LOGIC TO LOAD THE OLD FORCE JUMP ADDRESS REGISTER AND TO PLACE THE OLD FORCE JUMP ADDRESS REGISTER DATA ONTO THE EODAL BUS. WHEN THE OLD FORCE JUMP ADDRESS REGISTER DATA IS ENABLED TO THE EODAL BUS, THE TEST WILL ENABLE THE DATA TO THE TDAL BUS AND LATCH THE DATA INTO THE TDAL DIAGNOSTIC LATCHES. THE NEXT PART OF THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC LATCHES CAN BE ENABLED TO THE EIDAL BUS AND THAT THE EIDAL BUS CAN BE ENABLED TO THE EODAL BUS THROUGH THE DATA BUS.

TEST 39:

THIS TEST WILL CHECK THAT THE FDAL REGISTER CAN BE ENABLED TO THE EODAL BUS VIA THE SIGNAL INTER L AND THAT THE EODAL BUS CAN BE ENABLED TO THE EIDAL BUS VIA THE SIGNAL COLB L. THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLEARED WHEN THE SIGNAL INTER L IS ASSERTED LOW. A BINARY COUNT DATA PATTERN WILL BE LOADED INTO THE FDAL REGISTER STARTING WITH A DATA PATTERN OF ONE AND INCREMENTING BY FOUR UNTIL THE DATA PATTERN 375 HAS BEEN LOADED AND CHECKED.

TEST 40:

THIS TEST WILL CHECK THAT THE SIGNALS READ H AND MSDI H CAN BE ASSERTED HIGH AND LOW. THESE SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE LOGIC LEVELS ON THE INPUT SIGNALS TO THE GATES WHICH GENERATE THE SIGNALS. THE SIGNALS READ H AND MSDI H ARE READ IN THE VDAL REGISTER AS BITS 3 AND 6 RESPECTIVELY.

TEST 41:

THIS TEST WILL CHECK THAT THE SIGNALS FETCT H AND BTS1 H CAN BE ASSERTED HIGH AND LOW. THESE TWO SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE INPUT SIGNALS TO THE GATES WHICH GENERATE THESE SIGNALS. THE PAUSE STATE MACHINE LOGIC IS USED TO TEST THE SIGNAL FETCT H. THE SIGNAL FETCT H IS ALSO CHECKED ON THE SIGNAL BTS1 H. THE SIGNAL BTS1 H IS READ IN THE VDAL REGISTER ON BIT 5.

TEST 42:

THIS TEST WILL CHECK THAT THE SIGNAL EDEOC H CAN BE SET TO THE HIGH STATE AND TO THE LOW STATE. THE SIGNAL EDEOC H IS READ IN THE VDAL REGISTER ON BIT 4 WHEN ADAL REAGISTER BIT 10 IS SET TO A ONE. THE PROGRAM WILL CHECK THE SIGNAL EDEOC H TO SET AND CLEAR BY CHANGING THE LOGIC LEVELS ON THE FOLLOWING SIGNALS: ADAL9 H, PSM L, INTER L, REFR L, XRAS H, XRAS L, XCAS H, XCAS L AND SOP L. THE

TEST WILL USE THE SIGNAL EDEOC H TO CHECK THAT THE REFR FLIP-FLOP CAN BE SET AND CLEARED. THE REFR FLIP-FLOP WILL BE CHECKED TO BE CLEARED BY CHANGING THE LOGIC LEVELS ON THE SIGNALS ADAL7 H AND XCAS H. THE REFR FLIP-FLOP CAN NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INV D L BECAUSE OF THE LOGIC DESIGN.

TEST 43:

THIS TEST WILL CHECK THE TARGET EMULATORS INTERRUPT LOGIC USING THE SIGNALS TOBRK H AND BRK H TO CAUSE INTERRUPT REQUESTS. THE TEST WILL CHECK THAT NO INTERRUPTS OCCUR WHEN THE INTERRUPT ENABLE BIT IS CLEARED AND THE INTERRUPT REQUEST SIGNAL IS ASSERTED HIGH. THE TEST WILL CHECK THAT AN INTERRUPT WILL OCCUR WHEN THE INTERRUPT ENABLE BIT IS SET AND THE SIGNAL TOBRK H IS ASSERTED HIGH. THE TEST WILL CHECK THAT THE BREAK LATCH FLIP-FLOP CAN BE SET, CLEARED, AND THAT IT CAN CAUSE AN INTERRUPT.

TEST 44:

THIS TEST WILL CHECK THAT THE SIGNALS ADAL 15:9, ADAL 7:3, ADAL 1:0, HDAL 15:0, FDAL7 H - FDAL0 H, VDAL7 H, VDAL2 H - VDAL0 H, GDAL15 H, GDAL2 H - GDAL0 H, AND MR15 H - MR0 H CAN ALL BE SET TO ONES. THEN A BRESET INSTRUCTION IS ISSUED AND THESE SIGNALS ARE TESTED TO THEN BE ZEROS. THEN THE PAUSE STATE WORKING FLIP-FLOP AND THE SINGLE STEP BREAK FLIP-FLOP ARE SET TO ONES AND AGAIN A BRESET INSTRUCTION IS ISSUED AND THESE FLIP-FLOPS ARE TESTED TO THEN BE ZEROS.

TEST 45:

THIS TEST WILL CHECK THAT THE T-11 CAN BE POWERED-UP TO ALL ITS STARTING ADDRESSES AND THAT IT CAN RUN WITH DIFFERENT MODES SELECTED. THE PROGRAM WILL USE THE PAUSE STATE MACHINE TO CHECK THAT THE T-11 POWERED-UP TO THE STARTING ADDRESS SELECTED BY THE MODE REGISTER. THE PROGRAM WILL SELECT THE FOLLOWING T-11 MODES: 16 BIT STATIC, 16 BIT DYNAMIC 4K/16K, 16 BIT DYNAMIC 64K, 8 BIT STATIC, 8 BIT DYNAMIC 4K/16K AND 8 BIT DYNAMIC 64K. FOR EACH MODE SELECTED, THE PROGRAM WILL CHECK THAT THE T-11 CAN BE POWERED-UP AT EACH OF ITS STARTING ADDRESSES. THE PROGRAM WILL SELECT THE CLOCK ON THE TARGET EMULATOR MODULE TO PROVIDE THE TIMING TO THE T-11 CHIP. THE TEST WILL ALSO CHECK THAT THE NEW FORCE JUMP ADDRESS REGISTER CAN BE LOADED AND THAT ITS CONTENTS CAN BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER.

1364			
1365			
1366			.TITLE PROGRAM HEADER AND TABLES
1367			.SBTTL PROGRAM HEADER
1368			
1369			.ENABL ABS
1370			.ENABL AMA
1371			.DSABL GBL
1372	002000		. = 2000
1373			
1374	002000		BGNMOD
1375			
1376			:++
1377			: THE PROGRAM HEADER IS THE INTERFACE BETWEEN
1378			: THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
1379			:--
1380			
1381	002000		POINTER BGNSETUP
1382			
1383			
1384	002000		HEADER CVDCB,0,60,0,PRI07
1385	002000		LSNAME:: :DIAGNOSTIC NAME
1386	002000	103	.ASCII /C/
1387	002001	126	.ASCII /V/
1388	002002	103	.ASCII /C/
1389	002003	104	.ASCII /D/
1390	002004	103	.ASCII /C/
1391	002005	000	.BYTE 0
1392	002006	000	.BYTE 0
1393	002007	000	.BYTE 0
1394	002010		LSREV:: :REVISION LEVEL
1395	002010	102	.ASCII /B/
1396	002011		LSDEPO:: :0
1397	002011	060	.ASCII /O/
1398	002012		LSUNIT:: :NUMBER OF UNITS
1399	002012	000001	.WORD T\$PTHV
1400	002014		LS\$TML:: :LONGEST TEST TIME
1401	002014	000074	.WORD 60.
1402	002016		LS\$HPCP:: :POINTER TO H.W. QUES.
1403	002016	036350	.WORD LS\$HARD
1404	002020		LS\$SPCP:: :POINTER TO S.W. QUES.
1405	002020	000000	.WORD 0
1406	002022		LS\$HPTP:: :PTR. TO DEF. H.W. PTABLE
1407	002022	002260	.WORD LS\$HW
1408	002024		LS\$SPTP:: :PTR. TO S.W. PTABLE
1409	002024	000000	.WORD 0
1410	002026		LS\$LADP:: :DIAG. END ADDRESS
1411	002026	036542	.WORD LS\$LAST
1412	002030		LS\$STA:: :RESERVED FOR APT STATS
1413	002030	000000	.WORD 0
1414	002032		LS\$CO::
1415	002032	000000	.WORD 0
1416	002034		LS\$DTYP:: :DIAGNOSTIC TYPE
1417	002034	000000	.WORD 0
1418	002036		LS\$APT:: :APT EXPANSION
1419	002036	000000	.WORD 0

1420	002040		LSDTP::		:PTR. TO DISPATCH TABLE
1421	002040	002124	.WORD	LSDISPATCH	
1422	002042		LSPRIO::		:DIAGNOSTIC RUN PRIORITY
1423	002042	000340	.WORD	PRI07	
1424	002044		LSENV1::		:FLAGS DESCRIBE HOW IT WAS SETUP
1425	002044	000000	.WORD	0	
1426	002046		LSEXP1::		:EXPANSION WORD
1427	002046	000000	.WORD	0	
1428	002050		LSMREV::		:SVC REV AND EDIT #
1429	002050	003	.BYTE	CSREVISION	
1430	002051	003	.BYTE	CSEDIT	
1431	002052		LSEF::		:DIAG. EVENT FLAGS
1432	002052	000000	.WORD	0	
1433	002054	000000	.WORD	0	
1434	002056		LSSPC::		
1435	002056	000000	.WORD	0	
1436	002060		LSDEVP::		: POINTER TO DEVICE TYPE LIST
1437	002060	002350	.WORD	LSDVTYP	
1438	002062		LSREPP::		:PTR. TO REPORT CODE
1439	002062	000000	.WORD	0	
1440	002064		LSEXP4::		
1441	002064	000000	.WORD	0	
1442	002066		LSEXP5::		
1443	002066	000000	.WORD	0	
1444	002070		LSAUT::		:PTR. TO ADD UNIT CODE
1445	002070	000000	.WORD	0	
1446	002072		LSDUT::		:PTR. TO DROP UNIT CODE
1447	002072	000000	.WORD	0	
1448	002074		LSLUN::		:LUN FOR EXERCISERS TO FILL
1449	002074	000000	.WORD	0	
1450	002076		LSDESP::		:POINTER TO DIAG. DESCRIPTION
1451	002076	002360	.WORD	LSDESC	
1452	002100		LSLOAD::		:GENERATE SPECIAL AUTOLOAD EMT
1453	002100	104035	EMT	ESLOAD	
1454	002102		LSETP::		:POINTER TO ERR TBL
1455	002102	000000	.WORD	0	
1456	002104		LSICP::		:PTR. TO INIT CODE
1457	002104	010066	.WORD	LSINIT	
1458	002106		LSCCP::		:PTR. TO CLEAN-UP CODE
1459	002106	010300	.WORD	LSCLEAN	
1460	002110		LSACP::		:PTR. TO AUTO CODE
1461	002110	010276	.WORD	LSAUTO	
1462	002112		LSPRT::		:PTR. TO PROTECT TABLE
1463	002112	010060	.WORD	LSPROT	
1464	002114		LSTEST::		:TEST NUMBER
1465	002114	000000	.WORD	0	
1466	002116		LSDLY::		:DELAY COUNT
1467	002116	000000	.WORD	0	
1468	002120		LSHIME::		:PTR. TO HIGH MEM
1469	002120	000000	.WORD	0	
1470					

1471
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1478 002122
1479 002122 000055
1480 002124
1481 002124 010344
1482 002126 010352
1483 002130 010436
1484 002132 010524
1485 002134 010574
1486 002136 010660
1487 002140 010746
1488 002142 011016
1489 002144 011062
1490 002146 011160
1491 002150 011250
1492 002152 011342
1493 002154 011416
1494 002156 011466
1495 002160 011556
1496 002162 011650
1497 002164 011724
1498 002166 011774
1499 002170 012072
1500 002172 012172
1501 002174 012246
1502 002176 012320
1503 002200 012442
1504 002202 012566
1505 002204 012666
1506 002206 012770
1507 002210 013236
1508 002212 013662
1509 002214 014570
1510 002216 015562
1511 002220 016752
1512 002222 020046
1513 002224 020316
1514 002226 021604
1515 002230 023156
1516 002232 023534
1517 002234 024356
1518 002236 024706
1519 002240 026132
1520 002242 026552
1521 002244 030472
1522 002246 031502
1523 002250 033236
1524 002252 034452
1525 002254 035622
1526

.SBTTL DISPATCH TABLE

:++
: THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
: IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
:--

DISPATCH 45.
.WORD 45
LSDISPATCH: :
.WORD T1
.WORD T2
.WORD T3
.WORD T4
.WORD T5
.WORD T6
.WORD T7
.WORD T8
.WORD T9
.WORD T10
.WORD T11
.WORD T12
.WORD T13
.WORD T14
.WORD T15
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.WORD T44
.WORD T45

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1536 002256
1537 002256 000003
1538 002260
1539 002260
1540
1541 002260 163010
1542 002262 000370
1543 002264 000002
1544
1545
1546 002266
1547 002766
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558 002266
1559 002266 000000
1560 002270
1561 002270
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1563
1564 002270
1565 002270
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1567 002270
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.SBTTL DEFAULT HARDWARE P-TABLE

:++
: THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF
: THE TEST-DEVICE PARAMETERS. THE STRUCTURE OF THIS TABLE
: IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,
: AND IS USED AS A "TEMPLATE" FOR BUILDING THE P-TABLES.
:--

          BGNHW  DFPTBL
          .WORD  L10000-L$HW/2
L$HW::
DFPTBL::

          .WORD  163010           :CSR ADDRESS
          .WORD  370             :VECTOR ADDRESS
          .WORD  2               :DEVICE SELECTION NUMBER

          ENDPHW
L10000:

.SBTTL SOFTWARE P-TABLE

:++
: THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE
: PROGRAM AS OPERATIONAL PARAMETERS. THESE PARAMETERS ARE
: SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR
: AT RUN TIME.
:--

          BGNSW  SFPTBL
          .WORD  L10001-L$SW/2
L$SW::
SFPTBL::

          ENDSW
L10001:

          ENDMOD
```


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002270

100000
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020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

001000
000400
000200
000100
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000020
000010
000004
000002
000001

000040
000037
000036
000035
000034

.TITLE GLOBAL AREAS
.SBTTL GLOBAL EQUATES SECTION

BGNMOD

..++
: THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
: ARE USED IN MORE THAN ONE TEST.
:--

EQUALS

: BIT DIFINITIONS

:
BIT15== 100000
BIT14== 40000
BIT13== 20000
BIT12== 10000
BIT11== 4000
BIT10== 2000
BIT09== 1000
BIT08== 400
BIT07== 200
BIT06== 100
BIT05== 40
BIT04== 20
BIT03== 10
BIT02== 4
BIT01== 2
BIT00== 1

:
BIT9== BIT09
BIT8== BIT08
BIT7== BIT07
BIT6== BIT06
BIT5== BIT05
BIT4== BIT04
BIT3== BIT03
BIT2== BIT02
BIT1== BIT01
BIT0== BIT00

: EVENT FLAG DEFINITIONS
: EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION

:
EF.START== 32. : START COMMAND WAS ISSUED
EF.RESTART== 31. : RESTART COMMAND WAS ISSUED
EF.CONTINUE== 30. : CONTINUE COMMAND WAS ISSUED
EF.NEW== 29. : A NEW PASS HAS BEEN STARTED
EF.PWR== 28. : A POWER-FAIL/POWER-UP OCCURRED

:
: PRIORITY LEVEL DEFINITIONS
:

1624	000340	PRI07== 340	
1625	000300	PRI06== 300	
1626	000240	PRI05== 240	
1627	000200	PRI04== 200	
1628	000140	PRI03== 140	
1629	000100	PRI02== 100	
1630	000040	PRI01== 40	
1631	000000	PRI00== 0	
1632		:	
1633		:OPERATOR FLAG BITS	
1634		:	
1635	000004	EVL== 4	
1636	000010	LOT== 10	
1637	000020	ADR== 20	
1638	000040	IDU== 40	
1639	000100	ISR== 100	
1640	000200	UAM== 200	
1641	000400	bOE== 400	
1642	001000	PN== 1000	
1643	002000	PRI== 2000	
1644	004000	IXE== 4000	
1645	010000	IBE== 10000	
1646	020000	IER== 20000	
1647	040000	LOE== 40000	
1648	100000	HOE== 100000	
1649		:	
1650		:CONTROL REGISTER 0 (GDAL BITS 15:0)	
1651		:	
1652		:	
1653		:	
1654	100000	GDAL15==BIT15	:BIT15=1 READ DEVICE TYPE IN 15:8 :TE DEVICE TYPE EQUALS 0000
1655			:
1656			:BIT15=0 READ DEVICE NUMBER INTO
1657			:BITS 11:8
1658			:
1659			:
1660	040000	GDAL14==BIT14	:ALWAYS A 0 ON READ
1661	020000	GDAL13==BIT13	:ALWAYS A 0 ON READ
1662	010000	GDAL12==BIT12	:ALWAYS A 0 ON READ
1663			:
1664	004000	GDAL11==BIT11	:BITS 11-8 ARE USED TO SELECT THE
1665	002000	GDAL10==BIT10	:DEVICE NUMBER TO ASSERT THE SIGNAL
1666	001000	GDAL9== BIT9	:DEVE L. WHEN SELECTING TE THESE BITS
1667	000400	GDAL8== BIT8	:MUST = THE SETTING OF DEV 3 - DEV 0
1668			:
1669	000200	GDAL7== BIT7	:SINGLE STEP BREAK INDICATOR (READ ONLY)
1670	000100	GDAL6== BIT6	:TIMEOUT BREAK INDICATOR (READ ONLY)
1671	000040	GDAL5== BIT5	:MEMORY SIM BREAK INDICATOR (READ ONLY)
1672	000020	GDAL4== BIT4	:STATE ANALYZER BREAK INDICATOR (READ ONLY)
1673	000010	GDAL3== BIT3	:ENABLE INTERRUPTS WHEN = TO 1
1674	000004	GDAL2== BIT2	:POINTER FOR EXTENDED REG SELECT
1675	000002	GDAL1== BIT1	:POINTER FOR EXTENDED RFG SELECT
1676	000001	GDAL0== BIT0	:POINTER FOR EXTENDED REG SELECT
1677			:
1678	000200	SSBRK== GDAL7	:SINGLE STEP BREAK INDICATOR (READ ONLY)
1679	000100	TOBRK== GDAL6	:TIMEOUT BREAK INDICATOR (READ ONLY)

1680	000040	MSBRK== GDAL5	:MEMORY SIM BREAK INDICATOR (READ ONLY)
1681	000020	EDBRK== GDAL4	:STATE ANALYZER BREAK INDICATOR (READ ONLY)
1682			
1683			
1684		:CONTROL REGISTER 2 (ADAL BITS 15:0)	
1685		:	
1686			
1687	100000	ADAL15==BIT15	:SELECT COLUMN AI FOR STATE ANALYZER
1688	040000	ADAL14==BIT14	:1 - SELECT ROW/COLUMN FOR AI TO STATE ANALYZER
1689			:0 - SELECT SERVICE FOR AI TO STATE ANALYZER
1690	020000	ADAL13==BIT13	:ENABLE SERVICE FOR EMULATOR
1691	010000	ADAL12==BIT12	:ENABLE MODE FROM EMULATOR
1692	004000	ADAL11==BIT11	:DISABLE SERVICE TO THE TARGET
1693	002000	ADAL10==BIT10	:MASTER SWITCH
1694	001000	ADAL9== BIT9	:ENABLE STATE ANALYZER CLOCKS (1)
1695	000400	ADAL8== BIT8	:ENABLE TIMEOUT BREAK
1696	000200	ADAL7== BIT7	:ENABLE REFRESH TO STATE ANALYZER
1697	000100	ADAL6== BIT6	:
1698	000040	ADAL5== BITS	:1 - ENABLE SINGLE STEP BREAK
1699			:0 - DISABLE SINGLE STEP BREAK
1700	000020	ADAL4== BIT4	:1 - PAUSE STATE MACHINE (RUN MODE)
1701			:0 - PAUSE STATE MACHINE (PAUSE MODE)
1702	000010	ADAL3== BIT3	:POWER-UP FROM TARGET (1)
1703	000004	ADAL2== BIT2	:POWER-UP FROM T-11
1704	000002	ADAL1== BIT1	:ENABLE INTERNAL CLOCK (1)
1705	000001	ADAL0== BIT0	:RESETS BREAK LOGIC (1)
1706			
1707			
1708		:CONTROL REGISTER 4 (VDAL BITS 15:0)	
1709		:	
1710			
1711	100000	VDAL15==BIT15	:TDFI H - TAKE NEW FORCE JUMP ADDRESS (READ ONLY)
1712	040000	VDAL14==BIT14	:EP8N H - 8 BIT ADDRESS HB F/F (READ ONLY)
1713	020000	VDAL13==BIT13	:EP8G H - 8 BIT ADDRESS LB F/F (READ ONLY)
1714	010000	VDAL12==BIT12	:EP8F H - 8 BIT INSTR HB F/F (READ ONLY)
1715	004000	VDAL11==BIT11	:EPFN H - 16 BIT ADDRESS F/F (READ ONLY)
1716	002000	VDAL10==BIT10	:EPSF H - PAUSE STATE SYNC F/F (READ ONLY)
1717	001000	VDAL9== BIT9	:PSMW H - PAUSE STATE WORKING F/F (READ ONLY)
1718	000400	VDAL8== BIT8	:PSMW H - GET NEW ADDRESS F/F (READ ONLY)
1719	000200	VDAL7== BIT7	:DIAGNOSTIC FETCT H (R/W)
1720	000100	VDAL6== BIT6	:MSDI H - LOGIC LEVEL MSDI H (READ ONLY)
1721	000040	VDAL5== BITS	:BTS1 H - LOGIC LEVEL BTS1 H (READ ONLY)
1722	000020	VDAL4== BIT4	:EDEOC H - LOGIC LEVEL EDEOC H (READ ONLY)
1723	000010	VDAL3== BIT3	:READ H - LOGIC LEVEL READ H (READ ONLY)
1724	000004	VDAL2== BIT2	:CLOCK TAI, TDAL, 0 PAUSE STATE MACHINE (R/W)
1725	000002	VDAL1== BIT1	:SPARE
1726	000001	VDAL0== BIT0	:ENABLE TAI AND TDAL READBACK FROM POD (R/W)
1727			
1728			
1729		:CONTROL REGISTER 6 (HDAL BITS 15:0)	
1730		:	
1731			
1732	100000	HDAL15==BIT15	:1/0 - PULSE SIGNAL XPI L
1733	040000	HDAL14==BIT14	:1/0 - PULSE SIGNAL EIDAL17 H
1734	020000	HDAL13==BIT13	:1/0 - PULSE SIGNAL XCAS H
1735	010000	HDAL12==BIT12	:1/0 - PULSE SIGNAL XRAS H

1736	004000	HDAL11==BIT11	:1/0 - PULSE SIGNAL EIDAL16 H
1737	002000	HDAL10==BIT10	:SPARE
1738	001000	HDAL9== BIT9	:1 - ENABLE DIAG ADDRESS TO ADDRESS BUS
1739			:0 - ENABLE EIDAL BUS TO ADDRESS BUS
1740			: WHEN ADAL10 H IS SET TO A ONE AND
1741			: DISABLE DIAG ADDRESS FROM ADDRESS BUS
1742	000400	HDAL8== BIT8	:1/0 - PULSE CREADY H
1743	000200	HDAL7== BIT7	:1/0 - PULSE PBCLR H
1744	000100	HDAL6== BIT6	:1/0 - PULSE PSEL1 H
1745	000040	HDAL5== BIT5	:1/0 - PULSE PSELO H
1746	000020	HDAL4== BIT4	:1/0 - PULSE PR/WHB L
1747	000010	HDAL3== BIT3	:1/0 - PULSE PR/WLB L
1748	000004	HDAL2== BIT2	:1 - ENABLES DIAG CONTROL OF T-11 TIMING
1749			: AND CONTROL SIGNALS
1750			:0 - ENABLES T-11 TO GENERATE SIGNALS
1751	000002	HDAL1== BIT1	:SPARE
1752	000001	HDAL0== BIT0	:1/0 - PULSE MSDI H
1753			
1754			
1755		:CONTROL REGISTER 6 (MODE REG BITS MR 15:0)	
1756			
1757			
1758	100000	MR15== BIT15	
1759	040000	MR14== BIT14	
1760	020000	MR13== BIT13	
1761	010000	MR12== BIT12	
1762	004000	MR11== BIT11	:1 - 8 BIT ADDRESS SELECTION
1763			:0 - 16 BIT ADDRESS SELECTION
1764	002000	MR10== BIT10	
1765	001000	MR9== BIT9	
1766	000400	MR8== BIT8	
1767	000200	MR7== BIT7	
1768	000100	MR6== BIT6	
1769	000040	MR5== BIT5	
1770	000020	MR4== BIT4	
1771	000010	MR3== BIT3	
1772	000004	MR2== BIT2	
1773	000002	MR1== BIT1	
1774	000001	MR0== BIT0	
1775			
1776			
1777		:CONTROL REGISTER 6 (FDAL BITS 7:0)	
1778			
1779			
1780	000200	FDAL7== BIT7	: INTERRUPT VECTOR
1781	000100	FDAL6== BIT6	: INTERRUPT VECTOR
1782	000040	FDAL5== BIT5	: INTERRUPT VECTOR
1783	000020	FDAL4== BIT4	: INTERRUPT VECTOR
1784	000010	FDAL3== BIT3	: INTERRUPT VECTOR
1785	000004	FDAL2== BIT2	: INTERRUPT VECTOR
1786	000002	FDAL1== BIT1	:SPARE
1787	000001	FDAL0== BIT0	:1 - ENABLES EOAI 7:0 BUS TO BE READ
1788			:0 - ENABLES CTL 7:0 REG TO BE READ
1789			
1790			
1791		:CONTROL REGISTER 6 (DIAG. ADDR BITS 15:0)	

1792		:	
1793			
1794	100000	ADDR15==	BIT15
1795	040000	ADDR14==	BIT14
1796	020000	ADDR13==	BIT13
1797	010000	ADDR12==	BIT12
1798	004000	ADDR11==	BIT11
1799	002000	ADDR10==	BIT10
1800	001000	ADDR9==	BIT9
1801	000400	ADDR8==	BIT8
1802	000200	ADDR7==	BIT7
1803	000100	ADDR6==	BIT6
1804	000040	ADDR5==	BIT5
1805	000020	ADDR4==	BIT4
1806	000010	ADDR3==	BIT3
1807	000004	ADDR2==	BIT2
1808	000002	ADDR1==	BIT1
1809	000001	ADDR0==	BIT0
1810			

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002274 000000
002276 000000

002300 163010
002302 163012
002304 163014
002306 163016

002310 000000
002312 000000
002314 000000
002316 000000

002320 000000
002322 000000
002324 000000
002326 000000

002330 000000
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002334 000000
002336 000000
002340 000000

002342 000000
002344 000000
002346 000000

.SBTTL GLOBAL DATA SECTION

;++
: THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
: IN MORE THAN ONE TEST.
:--

ERRTBL

LSERRTBL::
ERRTYP:: .WORD 0
ERRNBR:: .WORD 0
ERRMSG:: .WORD 0
ERRBLK:: .WORD 0

:GLOBAL DATA FOR TARGET EMULATOR

REG0:: .WORD 163010 ;CONTROL REGISTER 0
REG2:: .WORD 163012 ;CONTROL REGISTER 2
REG4:: .WORD 163014 ;CONTROL REGISTER 4
REG6:: .WORD 163016 ;CON ROL REGISTER 6

IDDEV:: .WORD 0 ;TARGET EMULATOR DEVICE # (11:8)
TEVECT:: .WORD 0 ;TARGET EMULATOR VECTOR ADDRESS
UNITNB:: .WORD 0 ;
IDTYPE:: .WORD 0 ;TARGET EMULATOR DEVICE TYPE (15-8)

R0LOAD:: .WORD 0 ;WORD LOADED INTO REGISTER 0
R0GOOD:: .WORD 0 ;EXPECTED REG 0
R0MASK:: .WORD 0 ;BITS TO BE IGNORED ON COMPARE
R0BAD:: .WORD 0 ;DATA READ MASKED WITH R0MASK

R2LOAD:: .WORD 0 ;WORD LOADED INTO REGISTER 2
R2READ:: .WORD 0 ;ACTUAL REG 2 READ

R4LOAD:: .WORD 0 ;WORD LOADED INTO REGISTER 4
R4GOOD:: .WORD 0 ;EXPECTED DATA FROM REGISTER 4
R4BAD:: .WORD 0 ;DATA READ FROM REGISTER 4

R6LOAD:: .WORD 0 ;WORD LOADED INTO REGISTER 6
R6READ:: .WORD 0 ;ACTUAL REGISTER 6 READ
R6MASK:: .WORD 0 ;BITS TO BE IGNORED

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002350
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002350 042103 026523 030461
002356 000
002360

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002360
002360 040524 043522 052105
002366 042440 052515 040514
002374 047524 020122 044504
002402 043501 000056

002406 042107 046101 030440
002414 035065 020060 042522
002422 020107 051105 047522
002430 000122
002432 047125 054105 042520
002440 052103 042105 044440
002446 052116 051105 052522
002454 052120 047440 041503
002462 051125 042105 000
002467 106 044501 042514
002474 020104 047524 044440
002502 052116 051105 052522
002510 052120 000

002513 101 040504 020114
002520 032461 030072 051040
002526 043505 042440 051122
002534 051117 000

```
.SBTTL GLOBAL TEXT SECTION

:++
: THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
: MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
: MORE THAN ONE TEST.
:--

:
: NAMES OF DEVICES SUPPORTED BY PROGRAM
:
:      DEVTYP <CDS-11>
L$DVTYP::
:      .ASCIZ /CDS-11/
:
:      .EVEN

: TEST DESCRIPTION
:
:      DESCRIPT <TARGET EMULATOR DIAG.>
L$DESC::
:      .ASCIZ /TARGET EMULATOR DIAG./
:
:      .EVEN

: ASCII MESSAGES USED BY ERROR CALLS
:
: CONTROL REGISTER 0 ERROR MESSAGES
GDALRG:: .ASCIZ /GDAL 15:0 REG ERROR/

UNEXIN:: .ASCIZ /UNEXPECTED INTERRUPT OCCURED/

NOINT:: .ASCIZ /FAILED TO INTERRUPT/

: CONTROL REGISTER 2 ERROR MESSAGES
ADALRG:: .ASCIZ /ADAL 15:0 REG ERROR/
```

1911					:CONTROL REGISTER 4 ERROR MESSAGES
1912					
1913	002537	126	040504	020114	VDALRG::.ASCIZ /VDAL 7:0 OR PAUSE STATE MACHINE ERROR/
1914	002544	035067	020060	051117	
1915	002552	050040	052501	042523	
1916	002560	051440	040524	042524	
1917	002566	046440	041501	044510	
1918	002574	042516	042440	051122	
1919	002602	051117	000		
1920					
1921					:CONTROL REGISTER 6 ERROR MESSAGES
1922					
1923	002605	110	040504	020114	HDALRG::.ASCIZ /HDAL 15:0 REG ERROR/
1924	002612	032461	030072	051040	
1925	002620	043505	042440	051122	
1926	002626	051117	000		
1927	002631	115	020122	032461	MODREG::.ASCIZ /MR 15:0 REG ERROR/
1928	002636	030072	051040	043505	
1929	002644	042440	051122	051117	
1930	002652	000			
1931	002653	106	040504	020114	FDALRG::.ASCIZ /FDAL 7:0 REG ERROR/
1932	002660	035067	020060	042522	
1933	002666	020107	051105	047522	
1934	002674	000122			
1935	002676	047505	044501	033440	EOAIFD::.ASCIZ /EOAI 7:0 OR FDAL 7:0 REG ERROR/
1936	002704	030072	047440	020122	
1937	002712	042106	046101	033440	
1938	002720	030072	051040	043505	
1939	002726	042440	051122	051117	
1940	002734	000			
1941	002735	104	040511	020107	ADDRRG::.ASCIZ /DIAG ADDR 15:0 REG ERROR/
1942	002742	042101	051104	030440	
1943	002750	035065	020060	042522	
1944	002756	020107	051105	047522	
1945	002764	000122			
1946	002766	047506	041522	020105	FJADRG::.ASCIZ /FORCE JUMP ADDRESS READBACK REG ERROR/
1947	002774	052512	050115	040440	
1948	003002	042104	042522	051523	
1949	003010	051040	040505	041104	
1950	003016	041501	020113	042522	
1951	003024	020107	051105	047522	
1952	003032	000122			
1953	003034	047111	052123	020122	IEODAL::.ASCIZ /INSTR REG TO EODAL BUS READBACK ERROR/
1954	003042	042522	020107	047524	
1955	003050	042440	042117	046101	
1956	003056	041040	051525	051040	
1957	003064	040505	041104	041501	
1958	003072	020113	051105	047522	
1959	003100	000122			
1960	003102	047515	042504	051040	MEODAL::.ASCIZ /MOJE REG TO EODAL BUS READBACK ERROR/
1961	003110	043505	052040	020117	
1962	003116	047505	040504	020114	
1963	003124	052502	020123	042522	
1964	003132	042101	040502	045503	
1965	003140	042440	051122	051117	
1966	003146	000			

1967	003147	106	051117	042503	FEDAL::ASCIZ /FORCE JUMP ADDRESS REG TO EODAL BUS READBACK ERROR/
1968	003154	045040	046525	020120	
1969	003162	042101	051104	051505	
1970	003170	020123	042522	020107	
1971	003176	047524	042440	042117	
1972	003204	046101	041040	051525	
1973	003212	051040	040505	041104	
1974	003220	041501	020113	051105	
1975	003226	047522	000122		
1976	003232	052103	020114	035067	CTLFDL::ASCIZ /CTL 7:0 OR FDAL 7:0 REG ERROR/
1977	003240	020060	051117	043040	
1978	003246	040504	020114	035067	
1979	003254	020060	042522	020107	
1980	003262	051105	047522	000122	
1981	003270	047515	042504	051040	MEIDAL::ASCIZ /MODE REG TO EIDAL BUS READBACK ERROR/
1982	003276	043505	052040	020117	
1983	003304	044505	040504	020114	
1984	003312	052502	020123	042522	
1985	003320	042101	040502	045503	
1986	003326	042440	051122	051117	
1987	003334	000			
1988	003335	115	042117	020105	MTOTMR::ASCIZ /MODE REG TO TARGET MODE REG ERROR/
1989	003342	042522	020107	047524	
1990	003350	052040	051101	042507	
1991	003356	020124	047515	042504	
1992	003364	051040	043505	042440	
1993	003372	051122	051117	000	
1994	003377	115	042117	020105	MADDRS::ASCIZ /MODE REG TO ADDRESS BUS READBACK ERROR/
1995	003404	042522	020107	047524	
1996	003412	040440	042104	042522	
1997	003420	051523	041040	051525	
1998	003426	051040	040505	041104	
1999	003434	041501	020113	051105	
2000	003442	047522	000122		
2001	003446	046117	020104	045106	FJAEID::ASCIZ /OLD FJA TO EIDAL BUS ERROR/
2002	003454	020101	047524	042440	
2003	003462	042111	046101	041040	
2004	003470	051525	042440	051122	
2005	003476	051117	000		
2006	003501	117	042114	043040	FJAADR::ASCIZ /OLD FJA TO ADDRESS BUS ERROR/
2007	003506	040512	052040	020117	
2008	003514	042101	051104	051505	
2009	003522	020123	052502	020123	
2010	003530	051105	047522	000122	
2011	003536	046117	020104	045106	FJATDL::ASCIZ /OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR/
2012	003544	020101	047524	052040	
2013	003552	040504	020114	040514	
2014	003560	041524	020110	047524	
2015	003566	042440	042111	046101	
2016	003574	041040	051525	042440	
2017	003602	051122	051117	000	
2018	003607	124	040504	020114	TDLEOD::ASCIZ /TDAL LATCH TO EIDAL TO DATA TO EODAL BUS ERROR/
2019	003614	040514	041524	020110	
2020	003622	047524	042440	042111	
2021	003630	046101	052040	020117	
2022	003636	040504	040524	052040	

2023	003644	020117	047505	040504	
2024	003652	020114	052502	020123	
2025	003660	051105	047522	000122	
2026	003666	042106	046101	051040	FDALĒO:::ASCIZ /FDAL REG TO EODAL BUS ERROR/
2027	003677	043505	052040	020117	
2028	003702	047505	040504	020114	
2029	003710	052502	020123	051105	
2030	003716	047522	000122		
2031	003722	042106	046101	051040	FDALĒI:::ASCIZ /FDAL REG TO EODAL BUS TO EIDAL BUS ERROR/
2032	003730	043505	052040	020117	
2033	003736	047505	040504	020114	
2034	003744	052502	020123	047524	
2035	003752	042440	042111	046101	
2036	003760	041040	051525	042440	
2037	003766	051122	051117	000	
2038	003773	120	052501	042523	NOPSM:::ASCIZ /PAUSE STATE NOT ENTERED WHEN T-11 CHIP IS POWERED-UP/
2039	004000	051440	040524	042524	
2040	004006	047040	052117	042440	
2041	004014	052116	051105	042105	
2042	004022	053440	042510	020116	
2043	004030	026524	030461	041440	
2044	004036	044510	020120	051511	
2045	004044	050040	053517	051105	
2046	004052	042105	052455	000120	
2047	004060	047506	041522	020105	FJSTAD:::ASCIZ /FORCE JUMP ADDRESS NOT = EXPECTED T-11 START-RESTART ADDRESS/
2048	004066	052512	050115	040440	
2049	004074	042104	042522	051523	
2050	004102	047040	052117	036440	
2051	004110	042440	050130	041505	
2052	004116	042524	020104	026524	
2053	004124	030461	051440	040524	
2054	004132	052122	051055	051505	
2055	004140	040524	052122	040440	
2056	004146	042104	042522	051523	
2057	004154	000			
2058		004156			.EVEN
2059					
2060					⋮
2061					⋮ FORMAT STATEMENTS USED IN PRINT CALLS
2062					⋮
2063					
2064	004156	040445	047503	052116	EMSGRO:::ASCIZ /%ACONTROL REG 0 ERROR%N/
2065	004164	047522	020114	042522	
2066	004172	020107	020060	051105	
2067	004200	047522	022522	000116	
2068	004206	040445	047503	052116	EMSGR2:::ASCIZ /%ACONTROL REG 2 ERROR%N/
2069	004214	047522	020114	042522	
2070	004222	020107	020062	051105	
2071	004230	047522	022522	000116	
2072	004236	040445	047503	052116	EMSGR4:::ASCIZ /%ACONTROL REG 4 ERROR%N/
2073	004244	047522	020114	042522	
2074	004252	020107	020064	051105	
2075	004260	047522	022522	000116	
2076	004266	040445	047503	052116	EMSGR6:::ASCIZ /%ACONTROL REG 6 ERROR%N/
2077	004274	047522	020114	042522	
2078	004302	020107	020066	051105	

2079	004310	047522	022522	000116	
2080	004316	040445	042522	030107	REG0EQ::ASCIZ /%AREG0 = /
2081	004324	036440	000040		
2082	004330	040445	042522	031107	REG2EQ::ASCIZ /%AREG2 = /
2083	004336	036440	000040		
2084	004342	040445	042522	032107	REG4EQ::ASCIZ /%AREG4 = /
2085	004350	036440	000040		
2086	004354	040445	042522	033107	REG6EQ::ASCIZ /%AREG6 = /
2087	004362	036440	000040		
2088	004366	040445	047514	042101	FRMTR0::ASCIZ /%ALOAD: %06%S1%AGOOD: %06%S1%ABAD: %06%N/
2089	004374	020072	047445	022466	
2090	004402	030523	040445	047507	
2091	004410	042117	020072	047445	
2092	004416	022466	030523	040445	
2093	004424	040502	035104	022440	
2094	004432	033117	047045	000	
2095	004437	045	046101	040517	FRMTR2::ASCIZ /%ALOAD: %06%S1%AREAD: %06%N/
2096	004444	035104	022440	033117	
2097	004452	051445	022461	051101	
2098	004460	040505	035104	022440	
2099	004466	033117	047045	000	
2100	004473	045	052101	046511	MSGTMO::ASCIZ /%ATIME OUT ERROR ADDRESSING CONTROL REG 0%N/
2101	004500	020105	052517	020124	
2102	004506	051105	047522	020122	
2103	004514	042101	051104	051505	
2104	004522	044523	043516	041440	
2105	004530	047117	051124	046117	
2106	004536	051040	043505	030040	
2107	004544	047045	000		
2108	004547	045	052101	046511	MSGTM2::ASCIZ /%ATIME OUT ERROR ADDRESSING CONTROL REG 2%N/
2109	004554	020105	052517	020124	
2110	004562	051105	047522	020122	
2111	004570	042101	051104	051505	
2112	004576	044523	043516	041440	
2113	004604	047117	051124	046117	
2114	004612	051040	043505	031040	
2115	004620	047045	000		
2116	004623	045	052101	046511	MSGTM4::ASCIZ /%ATIME OUT ERROR ADDRESSING CONTROL REG 4%N/
2117	004630	020105	052517	020124	
2118	004636	051105	047522	020122	
2119	004644	042101	051104	051505	
2120	004652	044523	043516	041440	
2121	004660	047117	051124	046117	
2122	004666	051040	043505	032040	
2123	004674	047045	000		
2124	004677	045	052101	046511	MSGTM6::ASCIZ /%ATIME OUT ERROR ADDRESSING CONTROL REG 6%N/
2125	004704	020105	052517	020124	
2126	004712	051105	047522	020122	
2127	004720	042101	051104	051505	
2128	004726	044523	043516	041440	
2129	004734	047117	051124	046117	
2130	004742	051040	043505	033040	
2131	004750	047045	000		
2132		004754			
2133					

.EVEN

2134
2135
2136
2137
2138
2139
2140
2141
2142
2143 004754
2144 004754
2145 004754 004537 005160
2146 004760 004156
2147 004762 004737 005230
2148 004766
2149 004766
2150 004766 104423
2151
2152 004770
2153 004770
2154 004770 004537 005160
2155 004774 004206
2156 004776 004737 005306
2157 005002
2158 005002
2159 005002 104423
2160
2161 005004
2162 005004
2163 005004 004537 005160
2164 005010 004236
2165 005012 004737 005360
2166 005016
2167 005016
2168 005016 104423
2169
2170 005020
2171 005020
2172 005020 004537 005160
2173 005024 004266
2174 005026 004737 005200
2175 005032
2176 005032
2177 005032 104423
2178
2179 005034
2180 005034
2181 005034 004537 005160
2182 005040 004266
2183 005042 004737 005212
2184 005046
2185 005046
2186 005046 104423
2187
2188 005050
2189 005050

.SBT'L GLOBAL ERROR REPORT SECTION

:++
: THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
: USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION. PRINTB
: (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
:--

ROEROR: BGNMSG ROEROR
JSR R5,PRNTBS ;GO PRINT CONTROL REG THAT FAILED
.WORD EMSGR0
JSR PC,PRNTR0 ;GO PRINT CONTROL REGISTER 0 INFO
ENDMSG
L10002: TRAP C\$MSG
R2EROR: BGNMSG R2EROR
JSR R5,PRNTBS ;GO PRINT CONTROL REG THAT FAILED
.WORD EMSGR2
JSR PC,PRNTR2 ;GO PRINT CONTROL REGISTER 2 INFO
ENDMSG
L10003: TRAP C\$MSG
R4EROR: BGNMSG R4EROR
JSR R5,PRNTBS ;GO PRINT CONTROL REG THAT FAILED
.WORD EMSGR4
JSR PC,PRNTR4 ;GO PRINT CONTROL REGISTER 4 INFO
ENDMSG
L10004: TRAP C\$MSG
R06ERR: BGNMSG R06ERR
JSR R5,PRNTBS ;GO PRINT CONTROL REG THAT FAILED
.WORD EMSGR6
JSR PC,PR06R ;GO PRINT CONTROL REG 0 AND 6 INFO
ENDMSG
L10005: TRAP C\$MSG
R026ER: BGNMSG R026ER
JSR R5,PRNTBS ;GO PRINT CONTROL REG THAT FAILED
.WORD EMSGR6
JSR PC,PR026R
ENDMSG
L10006: TRAP C\$MSG
ROTM: BGNMSG ROTM

2190	005050			PRINTB	#MSGTMO
2191	005050	012746	004473	MOV	#MSGTMO,-(SP)
2192	005054	012746	000001	MOV	#1,-(SP)
2193	005060	010600		MOV	SP,R0
2194	005062	104414		TRAP	C\$PNTB
2195	005064	062706	000004	ADD	#4,SP
2196	005070			ENDMSG	
2197	005070			L10007:	
2198	005070	104423		TRAP	C\$MSG
2199					
2200	005072			BGNMSG	R2TM
2201	005072			R2TM::	
2202	005072			PRINTB	#MSGTM2
2203	005072	012746	004547	MOV	#MSGTM2,-(SP)
2204	005076	012746	000001	MOV	#1,-(SP)
2205	005102	010600		MOV	SP,R0
2206	005104	104414		TRAP	C\$PNTB
2207	005106	062706	000004	ADD	#4,SP
2208	005112			ENDMSG	
2209	005112			L10010:	
2210	005112	104423		TRAP	C\$MSG
2211					
2212	005114			BGNMSG	R4TM
2213	005114			R4TM::	
2214	005114			PRINTB	#MSGTM4
2215	005114	012746	004623	MOV	#MSGTM4,-(SP)
2216	005120	012746	000001	MOV	#1,-(SP)
2217	005124	010600		MOV	SP,R0
2218	005126	104414		TRAP	C\$PNTB
2219	005130	062706	000004	ADD	#4,SP
2220	005134			ENDMSG	
2221	005134			L10011:	
2222	005134	104423		TRAP	C\$MSG
2223					
2224	005136			BGNMSG	R6TM
2225	005136			R6TM::	
2226	005136			PRINTB	#MSGTM6
2227	005136	012746	004677	MOV	#MSGTM6,-(SP)
2228	005142	012746	000001	MOV	#1,-(SP)
2229	005146	010600		MOV	SP,R0
2230	005150	104414		TRAP	C\$PNTB
2231	005152	062706	000004	ADD	#4,SP
2232	005156			ENDMSG	
2233	005156			L10012:	
2234	005156	104423		TRAP	C\$MSG
2235					
2236				:ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.	
2237					
2238	005160			PRNTBS::PRINTB	(R5)+
2239	005160	012546		MOV	(R5)+,-(SP)
2240	005162	012746	000001	MOV	#1,-(SP)
2241	005166	010600		MOV	SP,R0
2242	005170	104414		TRAP	C\$PNTB
2243	005172	062706	000004	ADD	#4,SP
2244	005176	000205		RTS	R5
2245					

GLOBAL ERROR REPORT SECTION

```

2246 ;ROUTINE TO PRINT CONTROL REGISTER 0 AND 6 ERROR INFORMATION
2247
2248 005200 004737 005230 PR06R:: JSR PC,PRNTR0
2249 005204 004737 005436 JSR PC,PRNTR6
2250 005210 000207 RTS PC
2251
2252 ;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
2253
2254 005212 004737 005230 PR026R::JSR PC,PRNTR0 ;GO PRINT CONTROL REGISTER 0 INFO
2255 005216 004737 005306 JSR PC,PRNTR2 ;GO PRINT CONTROL REGISTER 2 INFO
2256 005222 004737 005436 JSR PC,PRNTR6 ;GO PRINT CONTROL REGISTER 6 INFO
2257 005226 000207 RTS PC
2258
2259 ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2260
2261 005230 PRNTR0::PRINTX #REG0EQ
2262 005230 012746 004316 MOV #REG0EQ,-(SP)
2263 005234 012746 000001 MOV #1,-(SP)
2264 005240 010600 MOV SP,R0
2265 005242 104415 TRAP C$PNTX
2266 005244 062706 000004 ADD #4,SP
2267 005250 PRINTX #FRMTR0,R0LOAD,R0GOOD,R0BAD
2268 005250 013746 002326 MOV R0BAD,-(SP)
2269 005254 013746 002322 MOV R0GOOD,-(SP)
2270 005260 013746 002320 MOV R0LOAD,-(SP)
2271 005264 012746 004366 MOV #FRMTR0,-(SP)
2272 005270 012746 000004 MOV #4,-(SP)
2273 005274 010600 MOV SP,R0
2274 005276 104415 TRAP C$PNTX
2275 005300 062706 000012 ADD #12,SP
2276 005304 000207 RTS PC
2277
2278 ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2279
2280 005306 PRNTR2::PRINTX #REG2EQ
2281 005306 012746 004330 MOV #REG2EQ,-(SP)
2282 005312 012746 000001 MOV #1,-(SP)
2283 005316 010600 MOV SP,R0
2284 005320 104415 TRAP C$PNTX
2285 005322 062706 000004 ADD #4,SP
2286 005326 PRINTX #FRMTR2,R2LOAD,R2READ
2287 005326 013746 002332 MOV R2READ,-(SP)
2288 005332 013746 002330 MOV R2LOAD,-(SP)
2289 005336 012746 004437 MOV #FRMTR2,-(SP)
2290 005342 012746 000003 MOV #3,-(SP)
2291 005346 010600 MOV SP,R0
2292 005350 104415 TRAP C$PNTX
2293 005352 062706 000010 ADD #10,SP
2294 005356 000207 RTS PC
2295
2296 ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2297
2298 005360 PRNTR4::PRINTX #REG4EQ
2299 005360 012746 004342 MOV #REG4EQ,-(SP)
2300 005364 012746 000001 MOV #1,-(SP)
2301 005370 010600 MOV SP,R0

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GLOBAL ERROR REPORT SECTION

2302	005372	104415		TRAP	C\$PNTX
2303	005374	062706	000004	ADD	#4,SP
2304	005400			PRINTX	#FRMTR0,R4LOAD,R4GOOD,R4BAD
2305	005400	013746	002340	MOV	R4BAD,-(SP)
2306	005404	013746	002336	MOV	R4GOOD,-(SP)
2307	005410	013746	002334	MOV	R4LOAD,-(SP)
2308	005414	012746	004366	MOV	#FRMTR0,-(SP)
2309	005420	012746	000004	MOV	#4,-(SP)
2310	005424	010600		MOV	SP,R0
2311	005426	104415		TRAP	C\$PNTX
2312	005430	062706	000012	ADD	#12,SP
2313	005434	000207		RTS	PC
2314					
2315					
2316					
2317	005436				
2318	005436	012746	004354	PRNTR6::PRINTX	#REG6EQ
2319	005442	012746	000001	MOV	#REG6EQ,-(SP)
2320	005446	010600		MOV	#1,-(SP)
2321	005450	104415		MOV	SP,R0
2322	005452	062706	000004	TRAP	C\$PNTX
2323	005456			ADD	#4,SP
2324	005456	013746	002344	PRINTX	#FRMTR2,R6LOAD,R6READ
2325	005462	013746	002342	MOV	R6READ,-(SP)
2326	005466	012746	004437	MOV	R6LOAD,-(SP)
2327	005472	012746	000003	MOV	#FRMTR2,-(SP)
2328	005476	010600		MOV	#3,-(SP)
2329	005500	104415		MOV	SP,R0
2330	005502	062706	000010	TRAP	C\$PNTX
2331	005506	000207		ADD	#10,SP
2332				RTS	PC

```

2333      .SBTTL  GLOBAL SUBROUTINES SECTION
2334
2335      :++
2336      : THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
2337      : THAT ARE USED IN MORE THAN ONE TEST.
2338      :--
2339
2340      :++
2341      : FUNCTIONAL DESCRIPTION:
2342      :   SUBROUTINE TO....SELECT AND INITIALIZE TARGET EMULATOR
2343
2344      : INPUTS:
2345      :   LOCATION IDDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8
2346      :   LOCATION IDTYPE CONTAINS TARGET EMULATOR DEVICE TYPE AND GDAL BIT 15
2347
2348
2349
2350      : IMPLICIT INPUTS:
2351
2352
2353      : OUTPUTS:
2354      :   R0LOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
2355      :   R2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED
2356      :   R4LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 4 WAS CLEARED
2357      :   R6LOAD CONTAINS ALL ZEROES TO INDICATE MODE REGISTER WAS CLEARED
2358      :
2359      :   ROMASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 0 BITS
2360      :   R6MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 6 BITS
2361
2362
2363      : IMPLICIT OUTPUTS:
2364
2365
2366      : SUBORDINATE ROUTINES USED:
2367      :   LDRDR0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
2368      :   LDRDR2 ROUTINE TO LOAD, READ AND COMPARE REGISTER 2 (USED FOR DEVICE TYPE)
2369      :   LDRDR4 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 4
2370      :   LDRDR6 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 6
2371
2372
2373
2374      : FUNCTIONAL SIDE EFFECTS:
2375      :   TARGET EMULATOR SELECTED
2376      :   CONTROL REGISTER 0 LOW BYTE EQUALS 0 (GDAL 7:0)
2377      :   CONTROL REGISTER 2 EQUALS 0 (ADAL 15:0)
2378      :   CONTROL REGISTER 4 LOW BYTE EQUALS 0 (VDAL 15:0)
2379      :   CONTROL REGISTER 6 - HDAL 15:0 REGISTER EQUALS FOUR
2380      :   CONTROL REGISTER 6 - MODE REGISTER 15:0 EQUALS ZERO
2381
2382
2383      : CALLING SEQUENCE:
2384      :   JSR PC,INITTE
2385
2386      :--
2387
2388

```



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2389                                     ;NOTE: ON A START OR RESTART COMMAND TO THE DIAGNOSTIC SUPERVISOR, A
2390                                     ; BUS RESET INSTRUCTION WILL BE ISSUED TO CLEAR ALL MODULES. THIS
2391                                     ; IS NEEDED TO CLEAR SIGNALS COMING INTO THE TARGET EMULATOR THAT
2392                                     ; MAY BE SET ON THE MEMORY SIMULATOR MODULE OR STATE ANALYZER MODULE.
2393
2394
2395
2396 005510                               INITTE:::BGNSEG                               ;ROUTINE TO INIT TE MODULE
2397 005510 104404                         TRAP          C$BSEG
2398 005512                               SETVEC        #4,#1$,#PRI07           ;SETUP VECTOR
2399 005512 012746 000340                   MOV          #PRI07,-(SP)
2400 005516 012746 005630                   MOV          #1$,-(SP)
2401 005522 012746 000004                   MOV          #4,-(SP)
2402 005526 012746 000003                   MOV          #3,-(SP)
2403 005532 104437                           TRAP          C$SVEC
2404 005534 062706 000010                   ADD          #10,SP
2405
2406                                     ;LOAD DEVICE NUMBER INTO REGISTER 0 AND CHECK IT
2407
2408 005540 012737 000300 002324             MOV          #SSBRK!TOBRK,ROMASK      ;SETUP TO IGNORE TE BREAK SIGNALS
2409 005546 013737 002310 002320             MOV          IDDEV,ROLOAD             ;GET USER DEFINED DEVICE NUMBER
2410 005554 013737 002320 002322             MOV          ROLOAD,ROGOOD           ;PUT DATA LOADED INTO EXPECTED
2411 005562 013777 002320 174510             MOV          ROLOAD,@REGO            ;WRITE WORD TO REGISTER 0
2412 005570 017737 174504 002326             MOV          @REGO,ROBAD             ;READ REGISTER CONTENTS BACK
2413 005576 043737 002324 002326             BIC          ROMASK,ROBAD           ;CLEAR OUT UNWANTED BITS
2414 005604 023737 002322 002326             CMP          ROGOOD,ROBAD           ;COMPARE EXPECTED WITH THAT READ
2415 005612 001414                           BEQ          2$                      ;IF COMPARE WAS GOOD THEN CONT
2416 005614                               ERRDF        1,GDALRG,ROEROR         ;DEVICE # OR LB NOT = EXPECTED
2417 005614 104455                         TRAP          C$ERDF
2418 005616 000001                           .WORD        1
2419 005620 002406                           .WORD        GDALRG
2420 005622 004754                           .WORD        ROEROR
2421 005624                               CKLOOP
2422 005624 104406                         TRAP          C$CLP1
2423 005626 000406                         BR           2$                      ;BRANCH AROUND TIME OUT ERROR
2424 005630 005726 1$:                    TST          (SP)+                  ;CLEAN UP STACK
2425 005632 005726                        TST          (SP)+                  ;CLEAN UP STACK
2426 005634                               ERRDF        1,ROTM                 ;TIME OUT ERPOR REG 0
2427 005634 104455                         TRAP          C$ERDF
2428 005636 000001                           .WORD        1
2429 005640 000000                           .WORD        0
2430 005642 005050                           .WORD        ROTM
2431 005644                               2$:                    CLRVEC        #4                      ;CLEAR VECTOR
2432 005644 012700 000004                   MOV          #4,RO
2433 005650 104436                         TRAP          C$CVEC
2434 005652                               ENDSEG
2435 005652                               10000$:
2436 005652 104405                         TRAP          C$ESEG
2437
2438                                     ;READ DEVICE TYPE IN REGISTER 0 - DEVICE TYPE SHOULD EQUAL 0
2439
2440 005654                               BGNSEG
2441 005654 104404                         TRAP          C$BSEG
2442 005656 052737 100000 002320             BIS          #GDAL15,ROLOAD          ;SETUP TO READ DEVICE TYPE
2443 005664 013737 002316 002322             MOV          IDTYPE,ROGOOD          ;SETUP EXPECTED DATA
2444 005672 004737 006562                   JSR          PC,LDRDOR              ;LOAD, READ AND COMPARE REG 0

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2445 005676 001404          BEQ      3$                ;IF EQUAL THEN DEVICE TYPE COMPARED
2446 005700                  ERRDF    1,GDALRG,ROEROR  ;DEVICE TYPE NOT EQUAL EXPECTED
2447 005700 104455          TRAP    C$ERDF
2448 005702 000001          .WORD   1
2449 005704 002406          .WORD   GDALRG
2450 005706 004754          .WORD   ROEROR
2451 005710                  3$:
2452 005710                  10001$:
2453 005710 104405          TRAP    C$ESEG
2454
2455
2456
2457
2458
2459 005712                  BGNSEG
2460 005712 104404          TRAP    C$BSEG
2461 005714 013737 002310 002320  MOV     IDDEV,ROLOAD      ;GET USER DEFINED DEVICE NUMBER
2462 005722 052737 000003 002320  BIS     #GDAL1!GDALO,ROLOAD ;SET BITS TO SELECT THE HDAL REGISTER
2463 005730 004737 006554          JSR     PC,LDRDPO        ;GO LOAD, READ AND CHECK GDAL REGISTER
2464 005734 001405          BEQ     4$                ;IF LOADED OK THEN CONTINUE
2465 005736                  ERRDF    1,GDALRG,ROEROR  ;GDAL REGISTER NOT EQUAL TO EXPECTED
2466 005736 104455          TRAP    C$ERDF
2467 005740 000001          .WORD   1
2468 005742 002406          .WORD   GDALRG
2469 005744 004754          .WORD   ROEROR
2470 005746
2471 005746 104406          CKLOOP
2472
2473
2474
2475
2476
2477
2478
2479
2480
2481
2482 005750                  4$:
2483 005750 012746 000340          SETVEC  #4,#5$,#PRI07    ;SETUP VECTOR
2484 005754 012746 006056          MOV     #PRI07,-(SP)
2485 005760 012746 000004          MOV     #5$,-(SP)
2486 005764 012746 000003          MOV     #4,-(SP)
2487 005770 104437          MOV     #3,-(SP)
2488 005772 062706 000010          TRAP    C$SVEC
2489 005776 012737 000004 002342  ADD     #10,SP
2490 006004 005037 002346          MOV     #HDAL2,R6LOAD    ;SETUP BIT TO BE LOADED
2491 006010 013777 002342 174270  CLR     R6MASK           ;SETUP MASK WORK TO COMPARE ALL BITS
2492 006016 017737 174264 002344  MOV     @R6LOAD,@REG6    ;WRITE WORD INTO REG 6
2493 006024 043737 002346 002344  MOV     @REG6,R6READ     ;READ THE WORD BACK
2494 006032 023737 002342 002344  BIC     R6MASK,R6READ    ;CLEAR OUT ANY UNWANTED BITS
2495 006040 001414          CMP     R6LOAD,R6READ    ;COMPARE DATA LOADED WITH DATA READ
2496 006042                  BEQ     6$                ;IF COMPARE WAS GOOD THEN CONT
2497 006042 104455          ERRDF    4,HDALRG,RO6ERR ;HDAL REGISTER NOT EQUAL TO EXPECTED
2498 006044 000004          TRAP    C$ERDF
2499 006046 002605          .WORD   4
2500 006050 005020          .WORD   HDALRG
                .WORD   RO6ERR

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2501 006052          CKLOOP
2502 006052 104406   TRAP   C$CLP1
2503 006054 000406   BR     6$          ;BRANCH AROUND TIME OUT ERROR
2504 006056 005726   5$:   TST   (SP)+      ;CLEAN UP STACK
2505 006060 005726   TST   (SP)+      ;CLEAN UP STACK
2506 006062          ERRDF  4,R6TM     ;TIME OUT ERROR REG 6
2507 006062 104455   TRAP   C$ERDF
2508 006064 000004   .WORD  4
2509 006066 000000   .WORD  0
2510 006070 005136   .WORD  R6TM
2511 006072          6$:   CLRVEC #4          ;CLEAR VECTOR
2512 006072 012700 000004 MOV   #4,R0
2513 006076 104436   TRAP   C$CVEC
2514 006100          ENDSEG
2515 006100          10002$:
2516 006100 104405   TRAP   C$ESEG
2517
2518          ;SELECT THE MODE REGISTER BY SETTING GDAL BIT 2 TO A ONE AND GDAL BITS
2519          ;1 AND 0 TO ZEROES. THIS IS DONE SO THAT THE MODE REGISTER CAN BE
2520          ;SELECTED AND CLEARED.
2521
2522 006102          BGNSEG
2523 006102 104404   TRAP   C$BSEG
2524 006104 013737 002310 002320 MOV   IDDEV,ROLOAD ;GET USER DEFINED DEVICE NUMBER
2525 006112 052737 000004 002320 BIS   #GDAL2,ROLOAD ;GET BIT TO SELECT MODE REGISTER
2526 006120 004737 006554 JSR   PC,LDRDRO    ;GO LOAD, READ AND CHECK MODE REGISTER
2527 006124 001405   BEQ   7$          ;IF LOADED OK THEN CONTINUE
2528 006126          ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
2529 006126 104455   TRAP   C$ERDF
2530 006130 000001   .WORD  1
2531 006132 002406   .WORD  GDALRG
2532 006134 004754   .WORD  ROEROR
2533 006136          CKLOOP
2534 006136 104406   TRAP   C$CLP1
2535
2536          ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
2537          ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BIT 2 SET TO A ONE
2538          ;AND GDAL BITS 1 AND 0 SET TO ZEROES, PULSES WILL OCCUR ON THE SIGNALS
2539          ;WPT4 LB H AND WPT4 HB H. THESE PULSES WILL LOAD THE DATA ON THE WRITE
2540          ;COMMAND INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6,
2541          ;DATA WILL BE READBACK FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.
2542
2543 006140 005037 002342 7$:   CLR   R6LOAD      ;SETUP TO LOAD ALL ZEROES INTO MODE REG
2544 006144 004737 006672 JSR   PC,LDRDR6   ;GO LOAD, READ AND CHECK MODE REGISTER
2545 006150 001404   BEQ   8$          ;IF LOADED OK THEN CONTINUE
2546 006152          ERRDF  4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL EXPECTED
2547 006152 104455   TRAP   C$ERDF
2548 006154 000004   .WORD  4
2549 006156 002631   .WORD  MODREG
2550 006160 005020   .WORD  R06ERR
2551 006162          8$:   ENDSEG
2552 006162          10003$:
2553 006162 104405   TRAP   C$ESEG
2554
2555 006164          BGNSEG
2556 006164 104404   TRAP   C$BSEG

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2566
2567 006166          SETVEC #4,#9$,#PRI07          ;SETUP VECTOR
2568 006166 012746 000340      MOV #PRI07,-(SP)
2569 006172 012746 006262      MOV #9$,-(SP)
2570 006176 012746 000004      MOV #4,-(SP)
2571 006202 012746 000003      MOV #3,-(SP)
2572 006206 104437          TRAP C$SVEC
2573 006210 062706 000010      ADD #10,SP
2574 006214 012737 000001 002330  MOV #ADALO,R2LOAD          ;SETUP BIT TO BE LOADED TO 0 SSBK F/F
2575 006222 013777 002330 174052  MOV R2LOAD,@REG2          ;WRITE BITS INTO REGISTER 2
2576 006230 017737 174046 002332  MOV @REG2,R2READ          ;READ REGISTER 2 BACK
2577 006236 023737 002330 002332  CMP R2LOAD,R2READ          ;CHECK IF EXP EQUALS ACTUAL
2578 006244 001415          BEQ 10$                    ;IF COMPARE WAS GOOD THEN CONT
2579 006246          ERRDF 2,ADALRG,R2EROR          ;REG 2 NOT EQUAL TO ADAL 0
2580 006246 104455          TRAP C$ERDF
2581 006250 000002          .WORD 2
2582 006252 002513          .WORD ADALRG
2583 006254 004770          .WORD R2EROR
2584 006256          CKLOOP
2585 006256 104406          TRAP C$CLP1
2586 006260 000407          BR 10$                    ;BRANCH AROUND TIME OUT ERROR
2587 006262 005726          9$: TST (SP)+                ;CLEAN UP STACK
2588 006264 005726          TST (SP)+                ;CLEAN UP STACK
2589 006266          ERRDF 2,,R2TM          ;TIME OUT ERROR REG 2
2590 006266 104455          TRAP C$ERDF
2591 006270 000002          .WORD 2
2592 006272 000000          .WORD 0
2593 006274 005072          .WORD R2TM
2594 006276          CKLOOP
2595 006276 104406          TRAP C$CLP1
2596 006300          10$: CLPVEC #4                ;CLEAR VECTOR
2597 006300 012700 000004      MOV #4,R0
2598 006304 104436          TRAP C$CVEC
2599 006306 005037 002330      CLR R2LOAD                ;SETUP TO CLEAR ADALO
2600 006312 004737 006614      JSR PC,LDRDR2            ;GO LOAD, READ AND CHECK REGISTER 2
2601 006316 001405          BEQ 11$                    ;IF LOADED OK THEN CONTINUE
2602 006320          ERRDF 2,ADALRG,R2EROR          ;REGISTER 2 NOT EQUAL EXPECTED
2603 006320 104455          TRAP C$ERDF
2604 006322 000002          .WORD 2
2605 006324 002513          .WORD ADALRG
2606 006326 004770          .WORD R2EROR
2607 006330          CKLOOP
2608 006330 104406          TRAP C$CLP1
2609
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;LOAD, READ AND CHECK CONTROL REGISTER 0. CHECK THE TIMEOUT BREAK AND
;THE SINGLE STEP BREAK FLIP-FLOPS TO BE CLEARED AS A RESULT OF ADALO H
;BEING SET AND CLEARED IN THE PREVIOUS CHECK.

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2613
2614 006332 005037 002324      11$: CLR      ROMASK      ;CLEAR MASK TO CHECK ALL BITS IN REG 0
2615 006336 105037 002320      CLRB     ROLOAD      ;SETUP TO CLEAR THE LOWER BYTE
2616 006342 004737 006554      JSR      PC,LDRDR0   ;GO LOAD, READ AND CHECK GDAL REGISTER
2617 006346 001404      BEQ      12$         ;IF ALL BITS CHECKED THEN CONTINUE
2618 006350      ERRDF    1,GDALRG,ROEROR ;REGISTER 0 NOT EQUAL TO DEVICE NUMBER
2619 006350 104455      TRAP     C$ERDF
2620 006352 000001      .WORD    1
2621 006354 002406      .WORD    GDALRG
2622 006356 004754      .WORD    ROEROR
2623 006360      12$: ENDSEG
2624 006360      10004$:
2625 006360 104405      TRAP     C$ESEG
2626
2627 006362      BGNSEG
2628 006362 104404      TRAP     C$BSEG
2629
2630      ;SET AND CLEAR VDAL2 IN CONTROL REGISTER 4. WHEN VDAL2 IS SET TO A
2631      ;ONE, THE PAUSE STATE MACHINE FLIP-FLOPS WILL BE CLEARED. THESE F/F'S
2632      ;ARE READBACK IN VDAL REGISTER BITS 15:8. THE REMAINING VDAL READ/
2633      ;WRITE BITS WILL BE LOADED AND CHECKED FOR ZEORES.
2634
2635 006364      SETVEC  #4,#13$,#PRI07 ;SETUP VECTOR
2636 006364 012746 000340      MOV      #PRI07,-(SP)
2637 006370 012746 006466      MOV      #13$,-(SP)
2638 006374 012746 000004      MOV      #4,-(SP)
2639 006400 012746 000003      MOV      #3,-(SP)
2640 006404 104437      TRAP     C$SVEC
2641 006406 062706 000010      ADD      #10,SP
2642 006412 012737 000004 002334      MOV      #VDAL2,R4LOAD ;SETUP BIT TO BE LOADED
2643 006420 013737 002334 002336      MOV      R4LOAD,R4GOOD ;SETUP EXPECTED DATA
2644 006426 013777 002334 173650      MOV      R4LOAD,@REG4  ;WRITE WORD INTO REGISTER 4
2645 006434 017737 173644 002340      MOV      @REG4,R4BAD   ;READ WORD BACK FROM REGISTER 4
2646 006442 023737 002336 002340      CMP      R4GOOD,R4BAD  ;COMPARE WORD EXPECTED WITH READ
2647 006450 001415      BEQ      14$         ;IF LOADED OK THEN CONT
2648 006452      ERRDF    3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL TO 2
2649 006452 104455      TRAP     C$ERDF
2650 006454 000003      .WORD    3
2651 006456 002537      .WORD    VDALRG
2652 006460 005004      .WORD    R4EROR
2653 006462      CKLOOP
2654 006462 104406      TRAP     C$CLP1
2655 006464 000407      BR       14$         ;BRANCH AROUND TIME OUT ERROR
2656

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2685
2686 ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 0
2687 ;CONDITION CODES ARE SET ON EXIT AS RESULT OF THE "CMP" INSTRUCTION.
2688
2689 006554 013737 002320 002322 LDRDR0::MOV R0LOAD,ROGOOD ;PUT DATA LOADED INTO EXPECTED
2690 006562 013777 002320 173510 LDRDR0::MOV R0LOAD,@REG0 ;WRITE WORD TO REGISTER 0
2691 006570 017737 173504 002326 READR0::MOV @REG0,ROBAD ;READ REGISTER CONTENTS BACK
2692 006576 043737 002324 002326 BIC ROMASK,ROBAD ;CLEAR OUT UNWANTED BITS
2693 006604 023737 002322 002326 CMP R0GOOD,ROBAD ;COMPARE EXPECTED WITH THAT READ
2694 006612 000207 RTS PC ;EXIT WITH CONDITION CODES SET
2695
2696 ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 2.
2697 ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION
2698
2699 006614 013777 002330 173460 LDRDR2::MOV R2LOAD,@REG2 ;WRITE BITS INTO REGISTER 2
2700 006622 017737 173454 002332 READR2::MOV @REG2,R2READ ;READ REGISTER 2 BACK
2701 006630 023737 002330 002332 CMP R2LOAD,R2READ ;CHECK IF EXP EQUALS ACTUAL
2702 006636 000207 RTS PC ;EXIT WITH CONDITION CODES SET
2703
2704 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF REGISTER 4.
2705 ;CONDITION CODES ARE SET ON EXET AS RESULT OF "CMP" INSTRUCTION.
2706
2707 006640 013737 002334 002336 LDRDR4::MOV R4LOAD,R4GOOD ;SETUP EXPECTED DATA
2708 006646 013777 002334 173430 LDRDR4::MOV R4LOAD,@REG4 ;WRITE WORD INTO REGISTER 4
2709 006654 017737 173424 002340 READR4::MOV @REG4,R4BAD ;READ WORD BACK FROM REGISTER 4
2710 006662 023737 002336 002340 CMP R4GOOD,R4BAD ;COMPARE WORD EXPECTED WITH READ
2711 006670 000207 RTS PC ;RETURN WITH CONDITION CODES SET
2712
2713 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF CONTROL REGISTER 6
2714 ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
2715
2716 006672 013777 002342 173406 LDRDR6::MOV R6LOAD,@REG6 ;WRITE WORD INTO REGISTER 6
2717 006700 017737 173402 002344 READR6::MOV @REG6,R6READ ;READ THE WORD BACK
2718 006706 043737 002346 002344 BIC R6MASK,R6READ ;CLEAR OUT ANY UNWANTED BITS
2719 006714 023737 002342 002344 CMP R6LOAD,R6READ ;COMPARE DATA LOADED WITH DATA READ
2720 006722 000207 RTS PC ;EXIT WITH CONDITION CODES SET
2721
2722 ;TARGET EMULATOR INTERRUPT SERVICE ROUTINE
2723
2724 006724 BGNSRV INTSRV
2725 006724 INTSRV::
2726 006724 017737 173350 002326 MOV @REG0,ROBAD ;READ GDAL REGISTER AND SAVE
2727 006732 012702 177777 MOV #-1,R2 ;SET SOFTWARE INTERRUPT FLAG
2728 006736 ENDSRV #PRI07
2729 006736
2730 006736 142766 000340 000002 L10013: BICB #340,2(SP)
2731 006744 152766 000340 000002 BISB #PRI07,2(SP)
2732 006752 000002 RTI
2733

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GLOBAL SUBROUTINES SECTION

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2734 ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO
2735 ;SELECT THE HDAL REGISTER. THE HDAL REGISTER WILL BE SELECTED BY EITHER
2736 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT2 EQUALS A 0
2737 ;AND GDAL BIT 1 AND GDAL BIT 0 EQUAL A ONE.
2738
2739 006754 SLHDAL: :BGNSEG
2740 006754 104404 TRAP C$BSEG
2741 006756 112737 000003 002320 MOVB #GDAL1!GDALO,ROLOAD ;SETUP BITS TO BE SELECTED
2742 006764 004737 006554 JSR PC,LDRDRO ;GO LOAD, READ AND CHECK GDAL REG
2743 006770 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
2744 006772 ERRDF 1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
2745 006772 104455 TRAP C$ERDF
2746 006774 000001 .WORD 1
2747 006776 002406 .WORD GDALRG
2748 007000 004754 .WORD ROEROR
2749 007002 1$: ENDSEG
2750 007002 10000$:
2751 007002 104405 TRAP C$ESEG
2752 007004 000207 RTS PC ;RETURN BACK TO TEST
2753
2754 ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO
2755 ;SELECT THE MODE REGISTER. THE MODE REGISTER WILL BE SELECTED BY EITHER
2756 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT 2 EQUALS A ONE
2757 ;AND GDAL BIT 1 AND GDAL BIT 0 EQUALS A ZERO.
2758
2759 007006 SLMODR: :BGNSEG
2760 007006 104404 TRAP C$BSEG
2761 007010 112737 000004 002320 MOVB #GDAL2,ROLOAD ;SETUP BITS TO SELECT MODE REGISTER
2762 007016 004737 006554 JSR PC,LDRDRO ;GO LOAD, READ AND CHECK GDAL REGISTER
2763 007022 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
2764 007024 ERRDF 1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
2765 007024 104455 TRAP C$ERDF
2766 007026 000001 .WORD 1
2767 007030 002406 .WORD GDALRG
2768 007032 004754 .WORD ROEROR
2769 007034 1$: ENDSEG
2770 007034 10001$:
2771 007034 104405 TRAP C$ESEG
2772 007036 000207 RTS PC ;RETURN BACK TO TEST
2773
2774 ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO SELECT
2775 ;THE ADDRESS BUS TO BE READBACK VIA THE SIGNAL RPT1 L WHEN A READ COMMAND IS
2776 ;ISSUED TO CONTROL REGISTER 6. ON A WRITE COMMAND TO CONTROL REGISTER 6, THE
2777 ;NEW FORCE JUMP ADDRESS REG WILL BE LOADED WITH LSI-11 Q-BUS DATA BY THE SIGNALS
2778 ;WPT1 LB H AND WPT1 HB H. SELECT POINTER ONE BY SETTING GDALO H TO A ONE AND
2779 ;GDAL1 H AND GDAL2 H TO A ZERO.
2780
2781 007040 SLFJAR: :BGNSEG
2782 007040 104404 TRAP C$BSEG
2783 007042 112737 000001 002320 MOVB #GDALO,ROLOAD ;SETUP TO SET GDALO H TO A ONE
2784 007050 004737 006554 JSR PC,LDRDRO ;GO LOAD, READ AND CHECK GDAL REGISTER
2785 007054 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
2786 007056 ERRDF 1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
2787 007056 104455 TRAP C$ERDF
2788 007060 000001 .WORD 1
2789 007062 002406 .WORD GDALRG

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2790 007064 004754
2791 007066
2792 007066
2793 007066 104405
2794 007070 000207
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2800
2801 007072
2802 007072 104404
2803 007074 105037 002320
2804 007100 004737 006554
2805 007104 001404
2806 007106
2807 007106 104455
2808 007110 000001
2809 007112 002406
2810 007114 004754
2811 007116
2812 007116
2813 007116 104405
2814 007120 000207
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2821 007122
2822 007122 104404
2823 007124 112737 000007 002320
2824 007132 004737 006554
2825 007136 001404
2826 007140
2827 007140 104455
2828 007142 000001
2829 007144 002406
2830 007146 004754
2831 007150
2832 007150
2833 007150 104405
2834 007152 000207
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2841 007154
2842 007154 104404
2843 007156 112737 000002 002320
2844 007164 004737 006554
2845 007170 001404

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        .WORD    ROEROR
1$:      ENDSEG
10002$:
        TRAP     C$ESEG
        RTS      PC
;RETURN BACK TO TEST

;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO SELECT
;THE DIAGNOSTIC ADDRESS REGISTER. THE DIAGNOSTIC ADDRESS REGISTER WILL BE
;SELECTED BY EITHER A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL
;BITS 2:0 ARE EQUAL TO A ZERO.

SLDADR::BGNSEG
        TRAP     C$BSEG
        CLR      ROLOAD
        JSR      PC,LDRDRO
        BEQ      1$
        ERRDF    1,GDALRG,ROEROR
        TRAP     C$ERDF
        .WORD    1
        .WORD    GDALRG
        .WORD    ROEROR
1$:      ENDSEG
10003$:
        TRAP     C$ESEG
        RTS      PC
;RETURN BACK TO TEST

;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0
;TO SELECT THE EODAL 15:0 BUS TO BE READBACK TO THE LSI-11 BUS WHEN
;A READ COMMAND IS ISSUED TO CONTROL REGISTER 6. CONTROL REGISTER 0
;GDAL BITS 2:0 WILL BE SET TO ONES TO SELECT THE EODAL BUS READBACK.

SEODAL::BGNSEG
        TRAP     C$BSEG
        MOV      #GDAL2!GDAL1!GDAL0,ROLOAD
        JSR      PC,LDRDRO
        BEQ      1$
        ERRDF    1,GDALRG,ROEROR
        TRAP     C$ERDF
        .WORD    1
        .WORD    GDALRG
        .WORD    ROEROR
1$:      ENDSEG
10004$:
        TRAP     C$ESEG
        RTS      PC

;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
;FDAL REGISTER. THE FDAL REGISTER WILL BE SELECTED BY EITHER A READ OR WRITE
;COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT 1 IS SET TO A ONE AND GDAL BITS
;2 AND 0 ARE SET TO ZEROES.

SLFDAL::BGNSEG
        TRAP     C$BSEG
        MOV      #GDAL1,ROLOAD
        JSR      PC,LDRDRO
        BEQ      1$
;SETUP TO SET GDAL1 H TO A ONE
;GO LOAD, READ AND CHECK GDAL REGISTER
;IF LOADED OK THEN CONTINUE

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2846 007172          ERRDF  1,GDALRG,ROEROR          ;GDAL REGISTER NOT EQUAL EXPECTED
2847 007172 104455   TRAP    C$ERDF
2848 007174 000001   .WORD  1
2849 007176 002406   .WORD  GDALRG
2850 007200 004754   .WORD  ROEROR
2851 007202          1$:    ENDSEG
2852 007202          10005$:
2853 007202 104405   TRAP    C$ESEG
2854 007204 000207   RTS     PC
2855
2856                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
2857                ;TARGET MODE REGISTER. THE TARGET MODE REGISTER WILL BE SELECTED ON A READ
2858                ;COMMAND TO CONTROL REGISTER 6 WHEN GDAL BITS 2 AND 0 ARE SET AND GDAL BIT1
2859                ;IS CLEARED.
2860
2861 007206          SELTMR::BGNSEG
2862 007206 104404   TRAP    C$BSEG
2863 007210 112737 000005 002320  MOVB   #GDAL2!GDAL0,ROLOAD          ;SETUP BITS TO BE LOADED
2864 007216 004737 006554          JSR    PC,LDRDRO          ;GO LOAD, READ AND CHECK GDAL REGISTER
2865 007222 001404          BEQ    1$                ;IF LOADED OK THEN CONTINUE
2866 007224          ERRDF  1,GDALRG,ROEROR          ;GDAL REGISTER NOT EQUAL EXPECTED
2867 007224 104455   TRAP    C$ERDF
2868 007226 000001   .WORD  1
2869 007230 002406   .WORD  GDALRG
2870 007232 004754   .WORD  ROEROR
2871 007234          1$:    ENDSEG
2872 007234          10006$:
2873 007234 104405   TRAP    C$ESEG
2874 007236 000207   RTS     PC
2875
2876                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
2877                ;EIDAL BUS TO BE READBACK. THE EIDAL BUS WILL BE SELECTED ON A READ COMMAND
2878                ;TO CONTROL REGISTER 6 WHEN GDAL BITS 2 AND 1 ARE SET TO ONES AND GDAL BIT 0
2879                ;IS A ZERO.
2880
2881 007240          SEIDAL::BGNSEG
2882 007240 104404   TRAP    C$BSEG
2883 007242 112737 000006 002320  MOVB   #GDAL2!GDAL1,ROLOAD          ;SETUP BITS TO BE LOADED
2884 007250 004737 006554          JSR    PC,LDRDRO          ;GO LOAD, READ AND CHECK GDAL REGISTER
2885 007254 001404          BEQ    1$                ;IF LOADED OK THEN CONTINUE
2886 007256          ERRDF  1,GDALRG,ROEROR          ;GDAL REGISTER NOT EQUAL EXPECTED
2887 007256 104455   TRAP    C$ERDF
2888 007260 000001   .WORD  1
2889 007262 002406   .WORD  GDALRG
2890 007264 004754   .WORD  ROEROR
2891 007266          1$:    ENDSEG
2892 007266          10007$:
2893 007266 104405   TRAP    C$ESEG
2894 007270 000207   RTS     PC

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2895
2896 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL12 IN THE HDAL REGISTER. HDAL12
2897 ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS 'XNAS L' AND
2898 ;'XNAS H'. HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
2899 ;THE T-11 TIMING AND CONTROL SIGNALS.
2900
2901 007272 004737 007304 XNAS:: JSR PC,XRASH ;GO SET XNAS H (HIGH) AND XNAS L (LOW)
2902 007276 004737 007336 JSR PC,XRASL ;GO SET XNAS H (LOW) AND XNAS L (HIGH)
2903 007302 000207 RTS PC ;RETURN BACK TO TEST
2904
2905 ;THE FOLLOWING ROUTINE WILL SET HDAL12 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
2906 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
2907 ;HDAL12 H ON A ONE WILL CAUSE THE SIGNAL XNAS H TO BE ASSERTED HIGH AND THE
2908 ;SIGNAL XNAS L TO BE ASSERTED LOW
2909
2910 007304 XRASH:: BGNSEG
2911 007304 104404 TRAP C$BSEG
2912 007306 052737 010004 002342 BIS #HDAL12,HDAL2,R6LOAD ;SETUP BIT TO BE LOADED
2913 007314 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
2914 007320 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
2915 007322 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
2916 007322 104455 TRAP C$ERDF
2917 007324 000004 .WORD 4
2918 007326 002605 .WORD HDALRG
2919 007330 005020 .WORD R06ERR
2920 007332 1$: ENDSEG
2921 007332 10010$:
2922 007332 104405 TRAP C$ESEG
2923 007334 000207 RTS PC ;RETURN BACK TO TEST
2924
2925 ;THE FOLLOWING ROUTINE WILL SET HDAL12 H TO A ZFRO AND HDAL2 H TO A ONE.
2926 ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
2927 ;CONTROL SIGNALS. HDAL12 H ON A ZERO WILL CAUSE THE SIGNAL XNAS H TO BE
2928 ;ASSERTED LOW AND THE SIGNAL XNAS L TO BE ASSERTED HIGH.
2929
2930 007336 XRASL:: BGNSEG
2931 007336 104404 TRAP C$BSEG
2932 007340 052737 000004 002342 BIS #HDAL2,R6LOAD ;SETUP DIAGNOSTIC CONTROL BIT
2933 007346 042737 010000 002342 BIC #HDAL12,R6LOAD ;SETUP BIT TO BE CLEARED
2934 007354 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
2935 007360 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
2936 007362 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
2937 007362 104455 TRAP C$ERDF
2938 007364 000004 .WORD 4
2939 007366 002605 .WORD HDALRG
2940 007370 005020 .WORD R06ERR
2941 007372 1$: ENDSEG
2942 007372 10011$:
2943 007372 104405 TRAP C$ESEG
2944 007374 000207 RTS PC ;RETURN BACK TO TEST
2945
2946 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL13 IN THE HDAL REGISTER. HDAL13
2947 ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS 'XCAS L' AND
2948 ;'XCAS H'. HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
2949 ;THE T-11 TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
2950

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2951
2952 007376 004737 007410      XCAS:: JSR      PC,XCASH      ;GO SET XCAS H (HIGH) AND XCAS L (LOW)
2953 007402 004737 007442      JSR      PC,XCASL      ;GO SET XCAS H (LOW) AND XCAS L (HIGH)
2954 007406 000207      RTS      PC
2955
2956      ;THE FOLLOWING ROUTINE WILL SET HDAL13 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
2957      ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL13 H
2958      ;ON A ONE WILL CAUSE THE SIGNAL XCAS H TO BE ASSERTED HIGH AND THE SIGNAL XCAS L
2959      ;TO BE ASSERTED LOW.
2960
2961 007410      XCASH:: BGNSEG
2962 007410 104404      TRAP     C$BSEG
2963 007412 052737 020004 002342      BIS      #HDAL13!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
2964 007420 004737 006672      JSR      PC,LDRDR6      ;GO LOAD, READ AND CHECK HDAL REGISTER
2965 007424 001404      BEQ     1$              ;IF LOADED OK THEN CONTINUE
2966 007426      ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
2967 007426 104455      TRAP     C$ERDF
2968 007430 000004      .WORD   4
2969 007432 002605      .WORD   HDALRG
2970 007434 005020      .WORD   R06ERR
2971 007436      1$:      ENDSEG
2972 007436      10012$:
2973 007436 104405      TRAP     C$ESEG
2974 007440 000207      RTS      PC
2975
2976      ;THE FOLLOWING ROUTINE WILL SET HDAL13 H TO A ZERO AND HDAL2 H TO A ONE.
2977      ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
2978      ;CONTROL SIGNALS. HDAL13 H ON A ZERO WILL CAUSE THE SIGNAL XCAS H TO BE
2979      ;ASSERTED LOW AND THE SIGNAL XCAS L TO BE ASSERTED HIGH.
2980
2981 007442      XCASL:: BGNSEG
2982 007442 104404      TRAP     C$BSEG
2983 007444 052737 000004 002342      BIS      #BIT2,R6LOAD      ;SETUP DIAGNOSTIC CONTROL BIT
2984 007452 042737 020000 002342      BIC      #HDAL13,R6LOAD    ;SETUP BIT TO BE CLEARED
2985 007460 004737 006672      JSR      PC,LDRDR6      ;GO LOAD, READ AND CHECK HDAL REGISTER
2986 007464 001404      BEQ     1$              ;IF LOADED OK THEN CONTINUE
2987 007466      ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
2988 007466 104455      TRAP     C$ERDF
2989 007470 000004      .WORD   4
2990 007472 002605      .WORD   HDALRG
2991 007474 005020      .WORD   R06ERR
2992 007476      1$:      ENDSEG
2993 007476      10013$:
2994 007476 104405      TRAP     C$ESEG
2995 007500 000207      RTS      PC              ;RETURN BACK TO TEST
2996
2997      ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL15 IN THE HDAL REGISTER. HDAL15
2998      ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL 'XPI H'.
2999      ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
3000      ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
3001
3002 007502 004737 007514      XPI:: JSR      PC,XPIH      ;GO SET PPI L AND XPI L TO THE LOW STATE
3003 007506 004737 007546      JSR      PC,XPIL      ;GO SET PPI L AND XPI L TO HIGH STATE
3004 007512 000207      RTS      PC              ;RETURN BACK TO TEST
3005
3006      ;THE FOLLOWING ROUTINE WILL SET HDAL15 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE

```

```

3007 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL15 H
3008 ;ON A ONE WILL ASSERT THE SIGNALS PPI L AND XPI L TO THE LOW STATE.
3009
3010 007514 XPIH:: BGNSEG
3011 007514 104404 TRAP CSBSEG
3012 007516 052737 100004 002342 BIS #HDAL15!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
3013 007524 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
3014 007530 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
3015 007532 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
3016 007532 104455 TRAP C$ERDF
3017 007534 000004 .WORD 4
3018 007536 002605 .WORD HDALRG
3019 007540 005020 .WORD R06ERR
3020 007542 1$: ENDSEG
3021 007542 10014$:
3022 007542 104405 TRAP C$ESEG
3023 007544 000207 RTS PC ;RETURN BACK TO TEST
3024
3025 ;THE FOLLOWING ROUTINE WILL SET HDAL15 H TO A ZERO AND HDAL2 H TO A ONE. HDAL2 H
3026 ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
3027 ;HDAL15 H ON A ZERO WILL CAUSE THE SIGNALS PPI L AND XPI L TO BE ASSERTED HIGH.
3028
3029 007546 XPIL:: BGNSEG
3030 007546 104404 TRAP CSBSEG
3031 007550 052737 000004 002342 BIS #HDAL2,R6LOAD ;SETUP DIAGNOSTIC CONTROL BIT
3032 007556 042737 100000 002342 BIC #HDAL15,R6LOAD ;SETUP BIT TO BE CLEARED
3033 007564 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
3034 007570 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
3035 007572 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
3036 007572 104455 TRAP C$ERDF
3037 007574 000004 .WORD 4
3038 007576 002605 .WORD HDALRG
3039 007600 005020 .WORD R06ERR
3040 007602 1$: ENDSEG
3041 007602 10015$:
3042 007602 104405 TRAP C$ESEG
3043 007604 000207 RTS PC ;RETURN BACK TO TEST
3044
3045 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL7 IN THE HDAL REGISTER. HDAL7
3046 ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL XBCLR H + PBCLR H.
3047 ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
3048 ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
3049
3050 007606 004737 007620 XBCLR:: JSR PC,XBCLRH ;SET XBCLR H AND PBCLR H TO HIGH STATE
3051 007612 004737 007652 JSR PC,XBCLRL ;SET XBCLR H AND PBCLR H TO LOW STATE
3052 007616 000207 RTS PC ;RETURN BACK TO TEST
3053
3054 ;THE FOLLOWING ROUTINE WILL SET HDAL7 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
3055 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL7 H
3056 ;ON A ONE WILL ASSERT THE SIGNALS XBCLR H AND PBCLR H TO THE HIGH STATE
3057
3058 007620 XBCLRH::BGNSEG
3059 007620 104404 TRAP CSBSEG
3060 007622 052737 000204 002342 BIS #HDAL7!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
3061 007630 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
3062 007634 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE

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3063 007636          ERRDF  4,HDALRG,R06ERR          ;HDAL REGISTER NOT EQUAL EXPECTED
3064 007636 104455  TRAP    C$ERDF
3065 007640 000004  .WORD  4
3066 007642 002605  .WORD  HDALRG
3067 007644 005020  .WORD  R06ERR
3068 007646          1$:  ENDSEG
3069 007646          10016$:
3070 007646 104405  TRAP    C$ESEG
3071 007650 000207  RTS     PC          ;RETURN BACK TO TEST
3072
3073
3074          ;THE FOLLOWING ROUTINE WILL SET HDAL7 H TO A ZERO AND HDAL2 H TO A ONE. HDAL2 H
3075          ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
3076          ;HDAL7 H ON A ZERO WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED LOW
3077 007652          XBCLRL: :BGNSEG
3078 007652 104404  TRAP    C$BSEG
3079 007654 052737 000004 002342  BIS     #HDAL2,R6LOAD          ;SETUP DIAGNOSTIC CONTROL BIT
3080 007662 042737 000200 002342  BIC     #HDAL7,R6LOAD          ;SETUP BIT TO BE CLEARED
3081 007670 004737 006672  JSR     PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
3082 007674 001404  BEQ     1$                ;IF LOADED OK THEN CONTINUE
3083 007676          ERRDF  4,HDALRG,R06ERR          ;HDAL REGISTER NOT EQUAL EXPECTED
3084 007676 104455  TRAP    C$ERDF
3085 007700 000004  .WORD  4
3086 007702 002605  .WORD  HDALRG
3087 007704 005020  .WORD  R06ERR
3088 007706          1$:  ENDSEG
3089 007706          10017$:
3090 007706 104405  TRAP    C$ESEG
3091 007710 000207  RTS     PC          ;RETURN BACK TO TEST
3092

```

```

3093
3094
3095      ;THE FOLLOWING ROUTINE WILL SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4. VDAL2 H
3096      ;ON A ONE WILL CLEAR THE FOLLOWING FLIP-FLOPS:
3097      ; PAUSE STATE WORKING          PSMW H 0
3098      ; PAUSE STATE SYNC              EPSF H 0
3099      ; 16 BIT ADDRESS                 EPFN H 0
3100      ; 8 BIT INSTRUCTION HB          EP8F H 0
3101      ; 8 BIT ADDRESS LB              EP8G H 0
3102      ; 8 BIT ADDRESS HB              EP8N H 0
3103      ; TAKE NEW F.J. ADDRESS          TNFI H 0
3104      ; GET NEW ADDRESS FLIP-FLOP     OUT NEW H
3105      ; PAUSE MODE FLIP-FLOP         PAUSE L 0
3106      ; REFRESH FLIP-FLOP            REFR H 0
3107      ; FETCT LATCH FLIP-FLOP        EDFET H 0
3108      ;SETTING AND CLEARING VDAL2 H WILL ALSO CLOCK THE TAI AND TDAL BUSSES INTO THE
3109      ;DIAGNOSTIC LATCHES.
3110      007712
3111      007712 104404
3112      007714 052737 000004 002334
3113      007722 004737 006640
3114      007726 001405
3115      007730
3116      007730 104455
3117      007732 000003
3118      007734 002537
3119      007736 005004
3120      007740
3121      007740 104406
3122      007742 042737 000004 002334 1$:
3123      007750 004737 006640
3124      007754 001404
3125      007756
3126      007756 104455
3127      007760 000003
3128      007762 002537
3129      007764 005004
3130      007766
3131      007766
3132      007766 104405
3133      007770 000207
3134

```

CLRPSM::BGNSEG

```

TRAP      C$BSEG
BIS       #VDAL2,R4LOAD
JSR       PC,LDRDR4
BEQ       1$
ERRDF     3,VDALRG,R4EROR
TRAP      C$ERDF
.WORD     3
.WORD     VDALRG
.WORD     R4EROR
CKLOOP
TRAP      C$CLP1
BIC       #VDAL2,R4LOAD
JSR       PC,LDRDR4
BEQ       2$
ERRDF     3,VDALRG,R4EROR
TRAP      C$ERDF
.WORD     3
.WORD     VDALRG
.WORD     R4EROR
2$:
ENDSEG
10020$:
TRAP      C$ESEG
RTS       PC

```

```

;SETUP BIT TO SET VDAL2 H TO A ONE
;GO LOAD, READ AND CHECK VDAL REGISTER
;IF ALL OTHER BITS CLEARED THEN CONT
;VDAL REG OR PAUSE STATE MACHINE ERROR

```

```

;SETUP TO CLEAR VDAL2 H
;GO LOAD, READ AND CHECK VDAL REGISTER
;IF LOADED OK THEN CONTINUE
;VDAL OR PAUSE STATE MACHINE ERROR

```

```

;RETURN BACK TO TEST

```

```

3135
3136      ;THE FOLLOWING ROUTINE WILL SET ADALO H TO A ONE AND THEN ZERO. ADALO H BEING
3137      ;SET AND CLEARED WILL CAUSE A PULSE ON THE SIGNAL 'BRKRES L'. THE SIGNAL
3138      ;'BRKRES L' WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP AND INTERRUPT RELATED
3139      ;LOGIC.
3140
3141      BRKRES::BGNSEG
3142      TRAP      C$BSEG
3143      BIS      #ADALO,R2LOAD      ;SETUP BIT TO BE LOADED
3144      JSR      PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REGISTER
3145      BEQ      1$                ;IF LOADED OK THEN CONTINUE
3146      ERRDF   2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
3147      TRAP      C$ERDF
3148      .WORD   2
3149      .WORD   ADALRG
3150      .WORD   R2EROR
3151      CKLOOP
3152      TRAP      C$CLP1
3153      BIC      #ADALO,R2LOAD      ;SETUP BIT TO BE CLEARED
3154      JSR      PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REGISTER
3155      BEQ      2$                ;IF LOADED OK THEN CONTINUE
3156      ERRDF   2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
3157      TRAP      C$ERDF
3158      .WORD   2
3159      .WORD   ADALRG
3160      .WORD   R2EROR
3161      2$:      ENDSEG
3162      10021$:
3163      TRAP      C$ESEG
3164      RTS      PC                ;RETRUN BACK TO TEST
3165
3166
3167      010052      ENDMOD
3168

```



```
3169 .TITLE MISCELLANEOUS SECTIONS
3170 .SBTTL REPORT CODING SECTION
3171
3172 010052 BGNMOD
3173
3174 :++
3175 : THE REPORT CODING SECTION CONTAINS THE
3176 : 'PRINTS' CALLS THAT GENERATE STATISTICAL REPORTS.
3177 :--
3178
3179 010052 BGNRPT
3180 010052 L$RPT::
3181
3182
3183 010052 EXIT RPT
3184 010052 000167 .WORD JSJMP
3185 010054 000000 .WORD L10014-2-.
3186
3187
3188 .EVEN
3189
3190 010056 ENDRPT
3191 010056 L10014:
3192 010056 104425 TRAP C$RPT
3193
3194 .SBTTL PROTECTION TABLE
3195
3196 :++
3197 : THIS TABLE IS USED BY THE RUNTIME SERVICES
3198 : TO PROTECT THE LOAD MEDIA.
3199 :--
3200
3201 010060 BGNPROT
3202 010060 L$PROT::
3203
3204 010060 177777 -1 ;OFFSET INTO P-TABLE FOR CSR ADDRESS
3205 010062 177777 -1 ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
3206 010064 177777 -1 ;OFFSET INTO P-TABLE FOR DRIVE NUMBER
3207
3208 010066 ENDPROT
3209
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010072 104447
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012700 000037
010102 104447
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010104 103404
010106
012700 000034
010106 104447
010112
010114
010114 103014
010116
010116 104433
010120
012746 000002
012746 000102
012746 000100
012746 000003
010140 104437
010142 062706 000010
010146
012700 000035
010152 104447
010154
010154 103003
012737 177777 002314
010164
012700 000036
010170 104447
010172
010172 103433
010174 005237 002314
010200
013700 002314
010204 104442
010206 010005
010210
010210 103371
012701 002300
010216 005002
011511
010222 060221
010224 005202

```

.SBTTL INITIALIZE SECTION

:++
: THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
: AT THE BEGINNING OF EACH PASS.
:--

      BGNINIT
LSINIT:
      READEF #EF.START           ;SEE IF A START COMMAND
      MOV    #EF.START,R0
      TRAP   CSREFG
      BCOMPLETE 1$              ;BRANCH IF START COMMAND
      BCS    1$
      READEF #EF.RESTART        ;SEE IF A RESTART COMMAND
      MOV    #EF.RESTART,R0
      TRAP   CSREFG
      BCOMPLETE 1$              ;BRANCH IF RESTART
      BCS    1$
      READEF #EF.PWR            ;SEE IF RECOVERING FROM A POWER FAIL
      MOV    #EF.PWR,R0
      TRAP   CSREFG
      BNCOMPLETE 2$             ;IF NOT CHECK IN CONTINUE
      BCC    2$
1$:    BRESET                    ;ISSUE A BUS RESET
      TRAP   CSRESET
      SETVEC #100,#102,#RTI     ;SETUP CLOCK VECTOR TO DO A RETURN
      MOV    #RTI,-(SP)
      MOV    #102,-(SP)
      MOV    #100,-(SP)
      MOV    #3,-(SP)
      TRAP   CSSVEC
      ADD    #10,SP
2$:    READEF #EF.NEW           ;SEE IF A NEW PASS
      MOV    #EF.NEW,R0
      TRAP   CSREFG
      BNCOMPLETE 3$             ;IF NOT GO CHECK IF CONTINUE
      BCC    3$
      MOV    #-1,UNITNB         ;SETUP TO INIT UNIT NUMBER
3$:    READEF #EF.CONTINUE      ;CHECK IF CONTINUE
      MOV    #EF.CONTINUE,R0
      TRAP   CSREFG
      BCOMPLETE 6$             ;IF YES THEN EXIT
      BCS    6$
4$:    INC    UNITNB            ;INC TO NEW UNIT NUMBER
      GPHARD UNITNB,R5         ;GET DEVICE INFORMATION
      MOV    UNITNB,R0
      TRAP   CSGPHRD
      MOV    R0,R5
      BNCOMPLETE 4$           ;GO TRY ANOTHER UNIT
      BCC    4$
      MOV    #REG0,R1          ;ADDRESS OF ED DEVICE ADDRESS TABLE
      CLR    R2                ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
5$:    MOV    (R5),(R1)         ;GET ADDRESS AND SAVE
      ADD    R2,(R1)+          ;ADD OFFSET TO ADDRESS
      INC    R2                ;UPDATE OFFSET BY 2
  
```

3266	010226	005202			INC	R2	
3267	010230	022702	000010		CMP	#10,R2	:CHECK IF DONE LOADING TABLE
3268	010234	001371			BNE	5\$:GO UPDATE NEXT ADDRESS
3269	010236	005725			TST	(R5)+	:UPDATE THE POINTER
3270	010240	012537	002312		MOV	(R5)+,TEVECT	:GET TARGET EMULATOR VECTOR ADDRESS
3271	010244	005037	002310		CLR	IDDEV	:CLEAR OUT DEVICE NUMBER
3272	010250	111537	002311		MOVB	(R5),IDDEV+1	:GET THE TE DEVICE NUMBER
3273	010254	012737	100000	002316	MOV	#GDAL15,IDTYPE	:SETUP TE DEVICE TYPE
3274	010262				SETPRI	#PRI07	:RAISE PROCESSOR PRIORITY
3275	010262	012700	000340	6\$:	MOV	#PRI07,R0	
3276	010266	104441			TRAP	C\$SPRI	
3277							
3278							
3279	010270				EXIT	INIT	
3280	010270	104432			TRAP	C\$EXIT	
3281	010272	000002			.WORD	L10016-	
3282							
3283							
3284					.EVEN		
3285							
3286	010274				ENDINIT		
3287	010274			L10016:			
3288	010274	104411			TRAP	C\$INIT	

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 3302 010276
 3303 010276
 3304 010276 104461
 3305
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 3314 010300
 3315 010300
 3316 010300 012700 000340
 3317 010304 104441
 3318 010306 013777 002310 171764
 3319
 3320 010314 012777 000000 171760
 3321
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 3323 010322
 3324 010322 104432
 3325 010324 000002
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 3330 010326
 3331 010326
 3332 010326 104412

```
.SBTTL AUTODROP SECTION

:++
: THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
: THE 'ADR' FLAG WAS SET. THE UNIT(S) UNDER TEST ARE CHECKED TO
: SEE IF THEY WILL RESPOND. THOSE THAT DON'T ARE IMMEDIATELY
: DROPPED FROM TESTING.
:--

      BGNAUTO
L$AUTO::

      ENDAUTO
L10017: TRAP  C$AUTO

.SBTTL CLEANUP CODING SECTION

:++
: THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
: AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
:--

      BGNCLN
L$CLEAN::
      SETPRI  #PRI07           ;RAISE THE CPU PRIORITY LEVEL TO 7
      MOV     #PRI07,R0
      TRAP   C$SPRI
      MOV     IDDEV,@REG0     ;CLEAR CONTROL REGISTER 0 EXCEPT
                               ;FOR DEVICE NUMBER
      MOV     #0,@REG.       ;CLEAR REGISTER 2

      EXIT   CLN
      TRAP  C$EXIT
      .WORD L10020-.

      .EVEN
L10020: ENDCLN
      TRAP  C$CLEAN
```

```
3333 .SBTTL DROP UNIT SECTION
3334
3335
3336 :++
3337 : THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
3338 : TO NO LONGER BE TESTED.
3339 :--
3340 010330          BGNDU
3341 010330
3342
3343
3344 010330          EXIT    DU
3345 010330 000167   .WORD   JSJMP
3346 010332 000000   .WORD   L10021-2-.
3347
3348
3349
3350
3351 010334          .EVEN
3352 010334          ENDDU
3353 010334 104453   L10021: TRAP   C$DU
3354
3355 .SBTTL ADD UNIT SECTION
3356
3357 :++
3358 : THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES
3359 : TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK
3360 : TO THE TEST CYCLE.
3361 :--
3362
3363 010336          B$GNAU
3364 010336
3365
3366
3367 010336          EXIT    AU
3368 010336 000167   .WORD   JSJMP
3369 010340 000000   .WORD   L10022-2-.
3370
3371
3372
3373
3374 010342          .EVEN
3375 010342          ENDAU
3376 010342 104452   L10022: TRAP   C$AU
3377
3378 010344          ENDMOD
3379
```

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.TITLE HARDWARE TESTS

.SBTTL TEST 1: SELECT AND INITIALIZE TARGET EMULATOR

BGNMOD

..**
: THIS TEST WILL CHECK THAT THE TARGET EMULATOR MODULE CAN BE SELECTED AND
: INITIALIZED TO A KNOWN STATE. THE TEST DESCRIBED BELOW WILL BE EXECUTED AT
: THE BEGINNING OF EACH TEST TO PUT THE TARGET EMULATOR IN A KNOWN STATE.
:
: THE TEST WILL LOAD AND CHECK THAT THE DEVICE NUMBER CAN BE LOADED INTO AND
: READ FROM CONTROL REGISTER 0. ALL THE READ/WRITE BITS WILL BE LOADED AND
: CHECKED FOR ZEROES. THE TEST WILL CHECK THAT THE TARGET EMULATOR DEVICE
: TYPE CAN BE READ BY SETTING CONTROL REGISTER 0 BIT 15 TO A ONE AND THEN
: READING CONTROL REGISTER 0. THE TEST WILL SET CONTROL REGISTER 0 BIT 15 TO
: A ZERO AND BITS 1 AND 0 TO ONES. BIT 15 ON A ZERO WILL ENABLE THE DEVICE
: NUMBER TO BE READ AGAIN. BITS 1 AND 0 SET TO ONES WILL CAUSE THE HDAL
: REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
: THE TEST WILL NOW LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL BIT 2
: SET TO A ONE AND ALL OTHER HDAL BITS CLEARED. HDAL BIT 2 SET TO A ONE WILL
: ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS USING THE
: BITS IN THE HDAL REGISTER. THE TEST WILL NOW SET CONTROL REGISTER 0 BITS
: 1 AND 0 TO ZEROES AND BIT 2 TO A ONE. CONTROL REGISTER 0 BIT 2 ON A ONE WILL
: CAUSE THE MODE REGISTER TO BE SELETED ON A WRITE OR READ COMMAND TO CONTROL
: REGISTER 6. THE TEST WILL LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA
: PATTERN OF ALL ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL CAUSE 16 BIT
: ADDRESS MODE TO BE SELECTED. THE TEST WILL SET ADAL REGISTER BIT 0 TO A 1
: AND THEN A ZERO. ALL OTHER ADAL REGISTER BITS WILL BE LOADED AND CHECKED FOR
: ZEROES. ADAL REGISTER BIT 0 BEING SET TO A ONE WILL CLEAR THE BREAK LATCH
: FLIP-FLOP, THE SINGLE STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK
: FLIP-FLOP. ADAL REGISTER BIT 2 ON A ZERO WILL CAUSE THE T-11 CHIP TO BE
: TURNED OFF. THE TEST WILL THEN READ AND CHECK CONTROL REGISTER 0 TO CHECK
: THAT ALL THE BREAK BITS ARE CLEARED. THE TEST WILL NOW SET VDAL REGISTER
: BIT 2 TO A ONE AND THEN A ZERO. ALL OTHER VDAL READ/WRITE BITS WILL BE
: LOADED AND CHECKED FOR ZEROES. VDAL REGISTER BIT 2 ON A ONE WILL CAUSE ALL
: THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE, EXCEPT THOSE CLEARED BY ADAL
: REGISTER BIT 0, TO BE SET TO A KNOWN STATE.
:--

T1:: BGNST
JSR PC,INITTE ;INITIALIZE THE TARGET EMULATOR

L10023: ENDTST
TRAP C\$ETST

TEST 2: GDAL 3:0 R/W REG TEST (1'S AND 0'S)

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010352
 010352
 010352 004737 005510
 010356
 010356 104404
 010360 112737 000017 002320
 010366 004737 006554
 010372 001404
 010374
 010374 104455
 010376 000001
 010400 002406
 010402 004754
 010404
 010404
 010404 104405
 010406
 010406 104404
 010410 105037 002320
 010414 004737 006554
 010420 001404
 010422
 010422 104455
 010424 000001
 010426 002406
 010430 004754
 010432
 010432
 010432 104405
 010434
 010434
 010434 104401

```
.SBTTL TEST 2: GDAL 3:0 R/W REG TEST (1'S AND 0'S)

:++
: THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS, GDAL 3:0, CAN
: BE SET TO ALL ONES (17), AND THEN SET TO ALL ZEROES. THE READ ONLY BITS,
: GDAL7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.
:--

T2::      BGNTST
          JSR      PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR

          BGNSEG
          TRAP     C$BSEG

          ;CHECK THAT R/W BITS GDAL 3:0 CAN BE SET TO ALL ONES

          MOVB     #17,ROLOAD         ;SETUP BITS TO BE LOADED
          JSR      PC,LDRDRO         ;GO LOAD, READ AND CHECK REG 0
          BEQ      1$                ;IF LOADED OK THEN CONTINUE
          ERRDF    1,GDALRG,ROEROR   ;REGISTER 0 NOT EQUAL 17
          TRAP     C$ERDF
          .WORD    1
          .WORD    GDALRG
          .WORD    ROEROR

1$:
10000$:   ENDSEG
          TRAP     C$ESEG

          BGNSEG
          TRAP     C$BSEG

          ;CHECK THAT R/W BITS GDAL 3:0 CAN BE SET TO ALL ZEROES

          CLRB     ROLOAD             ;SETUP TO CLEAR ALL BITS
          JSR      PC,LDRDRO         ;GO LOAD, READ AND CHECK REG 0
          BEQ      2$                ;IF LOADED OK THEN CONTINUE
          ERRDF    1,GDALRG,ROEROR   ;REGISTER 0 R/W BITS NOT EQUAL 0
          TRAP     C$ERDF
          .WORD    1
          .WORD    GDALRG
          .WORD    ROEROR

2$:
10001$:   ENDSEG
          TRAP     C$ESEG

L10024:   TRAP     C$ESETST
```

TEST 3: GDAL 3:0 R/W REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 3: GDAL 3:0 R/W REG TEST (1'S + 0'S, 0'S + 1'S)

;++
 : THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS GDAL 3:0, CAN
 : BE LOADED WITH ONES AND ZEORES (12) AND THEN LOADED WITH ZEROES AND ONES (5).
 : THE READ ONLY BITS GDAL 7:4 ARE CHECKED TO BE CLEARED DURING THIS TEST.
 :--

3482
 3483
 3484
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 3491
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 3493
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 3498
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010436
 010436
 010436 004737 005510
 010442
 010442 104404
 010444 112737 000012 002320
 010452 004737 006554
 010456 001404
 010460
 010460 104455
 010462 000001
 010464 002406
 010466 004754
 010470
 010470 104405
 010472
 010472 104404
 010474 112737 000005 002320
 010502 004737 006554
 010506 001404
 010510
 010510 104455
 010512 000001
 010514 002406
 010516 004754
 010520
 010520
 010520 104405
 010522
 010522
 010522 104401

BGNTST
 T3:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
 BGNSEG
 TRAP C\$BSEG
 :LOAD READ/WRITE BITS GDAL 3:0 WITH AN ALTERNATING ONES AND ZEROES DATA
 :PATTERN (12).
 MOVB #12,ROLOAD ;SETUP BITS TO BE LOADED
 JSR PC,LDRDRO ;GO LOAD, READ AND CHECK REGISTER 0
 BEQ 1\$;IF LOADED OK THEN CONTINUE
 ERRDF 1,GDALRG,ROEROR ;REGISTER 0 NOT EQUAL TO 12
 TRAP C\$ERDF
 .WORD 1
 .WORD GDALRG
 .WORD ROEROR
 1\$: ENDSEG
 10000\$: TRAP C\$ESEG
 BGNSEG
 TRAP C\$BSEG
 :LOAD READ/WRITE BITS GDAL 3:0 WITH AN ALTERNATING ZEROES AND ONES DATA
 :PATTERN
 MOVB #5,ROLOAD ;SETUP BITS TO BE LOADED
 JSR PC,LDRDRO ;GO LOAD, READ AND CHECK REGISTER 0
 BEQ 2\$;IF LOADED OK THEN CONTINUE
 ERRDF 1,GDALRG,ROEROR ;REGISTER 0 NOT EQUAL TO 5
 TRAP C\$ERDF
 .WORD 1
 .WORD GDALRG
 .WORD ROEROR
 2\$: ENDSEG
 10001\$: TRAP C\$ESEG
 L10025: TRAP C\$ETST

TEST 4: GDAL 3:0 R/W REG TEST VIA BINARY COUNT

.SBTTL TEST 4: GDAL 3:0 R/W REG TEST VIA BINARY COUNT

:++
: THIS TEST WILL CHECK CONTROL REGISTER 0 R/W BITS USING A BINARY COUNT PATTERN.
: THE PATTERN WILL START INITIALLY AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN
: EQUALS 17. THE READ ONLY BITS, GDAL 7:4, ARE CHECKED TO BE CLEARED DURING
: THIS TEST.
:--

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3541 010524
3542 010524
3543 010524 004737 005510
3544
3545 010530 105037 002320
3546
3547 010534
3548 010534 104404
3549 010536 004737 006554
3550 010542 001404
3551 010544
3552 010544 104455
3553 010546 000001
3554 010550 002406
3555 010552 004754
3556 010554
3557 010554
3558 010554 104405
3559 010556 005237 002320
3560 010562 122737 000020 002320
3561 010570 001361
3562 010572
3563 010572
3564 010572 104401
3565

T4:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
CLRB ROLOAD ;SETUP TO START PATTERN AT 0
1\$: BGNSEG
TRAP C\$BSEG
JSR PC,LDRDRO ;GO LOAD, READ AND CHECK CONTROL REG 0
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 1,GDALRG,ROEROR ;REGISTER 0 NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 1
.WORD GDALRG
.WORD ROEROR
2\$: ENDSEG
10000\$: TRAP C\$ESEG
INC ROLOAD ;UPDATE REGISTER 0 BY ONE
CMPB #?0,ROLOAD ;CHECK IF ALL R/W BITS TESTED
BNE 1\$;IF NOT THEN LOAD NEXT PATTERN
ENDTST
L10026: TRAP C\$ETST

TEST 5: ADAL 15:0 REG TEST (1'S AND 0'S)

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3599
3600
3601
3602
3603
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3605
3606
3607
3608
3609
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010574
010574
010574 004737 005510
010600
010600 104404
010602 012737 177777 002330
010610 004737 006614
010614 001404
010616
010616 104455
010620 000002
010622 002513
010624 004770
010626
010626 104405
010630
010630 104404
010632 005037 002330
010636 004737 006614
010642 001404
010644
010644 104455
010646 000002
010650 002513
010652 004770
010654
010654
010654 104405
010656
010656
010656 104401

.SBTTL TEST 5: ADAL 15:0 REG TEST (1'S AND 0'S)

:++
: THIS TEST WILL CHECK THAT CONTROL REGISTER 2 BITS ADAL 15:0 CAN BE SET TO
: ALL ONES (177777) AND THEN ALL ZERES (000000).
:--

T5:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C\$BSEG
;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH A DATA PATTERN OF ALL ONES
MOV #177777,R2LOAD ;SETUP FOR ALL ONES DATA PATTERN
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
BEQ 1\$;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL 177777
TRAP C\$ERDF
.WORD 2
.WORD ADALRG
.WORD R2EROR
1\$: ENDSEG
10000\$: TRAP C\$ESEG
BGNSEG
TRAP C\$BSEG
;LOAD, READ AND CHECK CONTROL REG 2 WITH A DATA PATTERN OF ALL ZEROES.
CLR R2LOAD ;SETUP ALL ZEROES DATA PATTERN
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL TO 000000
TRAP C\$ERDF
.WORD 2
.WORD ADALRG
.WORD R2EROR
2\$: ENDSEG
10001\$: TRAP C\$ESEG
L10027: ENDTST
TRAP C\$ETST

TEST 6: ADAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 6: ADAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

:++
: THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:0 WITH AN
: ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN WITH AN ALTERNATING
: ZEROES AND ONES DATA PATTERN (052525).
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3664

010660
010660
010660 004737 005510

010664
010664 104404

010666 012737 125252 002330

010674 004737 006614

010700 001404

010702

010702 104455

010704 000002

010706 002513

010710 004770

010712

010712

010712 104405

010714

010714 104404

010714

010714

010716 012737 052525 002330

010724 004737 006614

010730 001404

010732

010732 104455

010734 000002

010736 002513

010740 004770

010742

010742

010742 104405

010744

010744

010744 104401

T6:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR

BGNSEG
TRAP C\$BSEG

;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH AN ALTERNATING ONES AND
;ZEROES DATA PATTERN (125252)

MOV #125252,R2LOAD ;SETUP DATA PATTERN TO BE LOADED
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
BEQ 1\$;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL 125252
TRAP C\$ERDF
.WORD 2
.WORD ADALRG
.WORD R2EROR

1\$:

10000\$:
TRAP C\$ESEG

BGNSEG
TRAP C\$BSEG

;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH AN ALTERNATING ZEROES AND
;ONES DATA PATTERN (052525)

MOV #052525,R2LOAD ;SETUP PATTERN TO BE LOADED
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL 052525
TRAP C\$ERDF

2\$:

10001\$:
TRAP C\$ESEG

ENDTST

L10030:
TRAP C\$ETST

TEST 7: ADAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

.SBTTL TEST 7: ADAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

:++
: THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 7:0 USING A
: BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND
: INCREMENT TO 377 BY AN INCREMENT OF ONE.
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3665
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3673 010746
3674 010746
3675 010746 004737 005510
3676
3677 010752 005037 002330
3678
3679 010756
3680 010756 104404
3681 010760 004737 006614
3682 010764 001404
3683 010766
3684 010766 104455
3685 010770 000002
3686 010772 002513
3687 010774 004770
3688 010776
3689 010776
3690 010776 104405
3691 011000 005237 002330
3692 011004 032737 000400 002330
3693 011012 001761
3694 011014
3695 011014
3696 011014 104401

T7:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
CLR R2LOAD ;SET PATTERN INITIALLY TO 0
1\$: BGNSEG
TRAP C\$BSEG
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 2
WORD ADALRG
.WORD R2EROR
2\$: ENDSEG
10000\$: TRAP C\$ESEG
INC R2LOAD ;UPDATE TEST PATTERN BY ONE
BIT #ADAL8,R2LOAD ;CHECK IF PATTERN DONE
BEQ 1\$;IF NOT THEN DO NEXT PATTERN
ENDTST
L10031: TRAP C\$ETST

TEST 8: ADAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

.SBTTL TEST 8: ADAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

;++
 : THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:8 USING A
 : BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND
 : INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED.
 :--

3697
 3698
 3699
 3700
 3701
 3702
 3703
 3704
 3705
 3706
 3707
 3708
 3709
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 3712
 3713
 3714
 3715
 3716
 3717
 3718
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 3720
 3721
 3722
 3723
 3724
 3725
 3726
 3727
 3728

011016
 011016
 011016 004737 005510
 011022 005037 002330
 011026
 011026 104404
 011030 004737 006614
 011034 001404
 011036
 011036 104455
 011040 000002
 011042 002513
 011044 004770
 011046
 011046
 011046 104405
 011050 062737 000400 002330
 011056 001363
 011060
 011060
 011060 104401

BGNTST
 T8:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
 CLR R2LOAD ;SET PATTERN INITIALLY TO 0
 1\$: BGNSEG
 TRAP C\$BSEG
 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REGISTER 2
 BEQ 2\$;IF LOADED OK THEN CONTINUE
 ERRDF 2,ADALRG,R2EROR ;REGISTER 2 NOT EQUAL EXPECTED
 TRAP C\$ERDF
 .WORD 2
 .WORD ADALRG
 .WORD R2EROR
 2\$: ENDSEG
 10000\$: TRAP C\$ESEG
 ADD #ADALB,R2LOAD ;UPDATE TEST PATTERN BY ONE
 BNE 1\$;IF NOT DONE THEN DO NEXT PATTERN
 ENDTST
 L10032: TRAP C\$ETST

TEST 9: VDAL REGISTER R/W BIT TEST

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 3751
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 3755
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 3758
 3759
 3760
 3761
 3762
 3763
 3764
 3765
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 3767
 3768
 3769
 3770
 3771
 3772
 3773
 3774
 3775
 3776
 3777

011062
 011062
 011062 004737 005510
 011066 012737 000207 002334
 011074 012701 000010
 011100
 011100 104404
 011102 004737 006640
 011106 001404
 011110
 011110 104455
 011112 000003
 011114 002537
 011116 005004
 011120
 011120
 011120 104405
 011122 005301
 011124 001403
 011126 005337 002334
 011132 000762
 011134 105737 002334
 011140 100006
 011142 012701 000010
 011146 012737 000007 002334
 011154 000751
 011156
 011156
 011156 104401

.SBTTL TEST 9: VDAL REGISTER R/W BIT TEST

```

:++
: THIS TEST WILL CHECK THAT CONTROL REGISTER 4 READ/WRITE BITS VDAL7, VDAL2,
: VDAL1 AND VDALO CAN BE SET AND CLEARED. THE TEST WILL CHECK THESE BITS
: USING A DECREMENTING BINARY COUNT PATTERN. THE READ ONLY BITS WILL BE CHECKED
: TO BE ZEROES DURING THIS TEST. READ ONLY BITS VDAL 15:8 SHOULD BE ZERO AS A
: RESULT OF VDAL2 H BEING SET TO A ONE DURING THIS TEST. READ ONLY BITS 6:3
: SHOULD BE A ZERO AS A RESULT OF ADAL BIT 10 BEING A ZERO. THE ADAL REGISTER
: WAS CLEARED IN THE ABOVE ROUTINE "INITTE".
:--
  
```

```

          BGNSTST
T9::
          JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
          MOV    #VDAL7!VDAL2!VDAL1!VDALO,R4LOAD ;START ALL R/W BITS ON A ONE
          MOV    #3.,R1             ;SETUP TEST PATTERN COUNTER

1$:      BGNSEG
          TRAP   C$BSEG

          ;LOAD, READ AND CHECK VDAL REGISTER'S READ/WRITE BITS WITH A DECREASING
          ;BINARY COUNT PATTERN. THE PATTERN WILL START AT 207 AND DECREASE BY
          ;ONE TO A PATTERN OF 200. THE PATTERN WILL THEN BE RESET TO 7 AND
          ;DECREASE BY ONE UNTIL THE PATTERN OF ZERO HAS BEEN LOADED AND CHECKED.

          JSR    PC,LDRDR4          ;GO LOAD, READ AND CHECK VDAL REGISTER
          BEQ    2$                  ;IF LOADED OK THEN CONTINUE
          ERDF   3,VDALRG,R4EROR    ;VDAL REGISTER NOT EQUAL EXPECTED
          TRAP   C$ERDF
          .WORD  3
          .WORD  VDALRG
          .WORD  R4EROR

2$:      ENDSEG
10000$:  TRAP   C$ESEG

          DEC    R1                  ;CHECK IF DONE WITH LOW ORDER 3 BITS
          BEQ    3$                  ;IF YES CHECK IF BIT 7 HAS BEEN CLEARED
          DEC    R4LOAD              ;DECREMENT TEST PATTERN BY ONE
          BR     1$                  ;GO LOAD THE NEXT PATTERN
          TSTB   R4LOAD              ;CHECK IF BIT 7 HAS BEEN CLEARED
          BPL    4$                  ;IF YES THEN TEST IS DONE
          MOV    #8.,R1              ;RESET PATTERN COUNTER
          MOV    #VDAL2!VDAL1!VDALO,R4LOAD ;SET THE LOW ORDER 3 BITS TO ONES
          BR     1$                  ;REPEAT THE TEST AGAIN WITH BIT 7 A 0

3$:      TSTB   R4LOAD
          BPL    4$
          MOV    #8.,R1
          MOV    #VDAL2!VDAL1!VDALO,R4LOAD
          BR     1$

4$:      ENDTST
L10033:  TRAP   C$ETST
  
```

TEST 10: HDAL 15:0 REG TEST (1'S AND 0'S)

.SBTTL TEST 10: HDAL 15:0 REG TEST (1'S AND 0'S)

```

:++
: THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE SET TO ALL ONES
: (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE HDAL REGISTER, THE
: TEST WILL SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0. ON A WRITE
: COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDALO SET TO ONES, PULSES WILL
: OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE
: DATA ON THE WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER. ON A READ
: COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDALO SET TO ONES, A PULSE WILL
: OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE
: READBACK.
:--
  
```

3778
 3779
 3780
 3781
 3782
 3783
 3784
 3785
 3786
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 3788
 3789
 3790
 3791
 3792
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 3794
 3795
 3796
 3797
 3798
 3799
 3800
 3801
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 3810
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 3816
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 3819

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011160
011160
011160 004737 005510
011164
011164 104404
011166 004737 006754
011172 012737 177777 002342
011200 004737 006672
011204 001404
011206 104455
011210 000004
011212 002605
011214 005020
011216
011216
011216 104405
  
```

```

T10:: BGNTST
      JSR    PC,INITTE           ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
      ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
      JSR    PC,SLHDAL          ;SELECT HDAL REG VID GDAL BITS 2:0
      ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF
      ;ALL ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
      ;REGISTER 6 WITH GDAL1 AND GDALO SET IN CONTROL REGISTER 0.
      MOV    #177777,R6LOAD      ;SETUP DATA TO BE LOADED
      JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ    1$                 ;IF LOADED OK THEN CONTINUE
      ERRDF  4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL 177777
      TRAP   C$ERDF
      .WORD  4
      .WORD  HDALRG
      .WORD  R06ERR
1$:   ENDSEG
10000$: TRAP   C$ESEG
  
```

```

3820 011220          BGNSEG
3821 011220 104404  TRAP   C$BSEG
3822
3823
3824                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF
3825                ;ALL ZEROS (000000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
3826                ;REGISTER 6 WITH GDAL1 AND GDALO SET IN CONTROL REGISTER 0.
3827 011222 005037 002342 CLR   R6LOAD          ;SETUP DATA TO BE LOADED
3828 011226 004737 006672 JSR   PC,LDRDR6       ;GO LOAD, READ AND CHECK HDAL REGISTER
3829 011232 001404      BEQ   2$                ;IF LOADED OK THEN CONTINUE
3830 011234          ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL 000000
3831 011234 104455  TRAP   C$ERDF
3832 011236 000004      .WORD 4
3833 011240 002605      .WORD HDALRG
3834 011242 005020      .WORD R06ERR
3835 011244          2$: ENDSEG
3836 011244          10001$:
3837 011244 104405  TRAP   C$ESEG
3838 011246          ENDTST
3839 011246          L10034:
3840 011246 104401  TRAP   C$ETST
3841
  
```


TEST 11: HDAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 11: HDAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

```

:++
: THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE LOADED WITH AN
: ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND
: ONES DATA PATTERN (052525). TO SELECT THE HDAL REGISTER, THE TEST WILL SET
: GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL
: REGISTER 6 WITH GDAL1 AND GDALO SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS
: WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND
: TO BE LOADED INTO THE HDAL REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6
: WITH GDAL1 AND GDALO SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L.
: THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.
:--
  
```

3842
 3843
 3844
 3845
 3846
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 3853
 3854
 3855
 3856
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 3858
 3859
 3860
 3861
 3862
 3863
 3864
 3865
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 3867
 3868
 3869
 3870
 3871
 3872
 3873
 3874
 3875
 3876
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 3878
 3879
 3880
 3881
 3882
 3883
 3884

```

011250
011250
011250 004737 005510
011254
011254 104404
011256 004737 006754
011262 012737 125252 002342
011270 004737 006672
011274 001404
011276
011276 104455
011300 000004
011302 002605
011304 005020
011306
011306
011306 104405
  
```

```

T11:: BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
      ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
      JSR    PC,SLHDAL         ;SELECT HDAL REG VIA GDAL BITS 2:0
      ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH AN ALTERNATING ONES
      ;AND ZEROES DATA PATTERN (125252) BY ISSUING A WRITE AND READ COMMAND
      ;TO CONTROL REGISTER 6 WITH GDAL1 AND GDALO SET TO ONES IN CONTROL
      ;REGISTER 0.
      MOV    #125252,R6LOAD    ;SETUP DATA TO BE LOADED
      JSR    PC,LDRDR6        ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ    1$               ;IF LOADED OK THEN CONTINUE
      ERRDF  4,HDALRG,R06ERR  ;HDAL REGISTER NOT EQUAL 125252
      TRAP   C$ERRDF
      .WORD  4
      .WORD  HDALRG
      .WORD  R06ERR
1$:   ENDSEG
10000$: TRAP   C$ESEG
  
```

```
3885
3886 011310
3887 011310 104404
3888
3889
3890
3891
3892
3893
3894 011312 012737 052525 002342
3895 011320 004737 006672
3896 011324 001404
3897 011326
3898 011326 104455
3899 011330 000004
3900 011332 002605
3901 011334 005020
3902 011336
3903 011336
3904 011336 104405
3905
3906 011340
3907 011340
3908 011340 104401
3909
```

BGNSEG
TRAP C\$BSEG

:LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH AN ALTERNATING
:ZEROS AND ONES DATA PATTERN (052525) BY ISSUING A WRITE AND READ
:COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET IN CONTROL
:REGISTER 0.

MOV #052525,R6LOAD ;SETUP DATA PATTERN TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
BEQ 2\$;IF LOADED OK THEN CONTINUE
LRRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL 052525
IRAP C\$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
2\$:
10001\$:
ENDSEG
TRAP C\$ESEG
ENDTST
L10035:
TRAP C\$ETST

TEST 12: HDAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

.SBTTL TEST 12: HDAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

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3944
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3957

011342
011342
011342 004737 005510
011346 005037 002342
011352
011352 104404

011354 004737 006754

011360 004737 006672
011364 001404
011366
011366 104455
011370 000004
011372 002605
011374 005020
011376
011376
011376 104405
011400 005237 002342
011404 032737 000400 002342
011412 001757
011414
011414
011414 104401

:++
: THIS TEST WILL CHECK THE LOW BYTE OF THE HDAL REGISTER USING A BINARY COUNT
: PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE
: PATTERN 377 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED
: ARE HDAL BITS 7:0. TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND
: GDALO TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER
: 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
: WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
: THE HDAL REGISTER VIA THE SIGNAL RPT3 L.
:--

BGNTST
T12:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
CLR R6LOAD ;START INITIAL PATTERN AT 0
1\$: BGNSEG
TRAP C\$BSEG
:SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
:REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL BITS 2:0
:LOAD, READ AND CHECK HDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
:THE HIGH BYTE OF THE HDAL REGISTER WILL BE CHECKED TO CONTAIN ZEROES
:DURING THIS TEST.
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK THE HDAL REG
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REG NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
2\$: ENDSEG
10000\$: TRAP C\$ESEG
INC R6LOAD ;UPDATE TEST PATTERN BY ONE
BIT #HDAL8,R6LOAD ;CHECK IF TEST PATTERN DONE
BEQ 1\$;IF NOT THEN LOAD NEXT PATTERN
ENDTST
L10036: TRAP C\$ETST

TEST 13: HDAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

3958
 3959
 3960
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 3983
 3984
 3985
 3986
 3987
 3988
 3989
 3990
 3991
 3992
 3993
 3994
 3995
 3996
 3997
 3998
 3999
 4000
 4001
 4002
 4003
 4004

011416
 011416
 011416 004737 005510
 011422 005037 002342
 011426
 011426 104404
 011430 004737 006754
 011434 004737 006672
 011440 001404
 011442 104455
 011444 000004
 011446 002605
 011450 005020
 011452
 011452 104405
 011454 062737 000400 002342
 011462 001361
 011464
 011464
 011464 104401

.SBTTL TEST 13: HDAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

```

:++
: THIS TEST WILL CHECK THE HIGH BYTE OF THE HDAL REGISTER USING A BINARY COUNT
: PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE
: PATTERN 177400 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED
: ARE HDAL BITS 15:8. TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND
: GDALO TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER
: 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
: WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
: THE HDAL REGISTER VIA THE SIGNAL RPT3 L.
:--
  
```

```

BGNTST
T13:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
      CLR R6LOAD ;START INITIAL PATTERN AT 0
1$: BGNSEG
   TRAP C$BSEG
      ;SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
      ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
      JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL BITS 2:0
      ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A BINARY COUNT PATTERN
      ;THE LOW BYTE OF THE HDAL REGISTER WILL BE CHECKED TO CONTAIN ZEROES
      ;DURING THIS TEST.
      JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK THE HDAL REG
      BEQ 2$ ;IF LOADED OK THEN CONTINUE
      ERRDF 4,HDALRG,R06ERR ;HDAL REG NOT EQUAL EXPECTED
      TRAP C$ERDF
      .WORD 4
      .WORD HDALRG
      .WORD R06ERR
2$: ENDSEG
10000$: TRAP C$ESEG
      ADD #HDAL8,R6LOAD ;UPDATE THE HIGH BYTE BY ONE
      BNE 1$ ;IF PATTERN NOT DONE LOAD NEXT WORD
      ENDTST
L10037: TRAP C$ETST
  
```

TEST 14: MODE REG 15:0 REG TEST (1'S AND 0'S)

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4006
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011466
011466
011466 004737 005510
011472
011472 104404
011474 004737 007006
011500 012737 177777 002342
011506 004737 006672
011512 001404
011514 104455
011516 000004
011520 002631
011522 005020
011524
011524
011524 104405

```
.SBTTL TEST 14: MODE REG 15:0 REG TEST (1'S AND 0'S)
:++
: THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE SET TO ALL ONES
: (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE MODE REGISTER, THE
: TEST WILL SET GDAL2 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO
: CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, PULSES WILL BE OCCUR ON THE
: SIGNALS WPT4 LB H AND WPT4 HB H. THESE PULSE WILL CAUSE THE DATA ON THE
: WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO
: CONTROL REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0, A PULSE WILL OCCUR
: ON THE SIGNAL RPT4 L. THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK
:--

T14:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR

BGNSEG
TRAP C$BSEG

;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0

;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF
;ALL ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
;REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0.

MOV #177777,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL 177777
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR

1$: ENDSEG
10000$: TRAP C$ESEG
```

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4046
4047 011526
4048 011526 104404
4049
4050
4051
4052
4053
4054 011530 005037 002342
4055 011534 004737 006672
4056 011540 001404
4057 011542
4058 011542 104455
4059 011544 000004
4060 011546 002631
4061 011550 005020
4062 011552
4063 011552
4064 011552 104405
4065
4066 011554
4067 011554
4068 011554 104401
4069
```

```

BGNSEG
TRAP C$BSEG

;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF
;ALL ZERES (000000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
;REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0.

CLR R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL 000000
TRAP C$ERDF

.WORD 4
.WORD MODREG
.WORD R06ERR

2$:
10001$:
ENDSEG

TRAP C$ESEG

ENDTST

L10040:
TRAP C$ETST
```

TEST 15: MODE REG 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 15: MODE REG 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

: THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE LOADED WITH AN
: ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND
: ONES DATA PATTERN (052525). TO SELECT THE MODE REGISTER, THE TEST WILL SET
: GDAL2 IN THE LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL
: REGISTER 6 WITH GDAL2 SET TO A ONE IN REG 0, PULSES WILL OCCUR ON THE SIGNALS
: WPT4 LB H AND WPT4 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND
: TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6
: WITH GDAL2 SET TO A ONE, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L. THIS SIGNAL
: WILL CAUSE THE MODE REGISTER TO BE READBACK.
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4097
4098
4099
4100
4101
4102
4103
4104
4105
4106
4107
4108
4109
4110
4111

011556
011556
011556 004737 005510

011562
011562 104404

011564 004737 007006

011570 012737 125252 002342
011576 004737 006672
011602 001404
011604
011604 104455
011606 000004
011610 002631
011612 005020
011614
011614
011614 104405

BGNTST
15:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR

BGNSEG
TRAP C\$BSEG

:SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
:MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.

JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0

:LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH AN ALTERNATING ONES
:AND ZEROES DATA PATTERN (125252) BY ISSUING A WRITE AND READ COMMAND
:TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN CONTROL REGISTER 0.

MOV #125252,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 1\$;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL 125252
TRAP C\$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
1\$: ENDSEG
10000\$: TRAP C\$ESEG

```

4112
4113 011616          BGNSEG
4114 011616 104404  TRAP   C$BSEG
4115
4116                ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH AN ALTERNATING
4117                ;ZEROES AND ONES DATA PATTERN (052525) BY ISSUING A WRITE AND READ
4118                ;COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN CONTROL REG 0.
4119
4120 011620 012737 052525 002342  MOV   #052525,R6LOAD      ;SETUP DATA PATTERN TO BE LOADED
4121 011626 004737 006672          JSR   PC,LDRDR6          ;GO LOAD, READ AND CHECK MODE REGISTER
4122 011632 001404          BEQ   2$                ;IF LOADED OK THEN CONTINUE
4123 011634          ERRDF  4,MODREG,R06ERR      ;MODE REGISTER NOT EQUAL 052525
4124 011634 104455  TRAP   C$ERDF
4125 011636 000004  .WORD  4
4126 011640 002631  .WORD  MODREG
4127 011642 005020  .WORD  R06ERR
4128 011644          2$:  ENDSEG
4129 011644          10001$:
4130 011644 104405  TRAP   C$ESEG
4131
4132 011646          L10041:  ENDTST
4133 011646          TRAP   C$ETST
4134 011646 104401
4135

```


TEST 16: MODE REG 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

.SBTTL TEST 16: MODE REG 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

```

:++
: THIS TEST WILL CHECK THE LOW BYTE OF THE MODE REGISTER USING A BINARY COUNT
: PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE
: PATTERN 377 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED
: ARE MR BITS 7:0. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1
: IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER
: 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND
: WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
: THE MODE REGISTER VIA THE SIGNAL RPT4 L.
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 4183

```

011650
011650
004737 005510
011654 005037 002342
011660
011660 104404
011662 004737 007006
011666 004737 006672
011672 001404
011674 104455
011676 000004
011700 002631
011702 005020
011704
011704 104405
011706 005237 002342
011712 032737 000400 002342
011720 001757
011722
011722
011722 104401
  
```

```

T16:: BGNST
      JSR    PC,INITTE           ;SELECT AND INITIALIZE TARGET EMULATOR
      CLR    R6LOAD             ;START INITIAL PATTERN AT 0

1$:   BGNSEG
      TRAP   C$BSEG

      ;SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
      ;MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.

      JSR    PC,$LMDR          ;GO SELECT MODE REG VIA GDAL BITS 2:0

      ;LOAD, READ AND CHECK MODE REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
      ;THE HIGH BYTE OF THE MODE REGISTER WILL BE CHECKED TO CONTAIN ZEROES
      ;DURING THIS TEST.

      JSR    PC,$LDRDR6        ;GO LOAD, READ AND CHECK THE MODE REG
      BEQ    2$                ;IF LOADED OK THEN CONTINUE
      ERRDF  4,MODREG,R06ERR   ;MODE REG NOT EQUAL EXPECTED
      TRAP   C$ERRDF
      .WORD  4
      .WORD  MODREG
      .WORD  R06ERR

2$:   ENDSEG
10000$: TRAP   C$ES;
      INC    R6LOAD
      BIT    #MR8,R6LOAD      ;UPDATE TEST PATTERN BY ONE
      BEQ    1$                ;CHECK IF TEST PATTERN DONE
      ENDTST                    ;IF NOT THEN LOAD NEXT PATTERN

L10042: TRAP   C$ETST
  
```

TEST 17: MODE REG 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

.SBTTL TEST 17: MODE REG 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

:++
: THIS TEST WILL CHECK THE HIGH BYTE OF THE MODE REGISTER USING A BINARY COUNT
: PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE
: PATTERN 177400 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED
: ARE MR BITS 15:8. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1
: IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER
: 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND
: WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
: THE MODE REGISTER VIA THE SIGNAL RPT4 L.
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011724 004737 005510
011730 005037 002342
011734 104404
011736 004737 007006
011742 004737 006672
011746 001404
011750 104455
011752 000004
011754 002631
011756 005020
011760
011760 104405
011762 062737 000400 002342
011770 001361
011772
011772 104401

BGNTST
T17:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
CLR R6LOAD ;START INITIAL PATTERN AT 0
1\$: BGNSEG
TRAP C\$BSEG
;SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
;MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.
JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0
;LOAD, READ AND CHECK MODE REGISTER BITS 15:8 WITH BINARY COUNT PATTERN
;THE LOW BYTE OF THE MODE REGISTER WILL BE CHECKED TO CONTAIN ZEROES
;DURING THIS TEST.
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK THE MODE REG
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REG NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
2\$: ENDSEG
10000\$: TRAP C\$ESEG
ADD #MR8,R6LOAD ;UPDATE THE HIGH BYTE BY 1
BNE 1\$;IF PATTERN NOT DONE THEN LOAD NEXT
ENDTST
L10043: TRAP C\$ETST

TEST 18: FDAL 7:0 REG TEST (1'S AND 0'S)

.SBTTL TEST 18: FDAL 7:0 REG TEST (1'S AND 0'S)

```

:++
: THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE SET TO ALL ONES (377)
: AND THEN TO ALL ZEROES (000). TO SELECT THE FDAL REGISTER, THE TEST WILL SET
: GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER
: 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H.
: ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL
: REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER,
: WILL BE IGNORED DURING THIS TEST.
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4243 011774
4244 011774
4245 011774 004737 005510
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4247 012000
4248 012000 104404
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4251
4252
4253 012002 004737 007154
4254
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4259 012006 012737 177400 002346
4260 012014 012737 000377 002342
4261 012022 004737 006672
4262 012026 001404
4263 012030
4264 012030 104455
4265 012032 000004
4266 012034 002653
4267 012036 005020
4268 012040
4269 012040
4270 012040 104405
4271
  
```

```

T18:: BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
      ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
      JSR    PC,SLFDAL          ;GE SELECT FDAL REG VIA GDAL BITS 2:0
      ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
      ;ONES (377) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
      ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
      MOV    #177400,R6MASK      ;SETUP TO IGNORE HIGH BYTE
      MOV    #377,R6LOAD        ;SETUP DATA TO BE LOADED
      JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK FDAL REG
      BEQ    1$                 ;IF DATA LOADED OK THEN CONTINUE
      ERRDF 4,FDALRG,R06ERR     ;FDAL REGISTER NOT EQUAL TO 377
      TRAP   C$ERDF
      .WORD 4
      .WORD FDALRG
      .WORD R06ERR
1$:   ENDSEG
10000$: TRAP   C$ESEG
  
```

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4272
4273 012042
4274 012042 104404
4275
4276
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4279
4280 012044 005037 002342
4281 012050 004737 006672
4282 012054 001404
4283 012056
4284 012056 104455
4285 012060 000004
4286 012062 002653
4287 012064 005020
4288 012066
4289 012066
4290 012066 104405
4291
4292 012070
4293 012070
4294 012070 104401
4295

      BGNSEG
      TRAP  C$BSEG

      ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
      ;ZEROES (000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
      ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.

      CLR  R6LOAD          ;SETUP DATA TO BE LOADED
      JSR  PC,LDRDR6      ;GO LOAD, READ AND CHECK FDAL REG
      BEQ  2$              ;IF DATA LOADED OK THEN CONTINUE
      ERRDF 4,FDALRG,R06ERR ;FDAL REGISTER NOT EQUAL TO 000
      TRAP C$ERDF
      .WORD 4
      .WORD FDALRG
      .WORD R06ERR
      2$: ENDSEG
      10001$:
      L10044:
      TRAP C$ESEG
      TRAP C$SESEG
      TRAP C$SETST
  
```

TEST 19: FDAL 7:0 REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 19: FDAL 7:0 REG TEST (1'S + 0'S, 0'S + 1'S)

;++
: THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (125). TO SELECT THE FDAL REGISTER, THE TEST WILL SET THE SIGNAL GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER, WILL BE IGNORED DURING THIS TEST.
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012072
012072
012072 004737 005510
012076
012076 104404
012100 004737 007154
012104 012737 177400 002346
012112 012737 000252 002342
012120 004737 006672
012124 001404
012126
012126 104455
012130 000004
012132 002653
012134 005020
012136
012136
012136 104405

BGNTST
T19:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C\$BSEG
;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
JSR PC.SLFDAL ;GO SELECT FDAL REG VIA GDAL BITS 2:0
;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
MOV #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE
MOV #252,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK FDAL REG
BEQ 1\$;IF DATA LOADED OK THEN CONTINUE
ERRDF 4,FDALRG,R06ERR ;FDAL REGISTER NOT EQUAL TO 252
TRAP C\$ERDF
.WORD 4
.WORD FDALRG
.WORD R06ERR
1\$: ENDSEG
10000\$: TRAP C\$ESEG

```
4338
4339 012140          BGNSEG
4340 012140 104404  TRAP   C$BSEG
4341
4342                ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH AN ALTERNATING ZEROES
4343                ;AND ONES DATA PATTERN (125) BY ISSUING A WRITE AND READ COMMAND TO
4344                ;CONTROL REGISTER 6 WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
4345
4346 012142 012737 000125 002342  MOV   #125,R6LOAD      ;SETUP DATA TO BE LOADED
4347 012150 004737 006672          JSR   PC,LDRDR6        ;GO LOAD, READ AND CHECK FDAL REG
4348 012154 001404          BEQ   2$              ;IF DATA LOADED OK THEN CONTINUE
4349 012156          ERRDF 4,FDALRG,R06ERR  ;FDAL REGISTER NOT EQUAL TO 125
4350 012156 104455  TRAP   C$ERDF
4351 012160 000004          .WORD 4
4352 012162 002653          .WORD FDALRG
4353 012164 005020          .WORD R06ERR
4354 012166          2$:  ENDSEG
4355 012166          10001$:
4356 012166 104405  TRAP   C$ESEG
4357
4358 012170          L10045:  ENDTST
4359 012170          TRAP   C$ETST
4360 012170 104401
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```

TEST 20: FDAL 7:0 REG TEST USING BINARY COUNT

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 4400
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012172
 012172
 012172 004737 005510
 012176 005037 002342
 012202 012737 177400 002346
 012210
 012210 104404
 012212 004737 007154
 012216 004737 006672
 012222 001404
 012224 104455
 012226 000004
 012230 002653
 012232 005020
 012234
 012234 104405
 012236 105237 002342
 012242 001362
 012244
 012244 104401

.SBTTL TEST 20: FDAL 7:0 REG TEST USING BINARY COUNT

```

:++
: THIS TEST WILL CHECK FDAL REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE
: TEST PATTERN WILL START AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS
: BEEN LOADED INTO THE FDAL REGISTER. TO SELECT THE FDAL REGISTER, THE TEST
: WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL
: REGISTER 6, DATA WILL BE LOADED INTO THE FDAL REG VIA THE SIGNAL WPT2 LB H.
: ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE FDAL REG
: VIA THE SIGNAL RPT2 L.
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T20:: BGNTST
      JSR    PC,INITTE      ;SELECT AND INITIALIZE TARGET EMULATOR
      CLR    R6LOAD        ;SET STARTING PATTERN TO ZERO
      MOV    #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE ON READ

1$:   BGNSEG
      TRAP   C$BSEG

      ;SET GDAL1 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER
      ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

      JSR    PC,SLFDAL     ;GO SELECT FDAL REG VIA GDAL BITS 2:0

      ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
      ;FROM 0 TO 377 BY AN INCREMENT OF ONE.

      JSR    PC,LDRDR6     ;GO LOAD, READ AND CHECK FDAL REG
      BEQ    2$            ;IF LOADED OK THEN CONTINUE
      ERDF   4,FDALRG,R06ERR ;FDAL REG NOT EQUAL EXPECTED (0-377)
      TRAP   C$ERDF

      .WORD  4
      .WORD  FDALRG
      .WORD  R06ERR

2$:   ENDSEG
10000$: TRAP   C$ESEG
      INCB  R6LOAD        ;UPDATE TEST PATTERN BY ONE
      BNE   1$           ;IF NOT 0 THEN LOAD NEXT PATTERN

      ENDTST

L10046: TRAP   C$ETST
  
```

TEST 21: EOAI 7:0 REG TEST USING BINARY COUNT

.SBTTL TEST 21: EOAI 7:0 REG TEST USING BINARY COUNT

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:++
: THIS TEST WILL CHECK EOAI REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE
: TEST PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL A PATTERN OF ALL
: ONES HAS BEEN LOADED INTO THE EOAI REGISTER AND CHECKED. THE EOAI REGISTER IS
: THE HIGH BYTE OF THE FDAL REGISTER. DATA IS LOADED INTO THE EOAI REGISTER VIA
: THE SIGNAL WPT2 HB H WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
: THE FDAL REGISTER IS SELECTED VIA GDAL BITS 2:0. TO READ THE EOAI BUS, THE
: PROGRAM WILL SET FDALO H TO A ONE TO SELECT THE EOAI BUS TO BE READ INSTEAD OF
: THE CTL BUS. THE EOAI BUS IS READ BACK TO THE LSI-11 VIA THE SIGNAL RAT2 L
: WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS
: SELECTED.
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012246
012246
012246 004737 00551C
012252 012737 000001 002342
012260
012260 104404
012262 004737 007154
012266 004737 006672
012272 001404
012274
012274 104455
012276 000004
012300 002676
012302 005020
012304
012304 10000$
012304 104405
012306 062737 000400 002342
012314 103361
012316
012316
012316 104401
  
```

```

BGNTST
T21:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
      MOV #FDALO,R6LOAD ;SETUP EOAI FDAL ENABLES + DATA PATTERN
1$: BGNSEG
     TRAP C$BSEG
;SELECT FDAL REGISTER BY SETTING GDAL1 H TO A ONE AND GDAL BITS 2 AND 0
;TO ZEROES IN CONTROL REGISTER 0.
JSR PC,$LFDAL ;SELECT FDAL AND EOAI REG VIA GDAL 2:0
;LOAD, READ AND CHECK EOAI REGISTER BITS 7:0 WITH THE BINARY COUNT DATA
;PATTERN. THE EOAI REGISTER IS THE HIGH BYTE OF THE FDAL REGISTER. THE
;DATA PATTERN WILL BE LOADED VIA THE SIGNAL WPT2 HB H WHEN A WRITE
;COMMAND IS ISSUED TO CONTROL REGISTER 6. FDAL REGISTER BIT 0 WILL ALSO
;BE WRITTEN INTO THE FDAL REGISTER ON THE WRITE COMMAND TO CONTROL
;REGISTER 6. THE EOAI REGISTER WILL BE READBACK VIA THE SIGNAL RAT2 L WHEN
;A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL FDALO H IS
;SET TO A ONE. THE SIGNAL FDALO H ON A ONE WILL CAUSE THE EOAI BUS TO BE
;READBACK ON THE READ COMMAND INSTEAD OF THE CTL 7:0 BUS.
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK FDAL + EOAI
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,EOAIFD,R06ERR ;EOAI REG OR FDAL REG ERROR
TRAP C$ERDF
.WORD 4
.WORD EOAIFD
.WORD R06ERR
2$: ENDSEG
10000$: TRAP C$ESEG
ADD #BIT8,R6LOAD ;UPDATE EOAI PATTERN BY ONE
BCC 1$ ;IF NOT DONE LOAD NEXT PATTERN
ENDTST
L10047: TRAP C$ETST
  
```


TEST 22: DIAG ADDR 15:0 REG TEST (1'S AND 0'S)

.SBTTL TEST 22: DIAG ADDR 15:0 REG TEST (1'S AND 0'S)

:++
: THIS TEST WILL CHECK THAT THE DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN
: BE LOADED WITH ALL ONES (177777) AND THEN ALL ZEROES (000000).

: TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
: BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
: IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
: SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND
: TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
: WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAG-
: NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
: 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
: WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
: AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
: ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
: NOSTIC ADDRESS REGISTER.
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012320
012320
012320 004737 005510
012324
012324 104404
012326 004737 006754
012332 012737 001000 002342
012340 004737 006672
012344 001405
012346 104455
012350 000004
012352 002605
012354 005020
012356 104406

T22:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C\$BSEG
;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL BITS 2:0
;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ
;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
;ISTER VIA THE SIGNAL RPT3 L.
MOV #HDAL9,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REG
BEQ 1\$;IF DATA LOADED OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL 1000
TRAP C\$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLCOP
TRAP C\$CLP1
;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
1\$: JSR PC,SLDADR ;SELECT DIAG ADDRESS REG VIA GDAL 2:0
;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A
;DATA PATTERN OF 177777. ON A WRITE COMMAND TO CONTROL REGISTER 6

```
4518 ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4519 ;ADDRESS REGISTER VIA THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ
4520 ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4521 ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPT0 L. PREVIOUSLY IN THIS
4522 ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4523 ;BITS ONTO THE ADDRESS BUS.
4524
4525 012364 012737 177777 002342 MOV #177777,R6LOAD ;SETUP DATA TO BE LOADED
4526 012372 004737 006672 JSR PC,LDRDR6 ;LOAD READ AND CHECK DIAG ADDRESS REG
4527 012376 001404 BEQ 2$ ;IF LOADED OK THEN CONTINUE
4528 012400 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDR REG NOT EQUAL 177777
4529 012400 104455 TRAP C$ERDF
4530 012402 000004 .WORD 4
4531 012404 002735 .WORD ADDRRG
4532 012406 005020 .WORD R06ERR
4533 012410 2$: ENDSEG
4534 012410 10000$:
4535 012410 104405 TRAP C$ESEG
4536
4537 012412 BGNSEG
4538 012412 104404 TRAP C$BSEG
4539
4540 ;LOAD, READ AND CHECK DAIGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A DATA
4541 ;PATTERN OF 000000. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL
4542 ;BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC ADDRESS
4543 ;REGISTER VIA THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND
4544 ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAGNOSTIC
4545 ;ADDRESS REGISTER VIA THE SIGNAL RPT0 L. PREVIOUSLY IN THIS TEST, HDAL9
4546 ;WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE
4547 ;ADDRESS BUS
4548
4549 012414 005037 002342 CLR R6LOAD ;SETUP DATA TO BE LOADED
4550 012420 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK ADDRESS REG
4551 012424 001404 BEQ 3$ ;IF DATA LOADED OK THEN CONTINUE
4552 012426 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDR REG NOT EQUAL 000000
4553 012426 104455 TRAP C$ERDF
4554 012430 000004 .WORD 4
4555 012432 002735 .WORD ADDRRG
4556 012434 005020 .WORD R06ERR
4557 012436 3$: ENDSEG
4558 012436 10001$:
4559 012436 104405 TRAP C$ESEG
4560 012440 ENDTST
4561 012440 L10050:
4562 012440 104401 TRAP C$ETST
4563
```

TEST 23: DIAG ADDR 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

.SBTTL TEST 23: DIAG ADDR 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

```

:++
: THIS TEST WILL CHECK THAT THE DAIGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN
: BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATERRN (125252) AND AN
: ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
:
: TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
: BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
: IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
: SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND
: TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
: WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAG-
: NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
: 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
: WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
: AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
: ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
: NOSTIC ADDRESS REGISTER.
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012442 004737 005510
012446
012446 104404
012450 004737 006754
012454 012737 001000 002342
012462 004737 006672
012466 001405
012470
012470 104455
012472 000004
012474 002605
012476 005020
012500
012500 104406
012502 004737 007072
  
```

```

T23:: BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
      ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
      JSR    PC,SLHDAL         ;GO SELECT HDAL REG VIA GDAL BITS 2:0
      ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
      ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
      ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ
      ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
      ;ISTER VIA THE SIGNAL RPT3 L.
      MOV    #HDAL9,R6LOAD     ;SETUP DATA TO BE LOADED
      JSR    PC,LDRDR6         ;GO LOAD, READ AND CHECK HDAL REG
      BEQ    1$                ;IF DATA LOADED OK THEN CONTINUE
      ERDF   4,HDALRG,R06ERR   ;HDAL REGISTER NOT EQUAL 1000
      TRAP   C$ERDF
      .WORD  4
      .WORD  HDALRG
      .WORD  R06ERR
      CKLOOP
      TRAP   C$CLP1
      ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
      ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
      1$: JSR    PC,SLDADR         ;SELECT DIAG ADDRESS REG VIA GDAL 2:0
      ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A
  
```

TEST 23: DIAG ADDR 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

```

4620                                     :DATA PATTERN OF 125252. ON A WRITE COMMAND TO CONTROL REGISTER 6
4621                                     :WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4622                                     :ADDRESS REGISTER VIA THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ
4623                                     :COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4624                                     :NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPT0 L. PREVIOUSLY IN THIS
4625                                     :TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4626                                     :BITS ONTO THE ADDRESS BUS.
4627
4628 012506 012737 125252 002342      MOV      #125252,R6LOAD      ;SETUP DATA TO BE LOADED
4629 012514 004737 006672              JSR      PC,LDRDR6         ;LOAD READ AND CHECK DIAG ADDRESS REG
4630 012520 001404                      BEQ      2$                ;IF LOADED OK THEN CONTINUE
4631 012522                                ERRDF    4,ADDRRG,R06ERR   ;DIAG ADDR REG NOT EQUAL 125252
4632 012522 104455                      TRAP    C$ERDF
4633 012524 000004                      .WORD   4
4634 012526 002735                      .WORD   ADDRRG
4635 012530 005020                      .WORD   R06ERR
4636 012532                                ENDSEG
4637 012532                                2$:
4638 012532 104405                        10000$:
4639                                     TRAP    C$ESEG
4640 012534                                BGNSEG
4641 012534 104404                        TRAP    C$BSEG
4642
4643                                     :LOAD, READ AND CHECK DAIGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A DATA
4644                                     :PATTERN OF 052525. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL
4645                                     :BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC ADDRESS
4646                                     :REGISTER VIA THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND
4647                                     :TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAGNOSTIC
4648                                     :ADDRESS REGISTER VIA THE SIGNAL RPT0 L. PREVIOUSLY IN THIS TEST, HDAL9
4649                                     :WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE
4650                                     :ADDRESS BUS
4651
4652 012536 012737 052525 002342      MOV      #052525,R6LOAD   ;SETUP DATA PATTERN TO BE LOADED
4653 012544 004737 006672              JSR      PC,LDRDR6         ;GO LOAD, READ AND CHECK ADDRESS REG
4654 012550 001404                      BEQ      3$                ;IF DATA LOADED OK THEN CONTINUE
4655 012552                                ERRDF    4,ADDRRG,R06ERR   ;DIAG ADDR REG NOT EQUAL 052525
4656 012552 104455                      TRAP    C$ERDF
4657 012554 000004                      .WORD   4
4658 012556 002735                      .WORD   ADDRRG
4659 012560 005020                      .WORD   R06ERR
4660 012562                                ENDSEG
4661 012562                                3$:
4662 012562 104405                        10001$:
4663 012564                                TRAP    C$ESEG
4664 012564                                ENDTST
4665 012564 104401                        L10051:
4666                                     TRAP    C$ETST

```

TEST 24: DIAG ADDR 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

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012566
012566
012566 004737 005510
012572 005001

012574
012574 104404

012576 004737 006754

012602 012737 001000 002342
012610 004737 006672
012614 0C1405
012616
012616 104455
012620 000004
012622 002605
012624 005020
012626
012626 104406

.SBTTL TEST 24: DIAG ADDR 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

..**
 : THIS TEST WILL CHECK THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A
 : BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE
 : UNTIL THE PATTERN 377 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS
 : ADDR 7:0. THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED
 : WITH ZEROES DURING THIS TEST.

..--
 : TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
 : BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
 : IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
 : SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND
 : TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
 : WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAG-
 : NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
 : 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
 : WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
 : AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
 : ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
 : NOSTIC ADDRESS REGISTER.

```

T24::  BGNTST
      JSR    PC,INITTE      ;SELECT AND INITIALIZE TARGET EMULATOR
      CLR    R1             ;SET DATA PATTERN INITIALLY TO 0

1$:   BGNSEG
      TRAP   C$BSEG

      ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
      ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

      JSR    PC,SLHDAL      ;GO SELECT HDAL REG VIA GDAL BITS 2:0

      ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
      ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
      ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ
      ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
      ;ISTER VIA THE SIGNAL RPT3 L.

      MOV    #HDAL9,R6LOAD  ;SETUP DATA TO BE LOADED
      JSR    PC,LDRDR6      ;GO LOAD, READ AND CHECK HDAL REG
      BEQ    2$             ;IF DATA LOADED OK THEN CONTINUE
      ERDF   4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL 1000
      TRAP   C$ERDF

      .WORD  4
      .WORD  HDALRG
      .WORD  R06ERR
      CKLOOP
      TRAP   C$CLP1
  
```

```

4720
4721
4722 ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
4723 ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
4724 012630 004737 007072 2$: JSR PC,SLDADR ;SELECT DIAG ADDRESS REG VIA GDAL 2:0
4725
4726 ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 7:0 WITH THE
4727 ;BINARY COUNT PATTERN (0-377). ON A WRITE COMMAND TO CONTROL REGISTER 6
4728 ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4729 ;ADDRESS REGISTER VIA THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ
4730 ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4731 ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPT0 L. PREVIOUSLY IN THIS
4732 ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4733 ;BITS ONTO THE ADDRESS BUS.
4734
4735 012634 010137 002342 MOV R1,R6LOAD ;SETUP DATA TO BE LOADED
4736 012640 004737 006672 JSR PC,LDRDR6 ;LOAD READ AND CHECK DIAG ADDRESS REG
4737 012644 001404 BEQ 3$ ;IF LOADED OK THEN CONTINUE
4738 012646 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDR REG NOT EQUAL 125252
4739 012646 104455 TRAP C$ERDF
4740 012650 000004 .WORD 4
4741 012652 002735 .WORD ADDRRG
4742 012654 005020 .WORD R06ERR
4743 012656 3$: ENDSEG
4744 012656 10000$: TRAP C$ESEG
4745 012656 104405 INCB R1 ;UPDATE THE TEST PATTERN BY ONE
4746 012660 105201 BNE 1$ ;IF NOT 0 THEN LOAD NEXT PATTERN
4747 012662 001344 ENDTST
4748 012664
4749 012664
4750 012664 104401 TRAP C$ETST
4751

```

TEST 25: DIAG ADDR 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

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4802
4803
4804

012666
012666
012666 004737 005510
012672 005001
012674
012674 104404
012676 004737 006754
012702 012737 001000 002342
012710 004737 006672
012714 001405
012716
012716 104455
012720 000004
012722 002605
012724 005020
012726
012726 104406

.SBTTL TEST 25: DIAG ADDR 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

++
 : THIS TEST WILL CHECK THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A
 : BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400
 : UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS
 : ADDR 15:8. THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED
 : WITH ZEROES DURING THIS TEST.

: TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
 : BUS AND TO DISABLE THE HDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
 : IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
 : SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND
 : TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
 : WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAG-
 : NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
 : 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
 : WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
 : AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
 : ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
 : NOSTIC ADDRESS REGISTER.

--
 T25:: BGNTST
 JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
 CLR R1 ;SET DATA PATTERN INITIALLY TO 0

1\$: BGNSEG
 TRAP CSBSEG
 :SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
 :REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
 JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL BITS 2:0
 :LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
 :ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
 :THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ
 :COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
 :ISTER VIA THE SIGNAL RPT3 L.

MOV #HDAL9,R6LOAD ;SETUP DATA TO BE LOADED
 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REG
 BEQ 2\$;IF DATA LOADED OK THEN CONTINUE
 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL 1000
 TRAP CSERDF
 .WORD 4
 .WORD HDALRG
 .WORD R06ERR
 CKLOOP
 TRAP CSCLP1

```
4805
4806
4807 ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
4808 ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
4809 012730 004737 007072 2$: JSR PC,SLDADR ;SELECT DIAG ADDRESS REG VIA GDAL 2:0
4810
4811 ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:8 WITH THE
4812 ;BINARY COUNT PATTERN (400-177400). ON A WRITE COMMAND TO CONTROL REG 6
4813 ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4814 ;ADDRESS REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H. ON A READ
4815 ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4816 ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPTO L. PREVIOUSLY IN THIS
4817 ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4818 ;BITS ONTO THE ADDRESS BUS.
4819
4820 012734 010137 002342 MOV R1,R6LOAD ;SETUP DATA TO BE LOADED
4821 012740 004737 006672 JSR PC,LDRDR6 ;LOAD READ AND CHECK DIAG ADDRESS REG
4822 012744 001404 BEQ 3$ ;IF LOADED OK THEN CONTINUE
4823 012746 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDR REG NOT EQUAL 125252
4824 012746 104455 TRAP C$ERDF
4825 012750 000004 .WORD 4
4826 012752 002735 .WORD ADDRRG
4827 012754 005020 .WORD R06ERR
4828 012756 3$: ENDSEG
4829 012756 10000$:
4830 012756 104405 TRAP C$ESEG
4831 012760 062701 000400 ADD #ADDR8,R1 ;UPDATE TEST PATTERN BY 400
4832 012764 001343 BNE 1$ ;IF NOT 0 THEN LOAD NEXT PATTERN
4833 012766 ENDTST
4834 012766 L10053:
4835 012766 104401 TRAP C$ETST
4836
```


TEST 26: READBACK MODE REG ON EODAL 15:0 BUS

.SBTTL TEST 26: READBACK MODE REG ON EODAL 15:0 BUS

```

:++
: THIS TEST WILL CHECK THAT THE MODE REGISTER CAN BE READBACK ON THE EODAL BUS.
: THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING PATTERNS: 125252,052525,
: 177400, 000377, 177777, AND 000000. FOR EACH PATTERN LOADED THE TEST
: WILL ENABLE THE MODE REGISTER ONTO THE EODAL BUS AND READ AND CHECK THE EODAL
: BUS FOR THE CORRECT MODE REGISTER PATTERN. THE MODE REGISTER WILL BE ENABLED
: TO THE EODAL BUS WHEN ADAL12 H IS SET TO A ONE AND THE SIGNAL XBCLR H IS
: ASSERTED HIGH.
:--
  
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012770
012770
012770 004737 005510
012774 012701 013220
013000 012702 000006

013004
013004 104404

013006 004737 006754

013012 005037 002342
013016 004737 007620

013022 004737 007006

013026 011137 002342
013032 004737 006672
013036 001405
013040
013040 104455
013042 000004
013044 002631
013046 005020
013050
013050 104406
  
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BGNTST
T26::
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #7$,R1 ;GET ADDRESS OF STARTING DATA PATTERN
MOV #6,R2 ;COUNTER FOR NUMBER OF PATTERNS

1$:
BGNSEG
TRAP C$BSEG
;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
;LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL7 H AND HDAL2 H SET TO
;ONES. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11
;TIMING AND CONTROL SIGNALS. HDAL7 H ON A ONE WILL CAUSE THE SIGNALS
;PBCLR H AND XBCLR H TO BE ASSERTED HIGH.
CLR R6LOAD ;SETUP TO CLEAR ALL OTHER HDAL BITS
JSR PC,XBCLRH ;SET XBCLR H (HIGH) AND HDAL2 H TO A 1
;SELECT THE MODE REGISTER BY SETTING GDAL2 H TO A ONE AND GDAL BITS
;1 AND 0 TO ZEROES. THE MODE REGISTER WILL BE SELECTED ON A WRITE OR
;READ COMMAND TO CONTROL REGISTER 6.
JSR PC,SLMODR ;SELECT MODE REG VIA GDAL BITS 2:0
;LOAD, READ AND CHECK MODE REGISTER WITH ONE OF THE FOLLOWING DATA
;PATTERNS: 125252, 052525, 177400, 000377, 177777, AND 000000.
MOV (R1),R6LOAD ;GET A DATA PATTERN FROM TABLE
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REG NOT EQUAL TO EXPECTED
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C$CLP1

;SET ADAL12 H TO A ONE IN ADAL REGISTER. WHEN ADAL12 H IS SET TO A ONE
;AND THE SIGNAL XBCLR H IS ASSERTED HIGH, THE MODE REGISTER WILL BE
;ENABLED TO THE EODAL BUS.
  
```

```

4893
4894 013052 012737 010000 002330 2$: MOV #ADAL2,R2LOAD ;SETUP ADAL BITS TO BE LOADED
4895 013060 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
4896 013064 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
4897 013066 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
4898 013066 104455 TRAP C$ERDF
4899 013070 000002 .WORD 2
4900 013072 002513 .WORD ADALRG
4901 013074 004770 .WORD R2EROR
4902 013076 CKLOOP
4903 013076 104406 TRAP C$CLP1
4904
4905 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. AT THIS POINT
4906 ;THE MODE REGISTER WILL BE ENABLED TO THE EODAL BUS. ON A READ COMMAND
4907 ;TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE READBACK TO THE LSI-11
4908 ;TROUGH THE EODAL BUS
4909
4910 013100 004737 007122 3$: JSR PC,SEODAL ;SELECT EODAL BUS VIA GDAL BITS 2:0
4911
4912 ;READ AND CHECK THAT THE MODE REGISTER WAS READBACK ON THE LSI-11 BUS
4913 ;THROUGH THE EODAL BUS, WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
4914 ;6. THE MODE REGISTER IS ENABLED TO THE EODAL BUS WHEN THE SIGNAL
4915 ;XBCLR H IS ASSERTED HIGH AND ADAL2 H IS SET TO A ONE.
4916
4917 013104 011137 002342 MOV (R1),R6LOAD ;GET MODE REGISTER DATA PATTERN
4918 013110 004737 006700 JSR PC,READR6 ;GO READ MODE REG ON THE EODAL BUS
4919 013114 001405 BEQ 4$ ;IF DATA = MODE REG THEN CONTINUE
4920 013116 ERRDF 4,MEODAL,R026ER ;MODE REGISTER TO EODAL BUS ERROR
4921 013116 104455 TRAP C$ERDF
4922 013120 000004 .WORD 4
4923 013122 003102 .WORD MEODAL
4924 013124 005034 .WORD R026ER
4925 013126 CKLOOP
4926 013126 104406 TRAP C$CLP1
4927
4928 ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
4929
4930 013130 004737 006754 4$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
4931
4932 ;LOAD, READ AND CHECK THE HDAL REGISTER WITH A DATA PATTERN OF ALL
4933 ;ZEROES. WHEN HDAL2 H IS SET TO A ZERO, THE T-11 WILL PROVIDE THE
4934 ;TIMING AND CONTROL SIGNALS TO THE TARGET EMULATOR MODULE. AT THIS
4935 ;TIME, THE T-11 IS TURNED OFF AS A RESULT OF ADAL2 H BEING A ZERO. WHEN
4936 ;THE T-11 IS TURNED OFF, THE SIGNALS PBCLR H AND XBCLR H WILL BE ASSERTED
4937 ;HIGH. THEREFORE, THE MODE REGISTER SHOULD STILL BE ENABLED TO THE
4938 ;EODAL BUS AS A RESULT OF XBCLR H AND ADAL2 H BEING ASSERTED HIGH.
4939
4940 013134 005037 002342 CLR R6LOAD ;SETUP TO CLEAR ALL HDAL REGISTER BITS
4941 013140 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK THE HDAL REG
4942 013144 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
4943 013146 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4944 013146 104455 TRAP C$ERDF
4945 013150 000004 .WORD 4
4946 013152 002605 .WORD HDALRG
4947 013154 005020 .WORD R06ERR
4948 013156 CKLOOP

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4949 013156 104406          TRAP    C$CLP1
4950
4951                        ;SELECT THE EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
4952
4953 013160 004737 007122    5$:   JSR     PC,SEODAL          ;SELECT EODAL BUS VIA GDAL BITS 2:0
4954
4955                        ;AS A RESULT OF HDAL2 H BEING CLEARED, THE T-11 WILL PROVIDE THE
4956                        ;TIMING AND CONTROL SIGNALS TO THE TARGET EMULATOR MODULE. AT THIS
4957                        ;TIME, THE T-11 IS TURNED OFF BY ADAL2 H BEING A ZERO, THEREFORE,
4958                        ;THE SIGNALS PBCLR H AND XBCLR H WILL BE ASSERTED HIGH. WHEN XBCLR H
4959                        ;AND ADAL2 H ARE ASSERTED HIGH, THE MODE REGISTER WILL BE ENABLED TO
4960                        ;THE EODAL BUS.
4961
4962 013164 011137 002342      MOV     (R1),R6LOAD          ;GET MODE REGISTER DATA PATTERN
4963 013170 004737 006700      JSR     PC,READR6          ;READ THE EODAL BUS FOR MODE REG DATA
4964 013174 001404              BEQ     6$                  ;IF DATA OK THEN CONTINUE
4965 013176              ERRDF  4,MEODAL,R026ER      ;MODE REG TO EODAL BUS ERROR
4966 013176 104455          TRAP    C$ERDF
4967 013200 000004          .WORD  4
4968 013202 003102          .WORD  MEODAL
4969 013204 005034          .WORD  R026ER
4970 013206              6$:   ENDSEG
4971 013206              10000$:
4972 013206 104405          TRAP    C$ESEG
4973
4974 013210 005721          TST     (R1)+              ;UPDATE THE POINTER TO DATA TABLE
4975 013212 005302          DEC     R2                ;CHECK IF ALL PATTERNS TESTED
4976 013214 001273          BNE     1$                ;IF NOT THEN LOAD NEXT PATTERN
4977 013216 000406          BR      8$                ;IF YES THEN END OF TEST
4978
4979 013220 125252          7$:   .WORD  125252
4980 013222 052525          .WORD  052525
4981 013224 177400          .WORD  177400
4982 013226 000377          .WORD  000377
4983 013230 177777          .WORD  177777
4984 013232 000000          .WORD  000000
4985
4986 013234              8$:   ENDTST
4987 013234              L10054:
4988 013234 104401          TRAP    C$ETST
4989

```

TEST 27: WRITE DIAG ADRESS REG INTO FJA READBACK REG (READ VIA RPT1 L)

.SBTTL TEST 27: WRITE DIAG ADRESS REG INTO FJA READBACK REG (READ VIA RPT1 L)

:++
: THIS TEST WILL CHECK THE FORCE JUMP ADDRESS READBACK REGISTER WITH THE FOLLOWING
: DATA PATTERNS 125252, 052525, 177400, 000377, 177777, AND 000000. THE DIAG-
: NOSTIC ADDRESS REGISTER WILL PROVIDE THE DATA ON THE ADDRESS BUS TO THE FORCE
: JUMP ADDRESS REGISTER AND FORCE JUMP ADDRESS READBACK REGISTER.
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013236
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013236 004737 005510
013242 012701 013644
013246 012702 000006

013252
013252 104404

013254 004737 006754

013260 012737 001004 002342
013266 004737 006672
013272 001405
013274
013274 104455
013276 000004
013300 002605
013302 005020
013304
013304 104406

T27:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #10\$,R1 ;GET ADDRESS OF DATA TABLE
MOV #6,R2 ;THE NUMBER OF DATA PATTERNS

1\$: BGNSEG
TRAP C\$BSEG

;SELECT THE HDAL REGISTER BY SETTING GDAL1 AND GDAL0 TO ONES IN
;CONTROL REGISTER 0 GDAL BITS 2:0. ON A WRITE COMMAND OR READ
;COMMAND TO CONTRCL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED.

JSR PC,SLHDAL ;GO SELECT HDAL REG VIA THE GDAL REG

;SET HDAL9 H AND HDAL2 H TO ONES IN THE HDAL REGISTER. HDAL9 H ON A
;ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO
;THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS BUS.
;HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL THE T-11 TIMING
;AND CONTROL SIGNALS. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA
;WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
;WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE
;READBACK FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

MOV #HDAL9!HDAL2,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLOOP
TRAP C\$CLP1

;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
;ZERES. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE
;DIAGNOSTIC ADDRESS REGISTER WILL BE SELECTED.

2\$: JSR PC,SLDADR ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0

;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
;FOLLOWING DATA PATTERNS 125252, 052525, 177400, 000377, 177777 OR
;000000. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED
;INTO THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL WPT0 LB H AND
;WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ-
;BACK FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL RPT0 L.

```
5046 ;PREVIOUSLY IN THIS TEST, HDAL9 H WAS SET TO A ONE TO DISABLE THE EIDAL
5047 ;BUS FROM THE ADDRESS BUS AND ENABLE THE DIAGNOSTIC ADDRESS REGISTER TO
5048 ;THE ADDRESS BUS.
5049
5050 013312 011137 002342 MOV (R1),R6LOAD ;GET THE DATA PATTERN FROM THE TABLE
5051 013316 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK DIAG ADDR REG
5052 013322 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
5053 013324 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5054 013324 104455 TRAP C$ERDF
5055 013326 000004 .WORD 4
5056 013330 002735 .WORD ADDRRG
5057 013332 005020 .WORD R06ERR
5058 013334 CKLOOP
5059 013334 104406 TRAP C$CLP1
5060
5061 ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE. SET
5062 ;AND CLEAR VDAL2 H TO CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS AND OTHER
5063 ;FLIP-FLOPS.
5064
5065 013336 012737 000200 002334 3$: MOV #VDAL7,R4LOAD ;SETUP BIT TO SET FETCT H
5066 013344 004737 007712 JSR PC,CLRPSM ;SET FETCT H AND CLEAR PAUSE STATE F/F'S
5067
5068 ;RESELECT THE HDAL REGISTER VIA THE GDAL REGISTER, SO THAT THE SIGNALS
5069 ;XRAS H AND XRAS L CAN BE PULSED BY SETTING AND CLEARING HDAL12 H.
5070
5071 013350 004737 006754 JSR PC,SLHDAL ;GO SELECT HDAL REG VIA THE GDAL REG
5072
5073 ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING THE SIGNAL
5074 ;HDAL12 H. THE SIGNAL XRAS H WILL CLOCK THE STATE OF FETCT H INTO THE
5075 ;EDFET FLIP-FLOP, THUS SETTING EDFET H TO A ONE. THE SIGNAL XRAS H WILL
5076 ;CAUSE THE SIGNAL RASP H TO PULSE. WHEN THE EDFET FLIP-FLOP IS SET TO A
5077 ;ONE AND THE SIGNAL RASP H IS PULSED, A PULSE WILL BE ISSUED
5078 ;ON THE SIGNAL DFET H. THE SIGNAL DFET H WILL CLOCK THE DIAGNOSTIC
5079 ;ADDRESS REGISTER WHICH IS ENABLED TO THE ADDRESS BUS INTO THE OLD FORCE
5080 ;JUMP ADDRESS REGISTER AND THE FORCE JUMP ADDRESS READBACK REGISTER.
5081
5082 013354 012737 001004 002342 MOV #HDAL9!HDAL2,R6LOAD ;RESET PREVIOUS CONTENTS OF HDAL REG
5083 013362 004737 007272 JSR PC,XRAS ;GO PULSE XRAS L AND XRAS H VIA HDAL12 H
5084
5085 ;ADAL4 H WAS SET TO A ZERO AT THE BEGINNING OF THIS TEST IN THE ROUTINE
5086 ;"INITTE". PULSING THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H (0)
5087 ;INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE
5088 ;HIGH STATE (1). THE SIGNAL PAUSE L BEING ASSERTED HIGH WILL CAUSE THE
5089 ;SIGNAL SOP H TO BE ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED
5090 ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE,
5091 ;THUS SETTING THE SIGNAL PSMW H TO THE HIGH STATE. THE SIGNAL PSMW H
5092 ;IS READ IN VDAL REGISTER AS VDAL9 H.
5093
5094 013366 052737 001000 002336 BIS #VDAL9,R4GOOD ;SETUP TO EXPECT PSMW H TO BE A 1
5095 013374 004737 006654 JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
5096 013400 001405 BEQ 4$ ;IF OK THEN CONTINUE
5097 013402 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
5098 013402 104455 TRAP C$ERDF
5099 013404 000003 .WORD 3
5100 013406 002537 .WORD VDALRG
5101 013410 005004 .WORD R4EROR
```

TEST 27: WRITE DIAG ADRESS REG INTO FJA READBACK REG (READ VIA RPT1 L)

```
5102 013412          CKLOOP
5103 013412 104406  TRAP  C$CLP1
5104
5105                ;SELECT THE FORCE JUMP ADDRESS REGISTER BY SETTING GDALO H TO A ONE
5106                ;AND GDAL1 H AND GDAL2 H TO ZEROES.  ON A READ COMMAND TO CONTROL
5107                ;REGISTER 6, THE FORCE JUMP ADDRESS READBACK REGISTER WILL BE READBACK
5108                ;VIA THE SIGNAL RPT1 L.
5109
5110 013414 004737 007040 4$: JSR  PC,SLFJAR          ;GO SELECT FJA REG VIA GDAL REG
5111
5112                ;READ THE FORCE JUMP ADDRESS READBACK REGISTER TO CHECK THAT THE DIAG-
5113                ;NOSTIC ADDRESS REGISTER DATA WAS LOADED INTO IT WHEN THE SIGNAL RASP H
5114                ;WAS PULSED WITH THE FLIP-FLOP EDFET H SET TO A ONE.  THE FORCE JUMP ADDRESS
5115                ;READBACK REGISTER IS LOADED BY THE SIGNAL DFET H.
5116
5117 013420 011137 002342  MOV  (R1),R6LOAD      ;GET PATTERN LOADED INTO DIAG ADDR REG
5118 013424 004737 006700  JSR  PC,READR6      ;GO READ FORCE JUMP ADDRESS READBACK REG
5119 013430 001405          BEQ  5$              ;IF DATA OK THEN CONTINUE
5120 013432          ERRDF 4,FJADRG,R06ERR      ;FJA READBACK REG NOT = DIAG ADDRESS REG
5121 013432 104455          TRAP  C$ERDF
5122 013434 000004          .WORD 4
5123 013436 002766          .WORD FJADRG
5124 013440 005020          .WORD R06ERR
5125 013442          CKLOOP
5126 013442 104406          TRAP  C$CLP1
5127
5128                ;RESELECT THE DIAGNOSTIC ADDRESS REGISTER VIA THE GDAL BITS
5129
5130 013444 004737 007072 5$: JSR  PC,SLDADR          ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0
5131
5132                ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA
5133                ;PATTERN OF 031463.
5134
5135 013450 012737 031463 002342  MOV  #031463,R6LOAD  ;SETUP DATA PATTERN TO BE LOADED
5136 013456 014737 006672  JSR  PC,LDRDR6      ;GO LOAD, READ AND CHECK DIAG ADDR REG
5137 013462 001405          BEQ  6$              ;IF LOADED OK THEN CONTINUE
5138 013464          ERRDF 4,ADDRRG,R06ERR      ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5139 013464 104455          TRAP  C$ERDF
5140 013466 000004          .WORD 4
5141 013470 002735          .WORD ADDRREG
5142 013472 005020          .WORD R06ERR
5143 013474          CKLOOP
5144 013474 104406          TRAP  C$CLP1
5145
5146                ;SET THE SIGNAL VDAL7 H TO A ZERO TO ASSERT THE SIGNAL FETCT H LOW.
5147
5148 013476 042737 000200 002334 6$: BIC  #VDAL7,R4LOAD  ;SETUP TO CLEAR THE SIGNAL FETCT H
5149 013504 012737 001000 002336  MOV  #VDAL9,R4GOOD  ;SETUP TO EXPECT PSMW H TO BE SET TO 1
5150 013512 004737 006646  JSR  PC,LDRD4R      ;GO LOAD, READ AND CHECK VDAL REG
5151 013516 001405          BEQ  7$              ;IF LOADED OK THEN CONTINUE
5152 013520          ERRDF 3,VDALRG,R4EROR      ;VDAL REG OR PAUSE STATE MACHINE ERROR
5153 013520 104455          TRAP  C$ERDF
5154 013522 000003          .WORD 3
5155 013524 002537          .WORD VDALRG
5156 013526 005004          .WORD R4EROR
5157 013530          CKLOOP
```

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5158 013530 104406          TRAP    C$CLP1
5159
5160                      ;RESELECT THE HDAL REGISTER VIA THE GDAL REGISTER SO THAT THE SIGNAL
5161                      ;XRAS H AND XRAS L CAN BE PULSED BY SETTING AND CLEARING HDAL12 H.
5162
5163 013532 004737 006754    7$:   JSR    PC,SLHDAL          ;GO SELECT HDAL REG VIA THE GDAL REG
5164
5165                      ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. WITH THE
5166                      ;SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE EDFET
5167                      ;FLIP-FLOP WILL BE SET TO A ZERO, THUS ASSERTING THE SIGNAL EDFET H TO
5168                      ;THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL PB H WILL BE
5169                      ;ASSERTED LOW. WHEN THE SIGNAL XRAS H IS ASSERTED PULSES WILL OCCUR ON
5170                      ;THE SIGNALS RASP H AND RASP L.
5171                      ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE SIGNAL
5172                      ;RASP L WHEN THE SIGNALS EPFN L, EP8N L AND PSMW H ARE ALL ASSERTED TO
5173                      ;THE HIGH STATE. WHEN THE EDFET H FLIP-FLOP IS SET TO A ZERO AND THE
5174                      ;SIGNAL RASP H IS PULSED, NO PULSE SHOULD OCCUR ON THE SIGNAL DFET H,
5175                      ;THEREFORE, THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED TO THE
5176                      ;ADDRESS BUS WILL NOT BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER
5177                      ;OR THE FORCE JUMP ADDRESS READBACK REGISTER. THE ADDRESS BUS PRESENTLY
5178                      ;CONTAINS THE DIAGNOSTIC ADDRESS REGISTER DATA PATTERN 031463.
5179
5180 013536 012737 001004 002342  MOV    #HDAL9!HDAL2,R6LOAD    ;RESET PREVIOUS CONTENTS OF HDAL REG
5181 013544 004737 007272          JSR    PC,XRAS              ;GO PULSE XRAS L AND XRAS H VIA HDAL12 H
5182
5183                      ;CHECK THAT THE SIGNAL PSMW H IS STILL SET IN THE VDAL REGISTER AS A
5184                      ;RESULT OF THE PAUSE STATE MACHINE WORKING FLIP-FLOP BEING SET.
5185
5186 013550 004737 006654          JSR    PC,READR4          ;GO CHECK VDAL AND PAUSE STATE MACHINE
5187 013554 001405                BEQ    8$                  ;IF NO CHANGES THEN CONTINUE
5188 013556                          ERRDF  3,VDALRG,R4EROR      ;VDAL OR PAUSE STATE MACHINE ERROR
5189 013556 104455                TRAP  C$ERRDF
5190 013560 000003                .WORD 3
5191 013562 002537                .WORD VDALRG
5192 013564 005004                .WORD R4EROR
5193 013566                          CKLOOP
5194 013566 104406                TRAP  C$CLP1
5195
5196                      ;RESELECT THE FORCE JUMP ADDRESS REGISTER VIA THE GDAL REGISTER BITS
5197                      ;2:0. ON A READ COMMAND TO CONTROL REGISTER 6, THE FORCE JUMP ADDRESS
5198                      ;READBACK REGISTER WILL BE READBACK VIA THE SIGNAL RPT1 L.
5199
5200 013570 004737 007040    8$:   JSR    PC,SLFJAR          ;GO SELECT THE FORCE JUMP ADDRESS REG
5201
5202                      ;READ THE FORCE JUMP ADDRESS READBACK REGISTER AND CHECK THAT THE NEW
5203                      ;DATA (031463) WAS NOT LOADED INTO IT WHEN THE SIGNAL EDFET H IS
5204                      ;ASSERTED LOW AND THE SIGNAL RASP H WAS PULSED. NO PULSES SHOULD
5205                      ;OCCUR ON THE SIGNAL DFET H WHEN THE SIGNAL EDFET H IS LOW.
5206
5207 013574 011137 002342          MOV    (R1),R6LOAD        ;GET THE DATA PREVIOUSLY LOADED INTO
5208                      ;THE FORCE JUMP ADDRESS REGISTER
5209 013600 004737 006700          JSR    PC,READR6        ;GO READ FORCE JUMP ADDRESS REGISTER
5210 013604 001405                BEQ    9$                  ;IF NO CHANGE IN DATA THEN CONTINUE
5211 013606                          ERRDF  4,FJADRG,R06ERR    ;FORCE JUMP ADDRESS READBACK REG ERROR
5212 013606 104455                TRAP  C$ERRDF
5213 013610 000004                .WORD 4

```

TEST 27: WRITE DIAG ADRESS REG INTO FJA READBACK REG (READ VIA RPT1 L)

5214	013612	002766		.WORD	FJADRG	
5215	013614	005020		.WORD	R06ERR	
5216						
5217						:IF DATA EQUALS 031463 THEN DFET H WAS
5218	013616			CKLOOP		:PULSED WHEN FETCT H WAS ASSERTED LOW
5219	013616	104406		TRAP	C\$CLP1	
5220						
5221						:CLEAR THE PAUSE STATE MACHINE BY SETTING AND CLEARING VDAL2 H
5222						
5223	013620	005037	002334	9\$: CLR	R4LOAD	:SETUP TO EXPECT PSMW H TO BE A 0
5224	013624	004737	007712	JSR	PC,CLRPSM	
5225	013630			ENDSEG		
5226	013630			10000\$:		
5227	013630	104405		TRAP	C\$ESEG	
5228						
5229	013632	005721		TST	(R1)+	:UPDATE POINTER TO DATA TABLE
5230	013634	005302		DEC	R2	:CHECK IF ALL DATA PATTERNS LOADED
5231	013636	001410		BEQ	11\$:IF YES THEN END OF THE TEST
5232	013640	000137	013252	JMP	1\$:IF NOT LOAD NEXT PATTERN
5233						
5234	013644	125252		10\$: .WORD	125252	
5235	013646	052525		.WORD	052525	
5236	013650	177400		.WORD	177400	
5237	013652	000377		.WORD	000377	
5238	013654	177777		.WORD	177777	
5239	013656	000000		.WORD	000000	
5240						
5241	013660			11\$:	ENDTST	
5242	013660			L10055:		
5243	013660	104401		TRAP	C\$ETST	

TEST 28: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - OLD FJA

.SBTTL TEST 28: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - OLD FJA

..++
: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE
: PAUSE STATE MACHINE FLIP-FLOPS, PAUSE STATE WORKING, AND PAUSE
: STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING
: THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL
: FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADALO H
: WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE
: STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK
: SIGNAL FROM CAUSING A BREAK AND ADALO H ON A ONE WILL CLEAR THE BREAK LOGIC,
: THUS SETTING THE SIGNAL BRK H TO A ZERO.

..--
: THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD
: FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE OLD FORCE JUMP
: ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525
: 177400, 000377, 177777, AND 000000. THE OLD FORCE JUMP ADDRESS REGISTER GETS
: ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED ON THE ADDRESS
: BUS DURING THIS TEST.

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013662 004737 005510
013666 012701 014552
013672 012702 000006

013676
013676 104404

013700 004737 007006

013704 005037 002342
013710 004737 006672
013714 001405
013716
013716 104455
013720 000004
013722 002631
013724 005020
013726
013726 104406

013730 004737 006754

T28:: BGNST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #19\$,R1 ;GET ADDRESS OF DATA TABLE
MOV #6,R2 ;COUNTER FOR NUMBER OF DATA PATTERNS

1\$: BGNSEG
TRAP C\$BSEG

;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO
;TO A ZERO.

JSR PC,SLMODR ;GO SELECT MODE REG VIA CONTROL REG 0

;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH ZEROES. MR BIT 11
;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE
;MACHINE.

CLR R6LOAD ;SETUP DATA TO BE ZERO
JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
BEQ 2\$;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
TRAP C\$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C\$CLP1

;SET GDAL1 AND GDALO TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

2\$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0

;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.

```

5300 ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
5301 ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE HDAL BUS FROM THE ADDRESS
5302 ;BUS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
5303 ;TIMING AND CONTROL SIGNALS.
5304
5305 013734 012737 001004 002342 MOV #HDAL9!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
5306 013742 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
5307 013746 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
5308 013750 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
5309 013750 104455 TRAP C$ERDF
5310 013752 000004 .WORD 4
5311 013754 002605 .WORD HDALRG
5312 013756 005020 .WORD R06ERR
5313 013760 CKLOOP
5314 013760 104406 TRAP C$CLP1
5315
5316 ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
5317 ;ZEROS. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
5318 ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
5319
5320 013762 004737 007072 3$: JSR PC,SLDADR ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0
5321
5322 ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
5323 ;FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, AND
5324 ;000000.
5325
5326 013766 011137 002342 MOV (R1),R6LOAD ;GET DATA PATTERN FROM TABLE
5327 013772 004737 006672 JSR PC,LDRDR6 ;GO LOAD READ AND CHECK DIAG ADDRESS REG
5328 013776 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
5329 014000 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5330 014000 104455 TRAP C$ERDF
5331 014002 000004 .WORD 4
5332 014004 002735 .WORD ADDR RG
5333 014006 005020 .WORD R06ERR
5334 014010 CKLOOP
5335 014010 104406 TRAP C$CLP1
5336
5337 ;LOAD, READ AND CHECK ADAL REGISTER WITH A DATA PATTERN OF 0C0001.
5338 ;ADAL0 ON A ONE WILL HOLD THE BREAK LOGIC CLEARED. ADAL4 ON A ZERO
5339 ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
5340 ;WHEN THE SIGNAL XRAS H IS PULSED.
5341
5342 014012 012737 000001 002330 4$: MOV #ADAL0,R2LOAD ;SETUP BIT TO BE LOADED
5343 014020 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REG
5344 014024 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
5345 014026 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL 1
5346 014026 104455 TRAP C$ERDF
5347 014030 000002 .WORD 2
5348 014032 002513 .WORD ADALRG
5349 014034 004770 .WORD R2EROR
5350 014036 CKLOOP
5351 014036 104406 TRAP C$CLP1
5352
5353 ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
5354 ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
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5356 014040 005037 002334      5$: CLR      R4LOAD      ;SETUP TO CLEAR ALL BITS IN VDAL REG
5357 014044 004737 007712      JSR      PC,CLRPSM    ;GO SET AND CLEAR VDAL2 H
5358
5359                               ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A
5360                               ;ONE AND GDAL BITS 1 AND 2 TO ZEROES. ON A WRITE COMMAND TO CONTROL
5361                               ;REGISTER 6, DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS
5362                               ;REGISTER AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
5363                               ;TO A ONE.
5364
5365 014050 004737 007040      JSR      PC,SLFJAR    ;SELECT FORCE JUMP ADDRESS REG VIA GDAL
5366
5367                               ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA PATTERN
5368                               ;146314 INTO THE NEW FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS
5369                               ;WPT1 HB H AND WPT1 LB H. THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP
5370                               ;WILL ALSO GET SET VIA THE SIGNAL WPT1 LB H. THE NEW FORCE JUMP
5371                               ;ADDRESS REGISTER IS WRITTEN WITH DATA TO CHECK THAT THE CORRECT FORCE
5372                               ;JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS WHEN THE 16 BIT
5373                               ;ADDRESS FLIP-FLOP IS SET. THE OLD FORCE JUMP ADDRESS REGISTER SHOULD
5374                               ;BE ENABLED TO THE EODAL BUS DURING THIS TEST. THE TAKE NEW FORCE
5375                               ;JUMP ADDRESS FLIP-FLOP WILL BE CLEARED FOLLOWING THE CHECK THAT IT
5376                               ;WAS SET TO A ONE.
5377
5378 014054 012777 146314 166224  MOV      #146314,@REG6 ;WRITE NEW FORCE JUMP ADDRESS REGISTER
5379
5380                               ;READ THE VDAL REGISTER TO CHECK THAT THE NEW FORCE JUMP ADDRESS FLIP-
5381                               ;FLOP IS SET TO A ONE. THE FLIP-FLOP WILL BE READ IN THE VDAL REGISTER
5382                               ;AS THE SIGNAL TNFJ H.
5383
5384 014062 052737 100000 002336  BIS      #VDAL15,R4GOOD ;SETUP TO EXPECT TNFJ H TO BE A 1
5385 014070 004737 006654      JSR      PC,READR4    ;GO READ VDAL AND PAUSE STATE MACHINE
5386 014074 001405      BEQ      8$          ;IF TNFJ H SET THEN CONTINUE
5387 014076      ERRDF    3,VDALRG,R4EROR ;TNFJ H PROBABLY NOT SET IN VDAL REG
5388 014076 104455      TRAP    C$ERRDF
5389 014100 000003      .WORD   3
5390 014102 002537      .WORD   VDALRG
5391 014104 005004      .WORD   R4EROR
5392 014106
5393 014106 104406      CKLOOP
5394      TRAP    C$CLP1
5395
5396                               ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H. SET VDAL2 H TO A ONE
5397                               ;TO CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS AND THE TAKE NEW FORCE
5398                               ;JUMP ADDRESS FLIP-FLOP.
5399 014110 012737 000200 002334 8$: MOV      #VDAL7,R4LOAD ;SETUP BIT TO SET FETCT H
5400 014116 004737 007712      JSR      PC,CLRPSM    ;GO SET FETCT H AND PULSE VDAL2 H
5401
5402                               ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
5403                               ;TO ONES. BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
5404                               ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L
5405
5406 014122 004737 006754      JSR      PC,SLHDAL    ;GO SELECT HDAL REG VIA GDAL 2:0
5407
5408                               ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
5409                               ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
5410                               ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
5411                               ;HIGH STATE. THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
  
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5412      :IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
5413      :TO THE HIGH STATE. THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
5414      :SIGNAL PAUSE L IS ASSERTED HIGH. WHEN SOP H AND FETCT H ARE ASSERTED
5415      :HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
5416      :WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
5417      :PSMW H WILL BE ASSERTED HIGH. THE SIGNAL PSMW H IS READ IN THE VDAL
5418      :REGISTER AS VDAL9 H. WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
5419      :SIGNAL PB H WILL BE ASSERTED HIGH. THE SIGNAL PB H IS THE DATA INPUT
5420      :LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
5421      :
5422      :THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED. WHEN THE
5423      :SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
5424      :PULSE WILL BE ISSUED ON THE SIGNAL DFET H. THE SIGNAL DFET H WILL
5425      :CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER. AT THE
5426      :PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
5427      :ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
5428      :LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.
5429      :
5430      014126 012737 001004 002342      MOV      #HDAL9!HDAL2,R6LOAD      ;BITS PREVIOUSLY SET IN HDAL REG
5431      014134 004737 007272              JSR      PC,XRAS                  ;PULSE XRAS H AND XRAS L VIA HDAL12 H
5432      :
5433      :CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
5434      :THE LOW STATE. CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
5435      :STATE AS A RESULT OF SOP H AND EDFET H BEING ASSERTED HIGH.
5436      :
5437      :   PAUSE STATE WORKING - PSMW H - 1
5438      :   PAUSE STATE SYNC - EPSF H - 0
5439      :   16 BIT ADDRESS - EPFN H - 0
5440      014140 042737 000200 002334      BIC      #VDAL7,R4LOAD            ;SETUP TO CLEAR FETCT H
5441      014146 013737 002334 002336      MOV      R4LOAD,R4GOOD            ;COPY DATA LOADED TO EXPECTED
5442      014154 052737 001000 002336      BIS      #VDAL9,R4GOOD            ;EXPECT PSMW H TO BE SET
5443      014162 004737 006646              JSR      PC,LDRD4R                ;GO LOAD, READ AND CHECK VDAL REG
5444      014166 001405              BEQ      11$                      ;IF LOADED OK THEN CONTINUE
5445      014170              ERDRDF 3,VDALRG,R4EROR            ;VDAL OR PAUSE STATE MACHINE ERROR
5446      014170 104455              TRAP    C$ERDF
5447      014172 000003              .WORD   3
5448      014174 002537              .WORD   VDALRG
5449      014176 005004              .WORD   R4EROR
5450      014200              CKLOOP
5451      014200 104406              TRAP    C$CLP1
5452      :
5453      :SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
5454      :SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
5455      :SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
5456      :SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE. THE SIGNAL XCAS H
5457      :WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-FLOP (0)
5458      :INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE 16 BIT ADDRESS
5459      :FLIP-FLOP TO A ZERO.
5460      :
5461      014202 004737 007410      11$:   JSR      PC,XCASH                  ;SET XCAS H TO THE HIGH STATE
5462      :
5463      :READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
5464      :IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET TO 1.
5465      :
5466      :   PAUSE STATE WORKING - PSMW H - 1
5467      :   PAUSE STATE SYNC - EPSF H - 1
5467      :   16 BIT ADDRESS - EPFN H - 0

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5468
5469 014206 052737 002000 002336   BIS      #VDAL10,R4GOOD      ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
5470 014214 004737 006654           JSR      PC,READR4         ;GO READ AND CHECK PAUSE STATE MACHINE
5471 014220 001405           BEQ      12$              ;IF LOADED OK THEN CONTINUE
5472 014222           ERRDF   3,VDALRG,R4EROR    ;EPSF H PROBABLE NOT SET IN VDAL REG
5473 014222 104455           TRAP    C$ERDF
5474 014224 000003           .WORD   3
5475 014226 002537           .WORD   VDALRG
5476 014230 005004           .WORD   R4EROR
5477 014232           CKLOOP
5478 014232 104406           TRAP    C$CLP1
5479
5480           ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE 16 BIT
5481           ;INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE EODAL BUS AT THIS TIME.
5482           ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE ENABLED
5483           ;TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
5484
5485 014234 004737 007122 12$:   JSR      PC,SEODAL         ;SELECT EODAL BUS VIA GDAL BITS 2:0
5486
5487           ;THE SIGNAL ACAS H WILL BE ASSERTED HIGH AS A RESULT OF THE SIGNAL
5488           ;XCAS H BEING ASSERTED HIGH AND THE SIGNAL PSMW H BEING ASSERTED HIGH.
5489           ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE PAUSE STATE SYNC FLIP-
5490           ;FLOP IS SET TO A ONE, THE SIGNALS EDRL L AND EDRH L WILL BE ASSERTED
5491           ;LOW. THESE TWO SIGNALS WILL ENABLE THE 16 BIT INSTRUCTION REGISTER
5492           ;ONTO THE EODAL BUS. WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
5493           ;6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL
5494           ;RPT7 L. THE SIGNAL RPT7 L WILL READBACK THE 16 BIT INSTRUCTION REGIS-
5495           ;TER WHICH IS ENABLED TO THE EODAL BUS AT THIS POINT IN TIME.
5496
5497 014240 012737 000137 002342   MOV      #137,R6LOAD      ;SETUP EXPECTED 16 BIT INSTRUCTION (JMP)
5498 014246 004737 006700           JSR      PC,READR6         ;READ 16 BIT INSTRUCTION REG ON EODAL BUS
5499 014252 001405           BEQ      13$              ;IF INSTRUCTION EQUALS "JMP" THEN CONT
5500 014254           ERRDF   4,IEODAL,R06ERR   ;EODAL BUS ERROR, OR 16 BIT INSTRUCTION
5501 014254 104455           TRAP    C$ERDF
5502 014256 000004           .WORD   4
5503 014260 003034           .WORD   IEODAL
5504 014262 005020           .WORD   R06ERR
5505
5506           ;REGISTER ERROR, OR 16 BIT INSTRUCTION
5507           ;REGISTER NOT ENABLED TO THE BUS
5507 014264           CKLOOP
5508 014264 104406           TRAP    C$CLP1
5509
5510           ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND
5511           ;GDAL0 TO ONES.
5512
5513 014266 004737 006754 13$:   JSR      PC,SLHDAL        ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
5514
5515           ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER
5516
5517 014272 012737 021004 002342   MOV      #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
5518 014300 004737 007442           JSR      PC,XCASL         ;GO SET XCAS H TO THE LOW STATE
5519
5520           ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
5521           ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.
5522
5523 014304 004737 007502           JSR      PC,XPI          ;GO PULSE XPI H VIA HDAL15 H

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5534 014310 004737 007272
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5542 014314 004737 006654
5543 014320 001405
5544 014322
5545 014322 104455
5546 014324 000003
5547 014326 002537
5548 014330 005004
5549 014332
5550 014332 104406
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5554
5555
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5557
5558
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5560 014334 004737 007410 14$:
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5568 014340 042737 002000 002336
5569 014346 052737 004000 002336
5570 014354 004737 006654
5571 014360 001405
5572 014362
5573 014362 104455
5574 014364 000003
5575 014366 002537
5576 014370 005004
5577 014372
5578 014372 104406
5579

;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
;WITH THE SIGNAL FEICT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
;AND RASP L WILL BE PULSED.
;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

JSR PC,XRAS ;GO PULSE XRAS H BY HDAL12

;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
: PAUSE STATE WORKING - PSMW H - 1
: PAUSE STATE SYNC - EPSF H - 1
: 16 BIT ADDRESS - EPFN H - 0

JSR PC,READR4 ;CHECK VDAL AND PAUSE STATE MACHINE
BEQ 14$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;PAUSE STATE WORKING F/F PROBABLY NOT SET
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1

;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
;SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
;SIGNAL 'PB H', WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
;THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO. THE SIGNAL
;XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
;FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE
;16 BIT ADDRESS FLIP-FLOP TO A ONE.

JSR PC,XCASH ;SET THE SIGNAL XCAS H TO HIGH STATE

;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
: PAUSE STATE WORKING - PSMW H - 1
: PAUSE STATE SYNC - EPSF H - 0
: 16 BIT ADDRESS - EPFN H - 1

BIC #VDAL10,R4GOOD ;CLEAR BITS FOR EPSF H
BIS #VDAL11,R4GOOD ;SET BIT FOR EPFN H
JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
BEQ 15$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;EPFN H PROBABLY NOT SET IN VDAL REG
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1
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5580 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE FORCE
5581 ;JUMP ADDRESS REGISTER SHOULD BE ENABLED ON THE EODAL BUS AT THIS TIME.
5582 ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ
5583 ;BACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
5584
5585 014374 004737 007122 15$: JSR FC,SEODAL ;SELECT EODAL BUS VIA GDAL BITS 2:0
5586
5587 ;ON THE FIRST PULSE OF XRAS H WHEN THE SIGNAL EDFET H WAS SET HIGH,
5588 ;THE FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED WITH THE DATA
5589 ;IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE CLOCKING SIGNAL DFET H
5590 ;(ADDRESS BUS TO FORCE JUMP ADDRESS REGISTER). AT THIS POINT IN TIME,
5591 ;THE FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS VIA
5592 ;THE SIGNALS OEARH L AND OEARL L. THESE SIGNALS ARE ASSERTED LOW AS A
5593 ;RESULT OF THE FLIP-FLOP "GET NEW ADDRESS" BEING CLEARED AND THE
5594 ;SIGNALS EARH H AND EARL H BEING ASSERTED HIGH. THE "GET NEW ADDRESS"
5595 ;FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THE TEST WHEN VDAL REGISTER
5596 ;BIT 2 WAS SET AND CLEARED. THE SIGNAL EARH H AND EARL H ARE ASSERTED
5597 ;HIGH AS A RESULT OF THE 16 BIT ADDRESS FLIP-FLOP BEING SET TO A ONE,
5598 ;THE SIGNAL ACAS H BEING ASSERTED HIGH, AND MODE REGISTER BIT 11 SETUP
5599 ;FOR 16 BIT ADDRESS MODE. THE FOLLOWING SECTION WILL READ THE EODAL
5600 ;BUS VIA THE SIGNAL RPT7 L AND CHECK THAT THE DIAGNOSTIC ADDRESS
5601 ;REGISTER WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER AND THAT
5602 ;THE OLD FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS.
5603
5604 ;IF THE ADDRESS READ FROM THE FORCE JUMP ADDRESS REGISTER EQUALS
5605 ;146314 THEN THE WRONG FORCE JUMP ADDRESS REGISTER WAS READ. THE
5606 ;DATA PATTERN 146314 WAS WRITTEN INTO THE NEW FORCE JUMP ADDRESS
5607 ;REGISTER WHICH SHOULD NOT BE SELECTED. CHECK THE "GET NEW ADDRESS"
5608 ;FLIP-FLOP TO CHECK THAT IT IS CLEARED. THE "GET NEW ADDRESS" FLIP
5609 ;FLOP WAS CLEARED BY VDAL2 H AT THE BEGINNING OF THE TEST. THE OLD
5610 ;FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL BUS DURING
5611 ;THIS TEST. THE OLD FORCE JUMP ADDRESS REGISTER IS THAT REGISTER
5612 ;WHICH GETS ITS DATA FROM THE ADDRESS BUS.
5613
5614 014400 011137 002342 MOV (R1),R6LOAD ;GET DATA LOADED INTO DIAG ADDRESS REG
5615 014404 004737 006700 JSR PC,READR6 ;READ FORCE JUMP ADDRESS ON EODAL BUS
5616 014410 001405 BEQ 16$ ;IF FORCE JUMP ADDRESS REG OK THEN CONT
5617 014412 ERRDF 4,FEODAL,R06ERR ;FORCE JUMP ADDRESS REG TO EODAL BUS ERR
5618 014412 104455 TRAP C$ERRDF
5619 014414 000004 .WORD 4
5620 014416 003147 .WORD FEODAL
5621 014420 005020 .WORD R06ERR
5622 014422 CKLOOP
5623 014422 104406 TRAP C$CLP1
5624
5625 ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL BITS 1
5626 ;AND 0 TO ZEROES.
5627
5628 014424 004737 006754 16$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0
5629
5630 ;SET THE SIGNAL XCAS H WHICH IS PRESENTLY ASSERTED HIGH TO THE LOW
5631 ;STATE BY SETTING HDAL13 H TO A ZERO.
5632
5633 014430 012737 021004 002342 MOV #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
5634 014436 004737 007442 JSR PC,XCASL ;GO SET XCAS H TO THE LOW STATE
5635

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5636                                     ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
5637                                     ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.
5638
5639 014442 004737 007502              JSR      PC,XPI                      ;GO PULSE XPI H VIA HDAL15 H
5640
5641                                     ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
5642                                     ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
5643                                     ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
5644                                     ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
5645                                     ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
5646                                     ;AND RASP L WILL BE PULSED.
5647                                     ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L
5648                                     ;WHEN THE SIGNALS EP8N L AND PSMW H ARE ASSERTED HIGH AND EPFN L IS
5649                                     ;ASSERTED LOW. A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H WILL BE
5650                                     ;ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING
5651                                     ;CLEARED.
5652
5653 014446 004737 007272              JSR      PC,XRAJ                     ;PULSE XRAS VIA THE SIGNAL HDAL12
5654
5655                                     ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
5656                                     ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
5657                                     :      PAUSE STATE WORKING - PSMW H - 0
5658                                     :      PAUSE STATE SYNC - EPSF H - 0
5659                                     :      16 BIT ADDRESS - EPFN H - 1
5660
5661 014452 042737 001000 002336      BIC      #VDAL9,R4GOOD                ;SETUP TO EXPECT PSMW H TO BE 0
5662 014460 004737 006654              JSR      PC,READR4                    ;GO READ VDAL AND PAUSE STATE MACHINE
5663 014464 001405                      BEQ      17$                          ;IF OK THEN CONTINUE
5664 014466                               ERRDF   3,VDALRG,R4EROR                ;PSMW H PROBABLY NOT ZEROED
5665 014466 104455                      TRAP    C$ERDF
5666 014470 000003                      .WORD   3
5667 014472 002537                      .WORD   VDALRG
5668 014474 005004                      .WORD   R4EROR
5669 014476                               CKLOOP
5670 014476 104406                      TRAP    C$CLP1
5671
5672                                     ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13. THE SIGNAL
5673                                     ;XCAS H WILL CLOCK THE OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP INTO
5674                                     ;THE 16 BIT ADDRESS FLIP-FLOP, THUS CLEARING THE 16 BIT ADDRESS F/F.
5675
5676 014500 004737 007376              17$: JSR      PC,XCAS                      ;GO PULSE XCAS H VIA HDAL13 H
5677
5678                                     ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
5679                                     ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
5680                                     :      PAUSE STATE WORKING - PSMW H - 0
5681                                     :      PAUSE STATE SYNC - EPSF H - 0
5682                                     :      16 BIT ADDRESS - EPFN H - 0
5683
5684 014504 042737 004000 002336      BIC      #VDAL11,R4GOOD                ;SETUP TO EXPECT EPFN H TO BE 0
5685 014512 004737 006654              JSR      PC,READR4                    ;GO READ VDAL AND PAUSE STATE MACHINE
5686 014516 001405                      BEQ      18$                          ;IF OK THEN CONTINUE
5687 014520                               ERRDF   3,VDALRG,P4EROR                ;EPFN H PROBABLY NOT CLEARED
5688 014520 104455                      TRAP    C$ERD.
5689 014522 000003                      .WORD   3
5690 014524 002537                      .WORD   VDALRG
5691 014526 005004                      .WORD   R4EROR

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5692 014530          CKLOOP
5693 014530 104406  TRAP    C$CLP1
5694
5695                ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
5696                ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
5697
5698 014532 004737 007502 18$:   JSR    PC,XPI          ;GO PULSE XPI H VIA HDAL15 H
5699 014536          ENDSEG
5700 014536          10000$:
5701 014536 104405  TRAP    C$ESEG
5702
5703 014540 005721  TST    (R1)+          ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
5704 014542 005302  DEC    R2             ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
5705 014544 001410  BEQ    20$           ;IF YES THEN END OF TEST
5706 014546 000137 013676  JMP    1$             ;IF NOT THEN LOAD NEXT PATTERN
5707
5708 014552 125252 19$:   .WORD  125252
5709 014554 052525  .WORD  052525
5710 014556 177400  .WORD  177400
5711 014560 000377  .WORD  000377
5712 014562 177777  .WORD  177777
5713 014564 000000  .WORD  000000
5714
5715 014566          20$:   ENDTST
5716 014566          L10056:
5717 014566 104401  TRAP    C$ETST
5718
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TEST 29: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - NEW FJA

.SBTTL TEST 29: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - NEW FJA

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: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE
: PAUSE STATE MACHINE FLIP - FLOP'S , PAUSE STATE WORKING , PAUSE
: STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING
: THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL
: FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADALO H
: WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE
: STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK
: SIGNAL FROM CAUSING A BREAK AND ADALO H ON A ONE WILL CLEAR THE BREAK LOGIC,
: THUS SETTING THE SIGNAL BRK H TO A ZERO.
  
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: THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW
: FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE NEW FORCE JUMP
: ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525
: 177400, 000377, 177777, AND 000000. THE NEW FORCE JUMP ADDRESS REGISTER IS
: LOADED AT THE BEGINNING OF THE TEST.
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014570 004737 005510
014574 012701 015544
014600 012702 000006
014604
014604 104404
014606 004737 007006
014612 005037 002342
014616 004737 006672
014622 001405
014624
014624 104455
014626 000004
014630 002631
014632 005020
014634
014634 104406
  
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BGNTST
T29:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
      MOV #17$,R1 ;GET ADDRESS OF DATA TABLE
      MOV #6,R2 ;COUNTER FOR NUMBER OF DATA PATTERNS

1$: BGNSEG
   TRAP C$BSEG
   ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO
   ;TO A ZERO.
   JSR PC,SLMODR ;GO SELECT MODE REG VIA CONTROL REG 0
   ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH ZEROES. MR BIT 11
   ;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE
   ;MACHINE.
   CLR R6LOAD ;SETUP DATA TO BE ZERO
   JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
   BEQ 2$ ;IF LOADED OK THEN CONTINUE
   ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
   TRAP C$ERDF
   .WORD 4
   .WORD MODREG
   .WORD R06ERR
   CKLOOP
   TRAP C$CLP1
   ;SET GDAL1 AND GDALO TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
   ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
2$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0
   ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
   ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
  
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5775 ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
5776 ;BUS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
5777 ;TIMING AND CONTROL SIGNALS.
5778
5779 014642 012737 001004 002342 MOV #HDAL9!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
5780 014650 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
5781 014654 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
5782 014656 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
5783 014656 104455 TRAP C$ERDF
5784 014660 000004 .WORD 4
5785 014662 002605 .WORD HDALRG
5786 014664 005020 .WORD R06ERR
5787 014666 CKLOOP
5788 014666 104406 TRAP C$CLP1
5789
5790 ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
5791 ;ZEROS. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
5792 ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
5793
5794 014670 004737 007072 3$: JSR PC,SLDADR ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0
5795
5796 ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
5797 ;OF 146314. THE DIAGNOSTIC ADDRESS REGISTER IS WRITTEN WITH DATA TO
5798 ;CHECK THAT THE CORRECT FORCE JUMP ADDRESS IS ENABLED TO THE EODAL BUS
5799 ;WHEN THE 16 BIT ADDRESS FLIP-FLOP IS SET. THE NEW FORCE JUMP ADDRESS
5800 ;REGISTER WILL BE ENABLED TO THE EODAL BUS IN THIS TEST.
5801
5802 014674 012737 146314 002342 MOV #146314,R6LOAD ;WRITE DIAG ADDRESS REG WITH 146314
5803 014702 004737 006672 JSR PC,LDRDR6 ;GO LOAD READ AND CHECK DIAG ADDRESS REG
5804 014706 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
5805 014710 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5806 014710 104455 TRAP C$ERDF
5807 014712 000004 .WORD 4
5808 014714 002735 .WORD ADDR RG
5809 014716 005020 .WORD R06ERR
5810 014720 CKLOOP
5811 014720 104406 TRAP C$CLP1
5812
5813 ;LOAD, READ AND CHECK ADAL REGISTER WITH A DATA PATTERN OF 000001.
5814 ;ADAL0 ON A ONE WILL HOLD THE BREAK LOGIC CLEARED. ADAL4 ON A ZERO
5815 ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
5816 ;WHEN THE SIGNAL XRAS H IS PULSED.
5817
5818 014722 012737 000001 002330 4$: MOV #ADAL0,R2LOAD ;SETUP BIT TO BE LOADED
5819 014730 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REG
5820 014734 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
5821 014736 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL 1
5822 014736 104455 TRAP C$ERDF
5823 014740 000002 .WORD 2
5824 014742 002513 .WORD ADALRG
5825 014744 004770 .WORD R2EROR
5826 014746 CKLOOP
5827 014746 104406 TRAP C$CLP1
5828
5829 ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
5830 ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS

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5831
5832 014750 005037 002334      5$: CLR      R4LOAD      ;CLEAR WORKING BITS FOR VDAL REG
5833 014754 004737 007712      JSR      PC,CLRPSM    ;SET VDAL2 H TO A 1 AND THEN 0
5834
5835                               ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL0 H TO A
5836                               ;ONE AND GDAL BITS 1 AND 2 TO ZEROES. ON A WRITE COMMAND TO CONTROL
5837                               ;REGISTER 6, DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS
5838                               ;REGISTER AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
5839                               ;TO A ONE.
5840
5841 014760 004737 007040      JSR      PC,SLFJAR    ;SELECT FORCE JUMP ADDRESS REG VIA GDAL
5842
5843                               ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE DATA INTO THE NEW
5844                               ;FORCE JUMP ADDRESS REGISTER. THE DATA WILL BE LOADED INTO THE NEW FORCE
5845                               ;JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB H AND WPT1 HB H. THE TAKE
5846                               ;NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO BE CLOCKED TO A ONE BY THE
5847                               ;SIGNAL WPT1 LB H. THE DATA PATTERNS LOADED WILL BE ONE OF THE FOLLOW-
5848                               ;ING: 125252, 052525, 177400, 000377, 177777, AND 000000.
5849
5850 014764 011177 165316      MOV      (R1),@REG6   ;WRITE NEW FORCE JUMP ADDRESS REGISTER
5851
5852                               ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
5853                               ;CHECK THAT THE SIGNAL WPT1 LB H CLOCKED THE TAKE NEW FORCE JUMP ADDRESS
5854                               ;FLIP-FLOP TO A ONE.
5855
5856 014770 012737 000200 002334  MOV      #VDAL7,R4LOAD ;SETUP BITS TO BE LOADED
5857 014776 013737 002334 002336  MOV      R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
5858 015004 052737 100000 002336  BIS      #VDAL15,R4GOOD ;SETUP TO EXPECT TNFJ H FLIP-FLOP = 1
5859 015012 004737 006646      JSR      PC,LDRD4R    ;GO LOAD, READ AND CHECK VDAL REGISTER
5860 015016 001405      BEQ      6$          ;IF LOADED OK THEN CONTINUE
5861 015020      ERRDF 3,VDALRG,R4EROR ;TNFJ H PROBABLY NOT SET IN VDAL REG
5862 015020 104455      TRAP   C$ERRDF
5863 015022 000003      .WORD 3
5864 015024 002537      .WORD VDALRG
5865 015026 005004      .WORD R4EROR
5866 015030      CKLOOP
5867 015030 104406      TRAP   C$CLP1
5868
5869                               ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
5870                               ;TO ONES. BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
5871                               ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L
5872
5873 015032 004737 006754      6$: JSR      PC,SLHDAL    ;GO SELECT HDAL REG VIA GDAL 2:0
5874
5875                               ;SET HDAL12 H TO A ONE TO SET THE SIGNALS XRAS H AND XRAS L TO THE
5876                               ;HIGH AND LOW STATE RESPECTIVELY. THEY WILL REMAIN SET TO THESE STATES
5877                               ;UNTIL THE PROGRAM HAS PULSED THE SIGNALS XPI H AND XPI L.
5878
5879                               ;
5880                               ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
5881                               ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
5882                               ;HIGH STATE. THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
5883                               ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
5884                               ;TO THE HIGH STATE. THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
5885                               ;SIGNAL PAUSE L IS ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED
5886                               ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
                               ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL

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5943 : PAUSE STATE WORKING - PSMW H - 1
5944 : PAUSE STATE SYNC - EPSF H - 1
5945 : 16 BIT ADDRESS - EPFN H - 0
5946 : TAKE NEW FJ ADDRESS - TNFJ H - 1
5947 : GET NEW ADDRESS - OUTNEW H - 0
5948
5949 015116 052737 002000 002336 BIS #VDAL10,R4GOOD ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
5950 015124 004737 006654 JSR PC,READR4 ;GO READ AND CHECK PAUSE STATE MACHINE
5951 015130 001405 BEQ 8$ ;IF LOADED OK THEN CONTINUE
5952 015132 ERRDF 3,VDALRG,R4EROR ;EPSF H PROBABLE NOT SET IN VDAL REG
5953 015132 104455 TRAP C$ERDF
5954 015134 000003 .WORD 3
5955 015136 002537 .WORD VDALRG
5956 015140 005004 .WORD R4EROR
5957 015142 CKLOOP
5958 015142 104406 TRAP C$CLP1
5959
5960 :SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE 16 BIT
5961 :INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE EODAL BUS AT THIS TIME.
5962 :ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE ENABLED
5963 :TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
5964
5965 015144 004737 007122 8$: JSR PC,SEODAL ;SELECT EODAL BUS VIA GDAL BITS 2:0
5966
5967 :THE SIGNAL ACAS H WILL BE ASSERTED HIGH AS A RESULT OF THE SIGNAL
5968 :XCAS H BEING ASSERTED HIGH AND THE SIGNAL PSMW H BEING ASSERTED HIGH.
5969 :WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE PAUSE STATE SYNC FLIP-
5970 :FLOP IS SET TO A ONE, THE SIGNALS EDRL L AND EDRL L WILL BE ASSERTED
5971 :LOW. THESE TWO SIGNALS WILL ENABLE THE 16 BIT INSTRUCTION REGISTER
5972 :ONTO THE EODAL BUS. WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
5973 :6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL
5974 :RPT7 L. THE SIGNAL RPT7 L WILL READBACK THE 16 BIT INSTRUCTION REGIS-
5975 :TER WHICH IS ENABLED TO THE EODAL BUS AT THIS POINT IN TIME.
5976
5977 015150 012737 000137 002342 MOV #137,R6LOAD ;SETUP EXPECTED 16 BIT INSTRUCTION (JMP)
5978 015156 004737 006700 JSR PC,READR6 ;READ 16 BIT INSTRUCTION REG ON EODAL BUS
5979 015162 001405 BEQ 9$ ;IF INSTRUCTION EQUALS "JMP" THEN CONT
5980 015164 ERRDF 4,IEODAL,R06ERR ;EODAL BUS ERROR, OR 16 BIT INSTRUCTION
5981 015164 104455 TRAP C$ERDF
5982 015166 000004 .WORD 4
5983 015170 003034 .WORD IEODAL
5984 015172 005020 .WORD R06ERR
5985 :REGISTER ERROR, OR 16 BIT INSTRUCTION
5986 :REGISTER NOT ENABLED TO THE BUS
5987 015174 CKLOOP
5988 015174 104406 TRAP C$CLP1
5989
5990 :RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND
5991 :GDAL0 TO ONES.
5992
5993 015176 004737 006754 9$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
5994
5995 :SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER
5996 :
5997 :THE SIGNALS XRAS H AND XRAS L WILL REMAIN ASSERTED TO THE HIGH AND LOW
5998 :STATE RESPECTIVELY BY HDAL12 H BEING SET TO A ONE. THEY WILL NOT BE
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6055 015260 104455      TRAP   C$ERDF
6056 015262 000003      .WORD  3
6057 015264 002537      .WORD  VDALRG
6058 015266 005004      .WORD  R4EROR
6059 015270          CKLOOP
6060 015270 104406      TRAP   C$CLP1
6061
6062
6063      :TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
6064      :WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
6065      :EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
6066      :EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
6067      :PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
6068      :AND RASP L WILL BE PULSED.
6069      :THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
6070      :SIGNAL RASP L WHEN EPFN L, EPBN L, AND PSMW H ARE ALL ASSERTED HIGH.
6071 015272 004737 007272      11$: JSR    PC,XRAS          ;GO PULSE XRAS H BY HDAL12
6072
6073      :READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
6074      :TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
6075      :   PAUSE STATE WORKING - PSMW H - 1
6076      :   PAUSE STATE SYNC - EPSF H - 1
6077      :   16 BIT ADDRESS - EPFN H - 0
6078      :   TAKE NEW FJ ADDRESS - TNFJ H - 1
6079      :   GET NEW ADDRESS - OUTNEW H - 1
6080
6081 015276 004737 006654      JSR    PC,READR4          ;CHECK VDAL AND PAUSE STATE MACHINE
6082 015302 001405      BEQ    12$                ;IF OK THEN CONTINUE
6083 015304          ERRDF  3,VDALRG,R4EROR      ;VDAL OR PAUSE STATE MACHINE ERROR
6084 015304 104455      TRAP   C$ERDF
6085 015306 000003      .WORD  3
6086 015310 002537      .WORD  VDALRG
6087 015312 005004      .WORD  R4EROR
6088 015314          CKLOOP
6089 015314 104406      TRAP   C$CLP1
6090
6091      :SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
6092      :SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
6093      :SIGNAL 'PB H', WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
6094      :THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO. THE SIGNAL
6095      :XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
6096      :FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE
6097      :16 BIT ADDRESS FLIP-FLOP TO A ONE.
6098      :
6099      :THE SIGNAL XCAS H WILL ALSO CAUSE THE 'TAKE NEW FORCE JUMP ADDRESS'
6100      :FLIP-FLOP TO BE CLEARED WHEN THE 'GET NEW ADDRESS' FLIP-FLOP IS SET
6101      :TO A ONE.
6102
6103 015316 004737 007410      12$: JSR    PC,XCASH          ;ASSERT XCAS H TO THE HIGH STATE
6104
6105      :READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
6106      :FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
6107      :   PAUSE STATE WORKING - PSMW H - 1
6108      :   PAUSE STATE SYNC - EPSF H - 0
6109      :   16 BIT ADDRESS - EPFN H - 1
6110      :   TAKE NEW FJ ADDRESS - TNFJ H - 0

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6223      : PAUSE STATE SYNC - EPSF H - 0
6224      : 16 BIT ADDRESS - EPFN H - 0
6225      : TAKE NEW FJ ADDRESS - TNFJ H - 0
6226      : GET NEW ADDRESS - OUTNEW H - 1
6227
6228 015466 042737 004000 002336 BIC #VDAL11,R4GOOD ;SETUP TO EXPECT EPFN H TO BE 0
6229 015474 004737 006654 JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
6230 015500 001405 BEQ 16$ ;IF OK THEN CONTINUE
6231 015502 ERRDF 3,VDALRG,R4EROR ;EPFN H PROBABLY NOT CLEARED
6232 015502 104455 TRAP C$ERDF
6233 015504 000003 .WORD 3
6234 015506 002537 .WORD VDALRG
6235 015510 005004 .WORD R4EROR
6236 015512 CKLOOP
6237 015512 104406 TRAP C$CLP1
6238
6239      ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
6240      ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
6241
6242 015514 004737 007502 16$: JSR PC,XPI ;GO PULSE XPI H VIA HDAL15 H
6243
6244      ;TO CHECK THAT THE "GET NEW ADDRESS" FLIP-FLOP CAN BE CLEARED, THE
6245      ;PROGRAM WILL SET VDAL2 H TO A ONE AND THEN A ZERO. THE "GET NEW
6246      ;ADDRESS" FLIP-FLOP WILL BE CLEARED WHEN VDAL2 H IS SET TO A ONE.
6247
6248 015520 005037 002334 CLR R4LOAD ;CLEAR WORKING BITS FOR VDAL REG
6249 015524 004737 007712 JSR PC,CLRPSM ;SET VDAL2 H TO A 1 AND THEN 0
6250
6251 015530 ENDSEG
6252 015530 10000$: TRAP C$ESEG
6253 015530 104405
6254
6255 015532 005721 TST (R1)+ ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
6256 015534 005302 DEC R2 ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
6257 015536 001410 BEQ 18$ ;IF YES THEN END OF TEST
6258 015540 000137 014604 JMP 1$ ;IF NOT THEN LOAD NEXT PATTERN
6259
6260 015544 125252 17$: .WORD 125252
6261 015546 052525 .WORD 052525
6262 015550 177400 .WORD 177400
6263 015552 000377 .WORD 000377
6264 015554 177777 .WORD 177777
6265 015556 000000 .WORD 000000
6266
6267 015560 18$: ENDTST
6268 015560 L10057:
6269 015560 104401 TRAP C$ETST
6270

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TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

.SBTTL TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

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: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 'RUN' AND 16 BIT ADDRESS MODE.
: WHEN THE PAUSE STATE MACHINE IS SETUP IN 'RUN' MODE VIA ADAL4 H ON A ONE AND
: A PULSE ON THE SIGNAL XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN
: A BREAK CONDITION IS RECEIVED ON THE SIGNAL 'BRK H'. THIS TEST WILL USE THE
: TIMEOUT BREAK ONE SHOT TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK
: THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN NO BREAK CONDITION IS RECEIVED
: AND THAT IT IS ENTERED WHEN A BREAK CONDITION IS RECEIVED. THE TEST WILL CHECK
: ALL THE PAUSE STATE LOGIC ASSOCIATED WITH THE SIGNAL 'BRK H'. THE TEST WILL
: CHECK THAT THE SIGNAL 'TOBRK H' IS SET IN CONTROL REGISTER 0 WHEN THE TIME OUT
: BREAK ONE SHOT IS NOT BEING FIRED AND THAT IT IS NOT SET WHEN THE TIME OUT
: BREAK ONE SHOT IS BEING FIRED.
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015562 004737 005510

015566
015566 104404

015570 004737 007006

015574 005037 002342
015600 004737 006672
015604 001405
015606
015606 104455
015610 000004
015612 002631
015614 005020
015616
015616 104406

015620 004737 006754

015624 012737 000004 002342
015632 004737 006672
015636 001405
015640
015640 104455
015642 000004
015644 002605

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T30::  BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
      JSR    PC,SLMODR          ;SELECT MODE REGISTER VIA GDAL BITS 2:0
      ;CLEAR ALL BITS IN THE MODE REGISTER.  MODE REGISTER BIT 11 ON A ZERO
      ;WILL SELECT 16 BIT ADDRESS MODE FOR THE PAUSE STATE MACHINE.
      CLR    R6LOAD              ;SETUP TO CLEAR ALL BITS
      JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK MODE REGISTER
      BEQ    1$                 ;IF LOADED OK THEN CONTINUE
      ERRDF  4,MODREG,R06ERR    ;MODE REGISTER NOT EQUAL EXPECTED
      TRAP   C$ERDF
      .WORD  4
      .WORD  MODREG
      .WORD  R06ERR
      CKLOOP
      TRAP   C$CLP1
      ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
      1$: JSR    PC,SLHDAL        ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
      ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL REGISTER BITS TO A
      ;ZERO.  WHEN HDAL2 H IS SET TO A ONE, THE PROGRAM CAN GENERATE THE T-11
      ;TIMING AND CONTROL SIGNALS.
      MOV    #HDAL2,R6LOAD      ;SETUP BIT TO BE LOADED
      JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ    2$                 ;IF LOADED OK THEN CONTINUE
      ERRDF  4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
      TRAP   C$ERDF
      .WORD  4
      .WORD  HDALRG
  
```

TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

```

6327 015646 005020          .WORD  R06ERR
6328 015650                CKLOOP
6329 015650 104406          TRAP   C$CLP1
6330
6331                        ;SET ADAL REGISTER BIT 4 TO A ONE AND ALL OTHER ADAL REGISTER BITS TO A
6332                        ;ZERO. WHEN A PULSE IS ISSUED ON XRAS H AND ADAL4 H IS SET TO A ONE,
6333                        ;THE PAUSE MODE FLIP-FLOP WILL BE CLOCKED TO THE RUN MODE. WHEN THE
6334                        ;PAUSE MODE FLIP-FLOP IS SET TO THE RUN MODE, THE SIGNAL PAUSE L WILL
6335                        ;BE ASSERTED LOW. ADAL8 H ON A ZERO WILL CAUSE THE SIGNAL TOBRK H TO
6336                        ;BE ASSERTED LOW. WHEN THE SIGNAL TOBRK H IS ASSERTED LOW, THE SIGNAL
6337                        ;BRK H WILL ALSO BE ASSERTED LOW.
6338
6339 015652 012737 000020 002330 2$:  MOV   #ADAL4,R2LOAD          ;SETUP BIT TO BE LOADED
6340 015660 004737 006614                JSR   PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REGISTER
6341 015664 001405                BEQ   3$                ;IF LOADED OK THEN CONTINUE
6342 015666                                ERRDF 2,ADALRG,R2EROR      ;ADAL REGISTER NOT EQUAL EXPECTED
6343 015666 104455                TRAP  C$ERDF
6344 015670 000002                .WORD 2
6345 015672 002513                .WORD ADALRG
6346 015674 004770                .WORD R2EROR
6347 015676                                CKLOOP
6348 015676 104406                TRAP  C$CLP1
6349
6350                        ;TOGGLE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN THE VDAL
6351                        ;REGISTER. A PULSE ON INVD L WILL CLEAR ALL THE FLIP-FLOPS ON THE
6352                        ;MODULE EXCEPT THE SINGLE STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR
6353                        ;BREAK FLIP-FLOP. A PULSE ON INVD L WILL ALSO SET THE PAUSE MODE FLIP-
6354                        ;FLOP TO THE RUN MODE, THUS ASSERTING THE SIGNAL PAUSE L TO THE LOW STATE.
6355                        ;A PULSE ON INVD L WILL ALSO RESET THE TIMEOUT BREAK ONE-SHOT.
6356
6357 015700 005037 002334 3$:  CLR   R4LOAD            ;SETUP TO CLEAR VDAL R/W BITS
6358 015704 004737 007712                JSR   PC,CLRPSM         ;GO PULSE INVD L VIA VDAL2 H
6359
6360                        ;SET ADAL REGISTER BIT 8 TO A ONE. ADAL8 H ON A ONE WILL ENABLE THE
6361                        ;SIGNAL TOBRK H TO CONTROL REGISTER 0 AND TO THE BRK H LOGIC. AT THIS
6362                        ;POINT IN TIME, THE TIMEOUT BREAK ONE SHOT HAS NOT BEEN FIRED BY THE
6363                        ;SIGNAL DFET H, THEREFORE, THE SIGNAL TOBRK H WILL BE ASSERTED HIGH
6364                        ;WHEN ADAL8 H IS ASSERTED HIGH (1). WHEN THE SIGNAL TOBRK H IS ASSERTED
6365                        ;HIGH, THE SIGNAL BRK H WILL ALSO BE ASSERTED HIGH.
6366
6367 015710 052737 000400 002330  BIS   #ADAL8,R2LOAD      ;SETUP BIT TO BE LOADED
6368 015716 004737 006614                JSR   PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REGISTER
6369 015722 001405                BEQ   4$                ;IF LOADED OK THEN CONTINUE
6370 015724                                ERRDF 2,ADALRG,R2EROR      ;ADAL REGISTER NOT EQUAL EXPECTED
6371 015724 104455                TRAP  C$ERDF
6372 015726 000002                .WORD 2
6373 015730 002513                .WORD ADALRG
6374 015732 004770                .WORD R2EROR
6375 015734                                CKLOOP
6376 015734 104406                TRAP  C$CLP1
6377
6378                        ;READ CONTROL REGISTER 0 AND CHECK THAT THE SIGNAL TOBRK H IS SET TO
6379                        ;A ONE WHEN THE ONE SHOT HAS NOT BEEN FIRED AND THE SIGNAL ADAL8 H IS
6380                        ;ASSERTED HIGH.
6381
6382 015736 052737 000100 002322 4$:  BIS   #TOBRK,ROGOOD      ;EXPECT TOBRK H TO BE A ONE
  
```

6383	015744	004737	006570		JSR	PC,READRO	:READ AND CHECK GDAL REGISTER
6384	015750	001405			BEQ	5\$:IF OK THEN CONTINUE
6385	015752				ERRDF	1,GDALRG,ROEROR	:TOBRK H PROBABLY NOT A ONE
6386	015752	104455			TRAP	C\$ERDF	
6387	015754	000001			.WORD	1	
6388	015756	002406			.WORD	GDALRG	
6389	015760	00475.			.WORD	ROEROR	
6390	015762				CKLOOP		
6391	015762	104406			TRAP	C\$CLP1	
6392							
6393							:READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE MACHINE FLIP-
6394							:FLOPS DID NOT CHANGE STATE WHEN THE SIGNALS TOBRK H AND BRK H WERE
6395							:ASSERTED HIGH.
6396							
6397	015764	004737	006654	5\$:	JSR	PC,READR4	:READ VDAL AND PAUSE STATE MACHINE
6398	015770	001405			BEQ	6\$:IF OK THEN CONTINUE
6399	015772				ERRDF	3,VDALRG,R4EROR	:VDAL OR PAUSE STATE MACHINE ERROR
6400	015772	104455			TRAP	C\$ERDF	
6401	015774	000003			.WORD	3	
6402	015776	002537			.WORD	VDALRG	
6403	016000	005004			.WORD	R4EROR	
6404	016002				CKLOOP		
6405	016002	104406			TRAP	C\$CLP1	
6406							
6407							:TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. WHEN
6408							:XRAS H IS PULSED AND FETCT H IS ASSERTED LOW, THE EDFET FLIP-FLOP
6409							:AND THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO.
6410							:WHEN EDFET FLIP-FLOP IS CLEARED AND A PULSE IS ISSUED ON RASP H,
6411							:NO PULSE SHOULD OCCUR ON THE SIGNAL DFET H. A PULSE ON XRAS H
6412							:CAUSES THE SIGNAL RASP H TO BE PULSED. IF NO PULSE OCCURS ON THE
6413							:SIGNAL DFET H, THE TIMEOUT ONE SHOT WILL REMAIN UNFIRED AND THE
6414							:SIGNAL TOBRK H WILL REMAIN HIGH. THE PAUSE MODE FLIP-FLOP WILL
6415							:BE CLOCKED TO THE RUN MODE BY XRAS H AS A RESULT OF ADAL4 H BEING
6416							:ASSERTED HIGH (1). WHEN THE PAUSE MODE ONE SHOT IS SET TO RUN
6417							:MODE, THE SIGNAL PAUSE L WILL BE ASSERTED LOW.
6418							
6419	016004	004737	007272	6\$:	JSR	PC,XRAS	:GO PULSE XRAS H VIA HDAL12 H
6420							
6421							:READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL TOBRK H IS STILL
6422							:SET TO A ONE AFTER A PULSE WAS ISSUED ON XRAS H AND THE EDFET FLIP-
6423							:FLOP WAS CLOCKED TO A ZERO. THE TIMEOUT BREAK ONE SHOT SHOULD NOT
6424							:BE FIRED BY THE SIGNAL DFET H WHEN THE EDFET FLIP-FLOP IS CLEARED.
6425							
6426	016010	004737	006570		JSR	PC,READRO	:READ AND CHECK GDAL REGISTER
6427	016014	001405			BEQ	7\$:IF OK THEN CONTINUE
6428	016016				ERRDF	1,GDALRG,ROEROR	:TOBRK ONE SHOT PROBABLY FIRED
6429	016016	104455			TRAP	C\$ERDF	
6430	016020	000001			.WORD	1	
6431	016022	002406			.WORD	GDALRG	
6432	016024	004754			.WORD	ROEROR	
6433	016026				CKLOOP		
6434	016026	104406			TRAP	C\$CLP1	
6435							
6436							:READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
6437							:DID NOT GET SET TO A ONE WHEN THE EDFET FLIP-FLOP IS CLEARED AND THE
6438							:BRK H SIGNAL IS ASSERTED HIGH. JUST AS A NOTE, THE SIGNAL PAUSE L

TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

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6439                                     ;SHOULD BE ASSERTED LOW.
6440
6441 016030 004737 006654      7$: JSR    PC,READR4      ;READ VDAL AND PAUSE STATE MACHINE
6442 016034 001405             BEQ    8$              ;IF OK THEN CONTINUE
6443 016036                     ERRDF  3,VDALRG,R4EROR  ;VDAL OR PAUSE STATE MACHINE ERROR
6444 016036 104455             TRAP   C$ERDF
6445 016040 000003             .WORD  3
6446 016042 002537             .WORD  VDALRG
6447 016044 005004             .WORD  R4EROR
6448 016046                     CKLOOP
6449 016046 104406             TRAP   C$CLP1
6450
6451                                     ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. A PULSE
6452                                     ;ON XCAS H WILL CLOCK THE LEVEL OF THE SIGNAL PB H, WHICH SHOULD BE
6453                                     ;LOW AS A RESULT OF EDFET H BEING ASSERTED LOW, INTO THE PAUSE STATE
6454                                     ;SYNC FLIP-FLOP, THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A
6455                                     ;ZERO.
6456
6457 016050 004737 007376      8$: JSR    PC,XCAS              ;GO PULSE XCAS H VIA HDAL13 H
6458
6459                                     ;READ CONTROL REGISTER 0 TO CHECK THAT A PULSE ON XCAS H DID NOT
6460                                     ;CAUSE THE TIME OUT BREAK ONE SHOT TO BE FIRED. THIS CONDITION SHOULD
6461                                     ;NEVER EXISTS.
6462
6463 016054 004737 006570      JSR    PC,READR0      ;READ AND CHECK GDAL REGISTER
6464 016060 001405             BEQ    9$              ;IF NO CHANGES THEN CONTINUE
6465 016062                     ERRDF  1,GDALRG,ROEROR  ;TIMEOUT BREAK ONE SHOT FIRED
6466 016062 104455             TRAP   C$ERDF
6467 016064 000001             .WORD  1
6468 016066 002406             .WORD  GDALRG
6469 016070 004754             .WORD  ROEROR
6470 016072                     CKLOOP
6471 016072 104406             TRAP   C$CLP1
6472
6473                                     ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
6474                                     ;WAS CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL EDFET H BEING ASSERTED
6475                                     ;LOW.
6476
6477 016074 004737 006654      9$: JSR    PC,READR4      ;READ VDAL AND PAUSE STATE MACHINE
6478 016100 001405             BEQ    10$             ;IF OK THEN CONTINUE
6479 016102                     ERRDF  3,VDALRG,R4EROR  ;VDAL OR PAUSE STATE MACHINE ERROR
6480 016102 104455             TRAP   C$ERDF
6481 016104 000003             .WORD  3
6482 016106 002537             .WORD  VDALRG
6483 016110 005004             .WORD  R4EROR
6484 016112                     CKLOOP
6485 016112 104406             TRAP   C$CLP1
6486
6487                                     ;SET THE SIGNAL ADAL8 H TO A ZERO. WHEN ADAL8 H IS A ZERO, THE SIGNAL
6488                                     ;TOBRK H WILL BE ASSERTED LOW WHICH WILL CAUSE THE SIGNAL BRK H TO BE
6489                                     ;ASSERTED LOW.
6490
6491 016114 042737 000400 002330 10$: BIC    #ADAL8,R2LOAD  ;SETUP TO CLEAR ADAL BIT 8
6492 016122 004737 006614      JSR    PC,LDRDR2      ;GO LOAD, READ AND CHECK ADAL REGISTER
6493 016126 001405             BEQ    11$             ;IF LOADED OK THEN CONTINUE
6494 016130                     ERRDF  2,ADALRG,R2EROR  ;ADAL REGISTER NOT EQUAL EXPECTED

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6495 016130 104455 TRAP C$ERDF
6496 016132 000002 .WORD 2
6497 016134 002513 .WORD ADALRG
6498 016136 004770 .WORD R2EROR
6499 016140 CKLOOP
6500 016140 104406 TRAP C$CLP1
6501
6502 ;READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL TOBRK H IS READ AS
6503 ;A ZERO WHEN ADAL REGISTER BIT 8 IS SET TO A ZERO.
6504
6505 016142 042737 000100 002322 11$: BIC #TOBRK,ROGOOD ;EXPECT TOBRK H TO BE A ZERO
6506 016150 004737 006570 JSR PC,READRO ;READ AND CHECK GDAL REGISTER
6507 016154 001405 BEQ 12$ ;IF OK THEN CONTINUE
6508 016156 ERRDF 1,GDALRG,ROEROR ;TOBRK K PROBABLY STILL HIGH
6509 016156 104455 TRAP C$ERDF
6510 016160 000001 .WORD 1
6511 016162 002406 .WORD GDALRG
6512 016164 004754 .WORD ROEROR
6513 016166 CKLOOP
6514 016166 104406 TRAP C$CLP1
6515
6516 ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
6517 ;CHECK THE PAUSE STATE MACHINF FLIP-FLOP'S TO BE CLEARED.
6518
6519 016170 012737 000200 002334 12$: MOV #VDAL7,R4LOAD ;SETUP BIT TO SET FETCT H TO HIGH STATE
6520 016176 004737 006640 JSR PC,LDRDR4 ;GO LOAD, READ AND CHECK VDAL REGISTER
6521 016202 001405 BEQ 13$ ;IF OK THEN CONTINUE
6522 016204 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6523 016204 104455 TRAP C$ERDF
6524 016206 000003 .WORD 3
6525 016210 002537 .WORD VDALRG
6526 016212 005004 .WORD R4EROR
6527 016214 CKLOOP
6528 016214 104406 TRAP C$CLP1
6529
6530 ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. A PULSE
6531 ;ON XRAS H WITH THE SIGNAL FETCT H SET HIGH, WILL CAUSE THE EDFET
6532 ;FLIP-FLOP TO BE CLOCKED TO A ONE, THUS SETTING THE SIGNAL EDFET H TO
6533 ;THE HIGH STATE. THE TIMEOUT BREAK ONE SHOT WILL ALSO BE FIRED AS A
6534 ;RESULT OF A PULSE ON THE SIGNAL DFET H. A PULSE OCCURS ON DFET H AS
6535 ;A RESULT OF THE EDFET FLIP-FLOP BEING SET AND THE SIGNAL RASP H BEING
6536 ;PULSED. THE SIGNAL RASP H IS PULSED VIA A PULSE ON THE SIGNAL XRAS H.
6537
6538 016216 004737 007272 13$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
6539
6540 ;SET THE SIGNAL FETCT H TO THE LOW STATE BY CLEARING VDAL7 H. CHECK
6541 ;THE PAUSE STATE MACHINE FLIP-FLOPS TO BE CLEARED AS A RESULT OF
6542 ;THE SIGNAL BRK H BEING ASSERTED LOW BY ADAL8 H BEING A ZERO AND THE
6543 ;SIGNAL PAUSE L BEING ASSERTED LOW.
6544
6545 016222 042737 000200 002334 BIC #VDAL7,R4LOAD ;SETUP TO SET FETCT H TO LOW STATE
6546 016230 004737 006640 JSR PC,LDRDR4 ;GO LOAD, READ AND CHECK VDAL REGISTER
6547 016234 001405 BEQ 14$ ;IF OK THEN CONTINUE
6548 016236 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6549 016236 104455 TRAP C$ERDF
6550 016240 000003 .WORD 3
  
```


TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

6551	016242	002537				.WORD	VDALRG	
6552	016244	005004				.WORD	R4EROR	
6553	016246					CKLOOP		
6554	016246	104406				TRAP	C\$CLP1	
6555								
6556								
6557								
6558								
6559								
6560								
6561	016250	052737	000400	002330	14\$:	BIS	#ADAL8,R2LOAD	:ENABLE TOBRK H TO BRK H LOGIC
6562	016256	004737	006614			JSR	PC,LDRDR2	:GO LOAD, READ AND CHECK ADAL REGISTER
6563	016262	001405				BEQ	15\$:IF LOADED OK THEN CONTINUE
6564	016264					ERRDF	2,ADALRG,R2EROR	:ADAL REGISTER NOT EQUAL EXPECTED
6565	016264	104455				TRAP	C\$ERDF	
6566	016266	000002				.WORD	2	
6567	016270	002513				.WORD	ADALRG	
6568	016272	004770				.WORD	R2EROR	
6569	016274					CKLOOP		
6570	016274	104406				TRAP	C\$CLP1	
6571								
6572								
6573								
6574								
6575								
6576								
6577	016276	004737	006570		15\$:	JSR	PC,READRO	:READ AND CHECK THE GDAL REGISTER
6578	016302	001405				BEQ	16\$:IF OK THEN CONTINUE
6579	016304					ERRDF	1,GDALRG,ROEROR	:TIMEOUT BREAK ONE SHOT FAILED TO FIRE
6580	016304	104455				TRAP	C\$ERDF	
6581	016306	000001				.WORD	1	
6582	016310	002406				.WORD	GDALRG	
6583	016312	004754				.WORD	ROEROR	
6584	016314					CKLOOP		
6585	016314	104406				TRAP	C\$CLP1	
6586								
6587								
6588								
6589								
6590								
6591								
6592								
6593								
6594	016316	004737	007376		16\$:	JSR	PC,XCAS	:GO PULSE XCAS H VIA HDAL13 H
6595								
6596								
6597								
6598								
6599								
6600	016322	004737	006654			JSR	PC,READR4	:READ VDAL AND PAUSE STATE MACHINE
6601	016326	001405				BEQ	17\$:IF OK THEN CONTINUE
6602	016330					ERRDF	3,VDALRG,R4EROR	:TIMEOUT BREAK ONE SHOT TIMED OUT
6603	016330	104455				TRAP	C\$ERDF	
6604	016332	000003				.WORD	3	
6605	016334	002537				.WORD	VDALRG	
6606	016336	005004				.WORD	R4EROR	

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6607 016340          CKLOC
6608 016340 104406  TRAP   C$CLP1
6609
6610          :SETUP A DELAY TO WAIT FOR THE TIMEOUT BREAK ONE SHOT TO FINISH
6611          :FIRING.  THE TIMEOUT BREAK ONE SHOT, ONCE FIRED, WILL NOT TIMEOUT
6612          :UNTIL APPROXIMATELY ONE SECOND HAS OCCURED.
6613
6614 016342 012702 000002      17$:  MOV   #2,R2          :SETUP DOUBLE PRECISION COUNTER
6615 016346 005001          CLR   R1            :SETUP SINGLE PRECISION COUNTER
6616 016350 017703 163724      18$:  MOV   @REGO,R3       :READ GDAL REGISTER
6617 016354 032703 000100      BIT   #TOBRK,R3     :CHECK IF TIMEOUT BREAK BIT SET
6618 016360 001004          BNE   19$          :IF YES THEN GO READ REGISTER AGAIN
6619 016362 005301          DEC   R1            :DECREMENT THE FIRST COUNTER
6620 016364 001371          BNE   18$          :IF NOT 0 THEN DO AGAIN
6621 016366 005302          DEC   R2            :DECREMENT THE SECOND COUNTER
6622 016370 001367          BNE   18$          :IF NOT 0 THEN DO AGAIN
6623 016372 052737 000100 002322 19$:  BIS   #TOBRK,ROGOOD :EXPECT TOBRK H TO BE SET TO A ONE
6624 016400 004737 006570      JSR   PC,READRO    :READ AND CHECK GDAL REGISTER
6625 016404 001405          BEQ   20$          :IF OK THEN CONTINUE
6626 016406          ERRDF 1,GDALRG,ROEROR :TOBRK H PROBABLY NOT SET
6627 016406 104455          TRAP  C$ERDF
6628 016410 000001          .WORD 1
6629 016412 002406          .WORD GDALRG
6630 016414 004754          .WORD ROEROR
6631 016416          CKLOOP
6632 016416 104406          TRAP  C$CLP1
6633
6634          :READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-
6635          :FLOP WAS SET TO A ONE AS A RESULT OF BRK H BEING ASSERTED HIGH BY
6636          :TOBRK H AND THE EDFET FLIP-FLOP BEING SET TO A ONE.
6637
6638 016420 052737 001000 002336 20$:  BIS   #VDAL9,R4GOOD :EXPECT PSMW H TO BE A ONE
6639 016426 004737 006654      JSR   PC,READR4    :READ VDAL AND PAUSE STATE MACHINE
6640 016432 001405          BEQ   21$          :IF OK THEN CONTINUE
6641 016434          ERRDF 3,VDALRG,R4EROR :PSMW H NOT SET VIA BRK H + EDFET H
6642 016434 104455          TRAP  C$ERDF
6643 016436 000003          .WORD 3
6644 016440 002537          .WORD VDALRG
6645 016442 005004          .WORD R4EROR
6646 016444          CKLOOP
6647 016444 104406          TRAP  C$CLP1
6648
6649          :TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE SIGNAL
6650          :XCAS H WILL CLOCK THE LEVEL OF PB H, WHICH SHOULD BE ASSERTED HIGH AS
6651          :A RESULT OF BRK H AND EDFET H BEING ASSERTED HIGH, INTO THE PAUSE
6652          :STATE SYNC FLIP-FLOP, THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO
6653          :A ONE.
6654
6655 016446 004737 007376      21$:  JSR   PC,XCAS      :GO PULSE XCAS H VI. HDAL13 H
6656
6657          :READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
6658          :WAS SET TO A ONE BY XCAS H WHEN BRK H AND EDFET H WERE ASSERTED HIGH.
6659
6660 016452 052737 002000 002336      BIS   #VDAL10,R4GOOD :EXPECT EPSF H TO BE A ONE
6661 016460 004737 006654      JSR   PC,READR4    :READ VDAL AND PAUSE STATE MACHINE
6662 016464 001405          BEQ   22$          :IF OK THEN CONTINUE

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6663	016466					ERRDF	3,VDALRG,R4EROR		:EPSF H NOT 1 VIA BRK H AND EDFET H
6664	016466	104455				TRAP	C\$ERDF		
6665	016470	000003				WORD	3		
6666	016472	002537				.WORD	VDALRG		
6667	016474	005004				.WORD	R4EROR		
6668	016476					CKLOOP			
6669	016476	104406				TRAP	C\$CLP1		
6670									
571									
6672									:SET THE SIGNALS TOBRK H AND BRK H TO THE LOW STATE BY CLEARING ADAL
6673									:REGISTER BIT 8.
6674	016500	042737	000400	002330	22\$:	BIC	#ADAL8,R2LOAD		:SETUP BIT TO BE CLEARED
6675	016506	004737	006614			JSR	PC,LDRDR2		:GO LOAD, READ AND CHECK ADAL REGISTER
6676	016512	001405				BEQ	23\$:IF LOADED OK THEN CONTINUE
6677	016514					ERRDF	2,ADALRG,R2EROR		:ADAL REGISTER NOT EQUAL EXPECTED
6678	016514	104455				TRAP	C\$ERDF		
6679	016516	000002				.WORD	2		
6680	016520	002513				.WORD	ADALRG		
6681	016522	004770				.WORD	R2EROR		
6682	016524					CKLOOP			
6683	016524	104406				TRAP	C\$CLP1		
6684									
6685									:TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL12 H. THE
6686									:SIGNAL XCAS H WILL CLOCK THE LEVEL OF PB H, WHICH SHOULD BE ASSERTED
6687									:LOW AS A RESULT OF BRK H AND PAUSE L BEING ASSERTED LOW, INTO THE
6688									:PAUSE STATE SYNC FLIP-FLOP, THUS CLEARING THE PAUSE STATE SYNC FLIP-
6689									:FLOP. THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP, WHICH
6690									:WAS HIGH, WILL BE CLOCKED INTO THE 16 BIT ADDRESS FLIP-FLOP BY XCAS H,
6691									:THUS SETTING THE 16 BIT ADDRESS FLIP-FLOP TO A ONE.
6692									
6693	016526	004737	007376		23\$:	JSR	PC,XCAS		:GO PULSE XCAS H VIA HDAL13 H
6694									
6695									:READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
6696									:WAS CLOCKED TO A ZERO BY XCAS H WHEN THE SIGNAL BRK H WAS ASSERTED
6697									:LOW. ALSO CHECK THAT THE 16 BIT ADDRESS FLIP-FLOP WAS CLOCKED TO
6698									:A ONE.
6699									
6700	016532	042737	002000	002336		BIC	#VDAL10,R4GOOD		:EXPECT EPSF H TO BE A 0
6701	016540	052737	004000	002336		BIS	#VDAL11,R4GOOD		:EXPECT EPFN H TO BE A 1
6702	016546	004737	006654			JSR	PC,READR4		:READ VDAL AND PAUSE STATE MACHINE
6703	016552	001405				BEQ	24\$:IF OK THEN CONTINUE
6704	016554					ERRDF	3,VDALRG,R4EROR		:BRK H PROBABLY NOT CLEARED
6705	016554	104455				TRAP	C\$ERDF		
6706	016556	000003				.WORD	3		
6707	016560	002537				.WORD	VDALRG		
6708	016562	005004				.WORD	R4EROR		
6709	016564					CKLOOP			
6710	016564	104406				TRAP	C\$CLP1		
6711									
6712									:SET ADAL REGISTER BIT 8 TO A ONE. THIS WILL ENABLE THE SIGNALS
6713									:TOBRK H AND BRK H TO BE ASSERTED HIGH.
6714									
6715	016566	052737	000400	002330	24\$:	BIS	#ADAL8,R2LOAD		:SETUP BIT TO BE LOADED
6716	016574	004737	006614			JSR	PC,LDRDR2		:GO LOAD, READ AND CHECK ADAL REGISTER
6717	016600	001405				BEQ	25\$:IF LOADED OK THEN CONTINUE
5718	016602					ERRDF	2,ADALRG,R2EROR		:ADAL REGISTER NOT EQUAL EXPECTED

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6719 016602 104455 TRAP C$ERDF
6720 016604 000002 .WORD 2
6721 016606 002513 .WORD ADALRG
6722 016610 004770 .WORD R2EROR
6723 016612 CKLOOP
6724 016612 104406 TRAP C$CLP1
6725
6726 ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
6727 ;WHEN BRK H AND FETCT H ARE ASSERTED HIGH, THE PAUSE MODE FLIP-FLOP
6728 ;WILL BE FORCED INTO PAUSE MODE, THUS SETTING THE SIGNAL PAUSE L TO
6729 ;THE HIGH STATE.
6730
6731 016614 052737 000200 002334 25$: BIS #VDAL7,R4LOAD ;SETUP BIT TO BE LOADED
6732 016622 052737 000200 002336 BIS #VDAL7,R4GOOD ;SETUP BIT TO BE EXPECTED ON READ
6733 016630 004737 006646 JSR PC,LDRD4R ;GO LOAD AND READ VDAL REGISTER
6734 016634 001405 BEQ 26$ ;IF OK THEN CONTINUE
6735 016636 ERRDF 3,VDALRG,R4EROR ;PAUSE STATE MACHINE CHANGED
6736 016636 104455 TRAP C$ERDF
6737 016640 000003 .WORD 3
6738 016642 002537 .WORD VDALRG
6739 016644 005004 .WORD R4EROR
6740 016646 CKLOOP
6741 016646 104406 TRAP C$CLP1
6742
6743 ;SET ADAL REGISTER BIT 8 TO A ZERO TO ASSERT THE SIGNALS BRK H AND
6744 ;TOBRK H TO THE LOW STATE.
6745
6746 016650 042737 000400 002330 26$: BIC #ADAL8,R2LOAD ;SETUP BIT TO BE CLEARED
6747 016656 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
6748 016662 001405 BEQ 27$ ;IF OK THEN CONTINUE
6749 016664 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
6750 016664 104455 TRAP C$ERDF
6751 016666 000002 .WORD 2
6752 016670 002513 .WORD ADALRG
6753 016672 004770 .WORD R2EROR
6754 016674 CKLOOP
6755 016674 104406 TRAP C$CLP1
6756
6757 ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. THE
6758 ;SIGNAL XCAS H SHOULD CLOCK THE PAUSE STATE SYNC FLIP-FLOP TO A ONE
6759 ;AS A RESULT OF PAUSE L BEING ASSERTED HIGH AND THE EDFET FLIP-FLOP
6760 ;BEING SET TO A ONE. THE SIGNAL PAUSE L SHOULD HAVE BEEN SET HIGH
6761 ;AS A RESULT OF THE SIGNAL BRK H AND FETCT H BEING ASSERTED HIGH
6762 ;PREVIOUSLY. THE 16 BIT ADDRESS FLIP-FLOP SHOULD BE CLOCKED TO A
6763 ;ZERO AS A RESULT OF XCAS H AND THE PREVIOUS OUTPUT OF THE PAUSE STATE
6764 ;SYNC FLIP-FLOP, WHICH WAS LOW.
6765
6766 016676 004737 007376 27$: JSR PC,XCAS ;GO PULSE XCAS H VIA HDAL13 H
6767
6768 ;READ THE VDAL REGISTER TO CHECK THAT BRK H AND FETCT H BEING ASSERTED
6769 ;HIGH PREVIOUSLY CAUSED THE PAUSE MODE FLIP-FLOP TO BE SET TO THE
6770 ;PAUSE MODE FROM THE RUN MODE. WHEN THE PAUSE MODE FLIP-FLOP IS SET
6771 ;TO THE PAUSE MODE, THE SIGNAL PAUSE L WILL BE ASSERTED HIGH.
6772
6773 016702 042737 004000 002336 BIC #VDAL11,R4GOOD ;EXPECT EPFN H TO BE A 0
6774 016710 052737 002000 002336 BIS #VDAL10,R4GOOD ;EXPECT EPSF H TO BE A 1
```

TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

6775	016716	004737	006654	JSR	PC,READR4	:READ VDAL AND PAUSE STATE MACHINE
6776	016722	001405		BEQ	28\$:IF OK THEN CONTINUE
6777	016724			ERRDF	3,VDALRG,R4EROR	:PAUSE L PROBABLY NOT SET HIGH
6778	016724	104455		TRAP	C\$ERDF	
6779	016726	000003		.WORD	3	
6780	016730	002537		.WORD	VDALRG	
6781	016732	005004		.WORD	R4EROR	
6782	016734			CKLOOP		
6783	016734	104406		TRAP	C\$CLP1	
6784						
6785						:CLEAR THE SIGNAL FETCT H AND PULSE THE SIGNAL INVD L VIA VDAL2 H.
6786						:THE SIGNAL INVD L WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS
6787						:TO BE CLEARED.
6788						
6789	016736	005037	002334	28\$: CLR	R4LOAD	:SETUP TO CLEAR FETCT H
6790	016742	004737	007712	JSR	PC,CLRPSM	:GO PULSE INVD L VIA VDAL2 H
6791						
6792	016746			ENDSEG		
6793	016746			10000\$:		
6794	016746	104405		TRAP	C\$ESEG	
6795	016750			ENDTST		
6796	016750			L10060:		
6797	016750	104401		TRAP	C\$ETST	
6798						
6799						

TEST 31: PAUSE STATE MACHINE - 16 BIT ADDRESS - RUN MODE

.SBTTL TEST 31: PAUSE STATE MACHINE - 16 BIT ADDRESS - RUN MODE

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: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 'RUN' AND 16 BIT ADDRESS MODE.
: WHEN THE PAUSE STATE MACHINE IS SETUP IN 'RUN' MODE VIA ADAL4 H ON A ONE AND
: A PULSE ON XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK
: CONDITION IS RECEIVED ON THE SIGNAL 'BRK H'. THIS TEST WILL USE THE SINGLE
: STEP BREAK FLIP-FLOP TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK
: THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN THE SINGLE STEP BREAK FLIP-
: FLOP IS CLEARED AND THAT IT CAN BE ENTERED WHEN THE SINGLE STEP BREAK FLIP-
: FLOP IS SET TO A ONE. THE TEST WILL CHECK THAT THE SINGLE STEP BREAK FLIP-
: FLOP ONCE SET, WILL REMAIN LATCHED TO THE SET STATE UNTIL CLEARED BY A PULSE
: BEING ISSUED ON THE SIGNAL 'BRKRES L'. THE TEST WILL SET THE PAUSE STATE
: MACHINE FLIP-FLOP'S: PAUSE STATE WORKING, PAUSE STATE SYNC AND 16 BIT ADDRESS
: VIA THE SIGNALS XRAS H AND XCAS H. ONCE ALL THESE FLIP-FLOPS ARE SET TO THE
: ONE STATE, THE TEST WILL CHECK THAT THEY CAN BE CLEARED BY ISSUING A PULSE ON
: THE SIGNAL 'INVD L'.
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016752
 016752
 016752 004737 005510
 016756 104404
 016760 005037 002330
 016764 004737 007772
 016770 004737 007006
 016774 005037 002342
 017000 004737 006672
 017004 001405
 017006 104455
 017010 000004
 017012 002631
 017014 005020
 017016 104406
 017020 004737 006754

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T31:: BGNTST
      JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP C$BSEG
      ;SET AND CLEAR ADALO H IN THE ADAL REGISTER TO CAUSE A PULSE ON THE SIGNAL
      ;BRKRES L. THE SIGNAL BRKRES L WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP.
      CLR R2LOAD ;SETUP TO CLEAR ALL R/W BITS IN ADAL REG
      JSR PC,BRKRES ;GO PULSE BRKRES L VIA ADALO H
      ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 AND CHECK THAT NO BREAK CONDITIONS
      ;ARE SET IN THE GDAL REGISTER.
      JSR PC,SLMODR ;SELECT THE MODE REG VIA GDAL BITS 2:0
      ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
      ;MODE REGISTER BIT 11 ON A ZERO WILL ENABLE 16 BIT ADDRESS MODE.
      CLR R6LOAD ;SETUP TO LOAD ALL ZEROES.
      JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
      BEQ 1$ ;IF LOADED OK THEN CONTINUE
      ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL EXPECTED
      TRAP C$ERDF
      .WORD 4
      .WORD MODREG
      .WORD R06ERR
      CKLOOP
      TRAP C$CLP1
      ;SELECT THE HDAL REGISTER VIA GGDAL BITS 2:0 IN CONTROL REGISTER 0.
      JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
      ;CLEAR ALL BITS IN THE HDAL REGISTER EXCEPT HDAL2 H. HDAL2 H WILL BE SET
      ;TO A 1 TO ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING + CONTROL SIGNALS
  
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6856
6857 017024 012737 000004 0C2342      MOV      #HDAL2,R6LOAD      ;SETUP BIT TO BE LOADED
6858 017032 004737 006672              JSR      PC,LDRDR6         ;LOAD, READ AND CHECK HDAL REGISTER
6859 017036 001405                      BEQ      2$                ;IF LOADED OK THEN CONTINUE
6860 017040                                ERRDF    4,HDALRG,R06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
6861 017040 104455                      TRAP    C$ERDF
6862 017042 000004                      .WORD   4
6863 017044 002605                      .WORD   HDALRG
6864 017046 005020                      .WORD   R06ERR
6865 017050                                CKLOOP
6866 017050 104406                      TRAP    C$CLP1
6867
6868                                ;TOGGLE THE SIGNAL INV D L BY SETTING AND CLEARING VDAL2 H IN CONTROL
6869                                ;REGISTER 4. INV D L WILL INITIALIZE ALL FLIP-FLOPS ON THE MODULE NOT
6870                                ;CLEARED BY THE SIGNAL BRKRES L. THE SINGLE STEP SYNC FLIP-FLOP WILL
6871                                ;BE PRESET TO A ONE THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE.
6872
6873 017052 005037 002334 2$:          CLR      R4LOAD            ;SETUP TO CLEAR ALL VDAL R/W BITS
6874 017056 004737 007712              JSR      PC,CLRPSM        ;PULSE INV D L VIA VDAL2 H
6875
6876                                ;SET ADAL REGISTER BITS 5 AND 4 TO ONES. ADAL REGISTER BIT 4 ON A ONE
6877                                ;WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE 'RUN MODE' WHEN THE
6878                                ;SIGNAL XRAS H IS PULSED. WHEN THE PAUSE MODE FLIP-FLOP IS SET TO 'RUN
6879                                ;MODE', THE SIGNAL PAUSE L WILL BE ASSERTED LOW, THEREFORE, THE PAUSE
6880                                ;STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDITION IS RECEIVED.
6881                                ;ADAL REGISTER BIT 5 ON A ONE WILL ENABLE THE SINGLE STEP BREAK FLIP-
6882                                ;FLOP TO BE SET WHEN A PULSE IS ISSUED ON THE SIGNAL XRAS H AND THE
6883                                ;SIGNALS FETCT H AND PSM L ARE ASSERTED HIGH.
6884
6885 017062 012737 000060 002330      MOV      #ADAL5!ADAL4,R2LOAD ;SETUP BITS TO BE LOADED
6886 017070 004737 006614              JSR      PC,LDRDR2         ;LOAD, READ AND CHECK ADAL REGISTER
6887 017074 001405                      BEQ      3$                ;IF LOADED OK THEN CONTINUE
6888 017076                                ERRDF    2,ADALRG,R2EROR  ;ADAL REGISTER NOT EQUAL EXPECTED
6889 017076 104455                      TRAP    C$ERDF
6890 017100 000002                      .WORD   2
6891 017102 002513                      .WORD   ADALRG
6892 017104 004770                      .WORD   R2EROR
6893 017106                                CKLOOP
6894 017106 104406                      TRAP    C$CLP1
6895
6896                                ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE
6897                                ;IN CONTROL REGISTER 4'S VDAL REGISTER.
6898
6899 017110 052737 000200 002334 3$:    BIS      #VDAL7,R4LOAD     ;SETUP BIT TO BE LOADED
6900 017116 004737 006640              JSR      PC,LDRDR4         ;LOAD, READ AND CHECK VDAL REGISTER
6901 017122 001405                      BEQ      4$                ;IF LOADED OK THEN CONTINUE
6902 017124                                ERRDF    3,VDALRG,R4EROR  ;VDAL REGISTER NOT EQUAL EXPECTED
6903 017124 104455                      TRAP    C$ERDF
6904 017126 000003                      .WORD   3
6905 017130 002537                      .WORD   VDALRG
6906 017132 005004                      .WORD   R4EROR
6907 017134                                CKLOOP
6908 017134 104406                      TRAP    C$CLP1
6909
6910                                ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. PULSING
6911                                ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH IS HIGH, INTO

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6912 :THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE LOW
6913 :STATE. A PULSE ON XRAS H WILL CLOCK THE STATE OF FETCT H, WHICH IS
6914 :HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
6915 :HIGH STATE. THE SINGLE STEP SYNC FLIP-FLOP WAS PRESET TO A ONE EARLIER
6916 :IN THIS TEST THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE. A PULSE
6917 :ON XRAS H WILL CAUSE THE SINGLE STEP BREAK FLIP-FLOP TO BE SET TO A ONE
6918 :AS A RESULT OF FETCT H, ADALS H AND PSM L BEING ASSERTED HIGH. WHEN THE
6919 :SINGLE STEP BREAK FLIP-FLOP GETS SET TO A ONE, THE SIGNAL 'BRK H' WILL
6920 :BE ASSERTED HIGH WHICH WILL CAUSE THE SIGNAL 'SOP H' TO BE ASSERTED HIGH.
6921 :WHEN THE SIGNALS SOP H AND EDFET H ARE ASSERTED HIGH, THE PAUSE STATE
6922 :WORKING FLIP-FLOP WILL BE PRESET TO A ONE, THUS SETTING THE SIGNALS
6923 :PSMW H AND PSMW L TO THE HIGH AND LOW STATES RESPECTIVELY. THE PAUSE
6924 :MODE FLIP-FLOP WILL BE SET TO PAUSE MODE AS A RESULT OF FETCT H AND
6925 :BRK H BEING ASSERTED HIGH. THE SIGNAL PAUSE L WILL BE ASSERTED HIGH
6926 :AS A RESULT OF THE PAUSE MODE FLIP-FLOP BEING SET TO PAUSE MODE.
6927
6928 017136 004737 007272 4$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
6929
6930 :READ THE GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
6931 :IS SET TO A ONE AS A RESULT OF A PULSE ON THE SIGNAL XRAS H AND THE
6932 :SIGNALS FETCT H, PSM L AND ADALS H BEING ASSERTED HIGH.
6933
6934 017142 052737 000200 002322 BIS #SSBRK,ROGOOD ;SETUP TO EXPECT SSBRK H TO EQUAL A 1
6935 017150 004737 006570 JSR PC,READRO ;READ AND CHECK GDAL REGISTER
6936 017154 001405 BEQ $$ ;IF OK THEN CONTINUE
6937 017156 ERRDF 1,GDALRG,ROEROR ;SSBRK H PROBABLY NOT SET TO A 1
6938 017156 104455 TRAP C$ERDF
6939 017160 000001 .WORD 1
6940 017162 002406 .WORD GDALRG
6941 017164 004754 .WORD ROEROR
6942 017166 CKLOOP
6943 017166 104406 TRAP C$CLP1
6944
6945 :READ THE VDAL REGISTER TO CHECK THAT SSBRK H BEING ASSERTED HIGH CAUSED
6946 :THE PAUSE STATE WORKING FLIP-FLOP TO GET SET TO A ONE VIA THE SIGNALS
6947 :BRK H, SOP H AND EDFET H.
6948
6949 017170 052737 001000 002336 5$: BIS #VDAL9,R4GOOD ;EXPECT PSMW H TO BE ASSERTED HIGH
6950 017176 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL REGISTER
6951 017202 001405 BEQ 6$ ;IF OK THEN CONTINUE
6952 017204 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
6953 017204 104455 TRAP C$ERDF
6954 017206 000003 .WORD 3
6955 017210 002537 .WORD VDALRG
6956 017212 005004 .WORD R4EROR
6957 017214 CKLOOP
6958 017214 104406 TRAP C$CLP1
6959
6960 :TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. THE SIGNAL
6961 :XCAS H WILL CLOCK THE SINGLE STEP SYNC FLIP-FLOP TO A ZERO AS A RESULT
6962 :OF THE SIGNAL PSMW L BEING ASSERTED LOW. THIS WILL CAUSE THE SIGNAL
6963 :PSM L TO BE ASSERTED LOW. THE PAUSE STATE SYNC FLIP-FLOP WILL BE SET
6964 :TO A ONE AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH WHEN A
6965 :PULSE IS ISSUED ON XCAS H.
6966
6967 017216 004737 007376 6$: JSR PC,XCAS ;GO PULSE XCAS H VIA HDAL13 H

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6968							
6969							
6970							
6971							
6972	017222	052737	002000	002336			
6973	017230	004737	006654				
6974	017234	001405					
6975	017236						
6976	017236	104455					
6977	017240	000003					
6978	017242	002537					
6979	017244	005004					
6980	017246						
6981	017246	104406					
6982							
6983							
6984							
6985							
6986	017250	004737	006570		7\$:		
6987	017254	001405					
6988	017256						
6989	017256	104455					
6990	017260	000001					
6991	017262	002406					
6992	017264	004754					
6993	017266						
6994	017266	104406					
6995							
6996							
6997							
6998							
6999							
7000							
7001							
7002							
7003	017270	004737	007272		8\$:		
7004							
7005							
7006							
7007							
7008	017274	004737	006570				
7009	017300	001405					
7010	017302						
7011	017302	104455					
7012	017304	000001					
7013	017306	002406					
7014	017310	004754					
7015	017312						
7016	017312	104406					
7017							
7018							
7019							
7020	017314	004737	006654		9\$:		
7021	017320	001405					
7022	017322						
7023	017322	104455					

:READ THE VDAL REGISTER TO CHECK THE THE PAUSE STATE SYNC FLIP-FLOP WAS
 :SET TO A ONE BBY XCAS H WHEN EDFETT H AND SOP H ARE ASSERTED HIGH.

```

BIS      #VDAL10,R4GOOD      :EXPECT EPSF H TO BE SET TO A ONE
JSR      PC,READR4          :READ AND CHECK VDAL REGISTER
BEQ      7$                 :IF OK THEN CONTINUE
ERRDF    3,VDALRG,R4EROR    :EPSF H PROBABLY NOT SET TO A ONE
TRAP     C$ERDF
.WORD    3
.WORD    VDALRG
.WORD    R4EROR
CKLOOP
TRAP     C$CLP1
  
```

:PEAD GDAL REGISTER TO CHECK THAT SINGLE STEP SYNC FLIP-FLOP IS STILL
 :SET TO A ONE AFTER XCAS H IS PULSED. NO CHANGE SHOULD HAVE OCCURED.

```

JSR      PC,READRO          :READ AND CHECK GDAL REGISTER
BEQ      8$                 :IF OK THEN CONTINUE
ERRDF    1,GDALRG,ROEROR    :GDAL REGISTER NOT EQUAL EXPECTED
TRAP     C$ERDF
.WORD    1
.WORD    GDALRG
.WORD    ROEROR
CKLOOP
TRAP     C$CLP1
  
```

:TOGGLE THE SIGNAL XRAS H AGAIN BY SETTING AND CLEARING HDAL12 H. THIS
 :IS DONE TO CHECK THAT ONCE THE SINGLE STEP BREAK FLIP-FLOP IS SET TO
 :A ONE, IT WILL REMAIN SET TO THAT STATE UNTIL CLEARED VIA A PULSE ON THE
 :SIGNAL BRKRES L. AT THIS POINT IN TIME, FETCT H AND ADAL5 H ARE ASSERTED
 :HIGH AND THE SIGNAL PSM L SHOULD BE ASSERTED LOW. THE PAUSE MODE
 :FLIP-FLOP WILL BE HELD IN PAUSE MODE VIA THE SIGNALS BRK H AND FETCT H.

```

JSR      PC,XRAS            :GO PULSE XRAS H VIA HDAL12 H
:READ GDAL REGISTER TO CHECK THAT SSBK H IS STILL ASSERTED HIGH AS A
:RESULT OF IT BEING LATCHED AND A PULSE ON XRAS H.
  
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```

JSR      PC,READRO          :READ AND CHECK GDAL REGISTER
BEQ      9$                 :IF OK THEN CONTINUE
ERRDF    1,GDALRG,ROEROR    :GDAL REGISTER NOT EQUAL EXPECTED
TRAP     C$ERDF
.WORD    1
.WORD    GDALRG
.WORD    ROEROR
CKLOOP
TRAP     C$CLP1
  
```

:READ VDAL REGISTER TO CHECK THAT NO CHANGE OCCURED AFTER PULSING XRAS H.

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JSR      PC,READR4          :READ AND CHECK VDAL REGISTER
BEQ      10$                :IF NO CHANGE THEN CONTINUE
ERRDF    3,VDALRG,R4EROR    :VDAL REGISTER NOT EQUAL EXPECTED
TRAP     C$ERDF
  
```

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 CVDCDB.P11 01-APR-82 14:12 TEST 31: PAUSE STATE MACHINE - 16 BIT ADDRESS - RUN MODE

SEQ 0144

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7024 017324 000003      .WORD 3
7025 017326 002537      .WORD VDALRG
7026 017330 005004      .WORD R4EROR
7027 017332             CKLOOP
7028 017332 104406      TRAP C$CLP1
7029
7030             ;TOGGLE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.
7031             ;A PULSE ON BRKRES L WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP.
7032
7033 017334 004737 007772      10$: JSR PC,BRKRES             ;PULSE BRKRES L VIA ADALO H
7034
7035             ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARING THE SINGLE STEP
7036             ;BREAK FLIP-FLOP. THE SIGNAL SSBK H SHOULD BE ASSERTED LOW.
7037
7038 017340 042737 000200 002322      BIC #SSBRK,ROGOOD      ;SETUP TO EXPECT SSBK H TO BE 0
7039 017346 004737 006570             JSR PC,READRO          ;READ AND CHECK GDAL REGISTER
7040 017352 001405             BEQ 11$                ;IF OK THEN CONTINUE
7041 017354             ERRDF 1,GDALRG,ROEROR      ;VDAL REGISTER NOT EQUAL EXPECTED
7042 017354 104455      TRAP C$ERDF
7043 017356 000001      .WORD 1
7044 017360 002406      .WORD GDALRG
7045 017362 004754      .WORD ROEROR
7046 017364             CKLOOP
7047 017364 104406      TRAP C$CLP1
7048
7049             ;READ VDAL REGISTER TO CHECK THAT NO CHANGE OCCURED AS A RESULT OF
7050             ;PULSING BRKRES L.
7051
7052 017366 004737 006654      11$: JSR PC,READR4          ;READ AND CHECK VDAL REGISTER
7053 017372 001405             BEQ 12$                ;IF NO CHANGE THEN CONTINUE
7054 017374             ERRDF 3,VDALRG,R4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
7055 017374 104455      TRAP C$ERDF
7056 017376 000003      .WORD 3
7057 017400 002537      .WORD VDALRG
7058 017402 005004      .WORD R4EROR
7059 017404             CKLOOP
7060 017404 104406      TRAP C$CLP1
7061
7062             ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THE SINGLE
7063             ;STEP BREAK FLIP-FLOP SHOULD NOT BE SET TO A ONE THIS TIME BECAUSE THE
7064             ;SIGNAL PSM L WAS ASSERTED LOW EARLIER IN THIS TEST WHEN THE PAUSE STATE
7065             ;WORKING FLIP-FLOP WAS SET TO A ONE AND A PULSE WAS ISSUED ON THE SIGNAL
7066             ;XCAS H. THE PAUSE MODE FLIP-FLOP WILL BE SET TO 'RUN MODE' AND THE
7067             ;EDFET FLIP-FLOP WILL BE SET TO A ONE WHEN THE SIGNAL XRAS H IS PULSED.
7068
7069 017406 004737 007272      12$: JSR PC,XRAS             ;GO PULSE XRAS H VIA HDAL12 H
7070
7071             ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP WAS
7072             ;NOT SET TO A ONE WHEN PSM L WAS ASSERTED LOW, FETCT H AND ADAL5 H
7073             ;WERE ASSERTED HIGH AND A PULSE WAS ISSUED ON THE SIGNAL XRAS H.
7074
7075 017412 004737 006570      JSR PC,READRO          ;READ AND CHECK GDAL REGISTER
7076 017416 001405             BEQ 13$                ;IF OK THEN CONTINUE
7077 017420             ERRDF 1,GDALRG,ROEROR      ;CHECK SIGNAL PSM L TO BE LOW
7078 017420 104455      TRAP C$ERDF
7079 017422 000001      .WORD 1

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HARDWARE TESTS MACY11 30A(1052) 01-APR-82 14:48 PAGE 145
 CVCDCB.P11 01-APR-82 14:12 TEST 31: PAUSE STATE MACHINE - 16 BIT ADDRESS - RUN MODE

SEQ 0145

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7080 017424 002406      .WORD  GDALRG
7081 017426 004754      .WORD  ROEROR
7082 017430             CKLOOP
7083 017430 104406      TRAP   C$CLP1
7084
7085                    ;READ VDAL REGISTER TO CHECK THAT NO CHANGES HAVE OCCURED .
7086
7087 017432 004737 006654 13$: JSR    PC,READR4      ;READ AND CHECK VDAL REGISTER
7088 017436 001405             BEQ    14$           ;IF NO CHANGE THEN CONTINUE
7089 017440             ERRDF  3,VDALRC,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7090 017440 104455      TRAP   C$ERDF
7091 017442 000003      .WORD  3
7092 017444 002537      .WORD  VDALRG
7093 017446 005004      .WORD  R4EROR
7094 017450             CKLOOP
7095 017450 104406      TRAP   C$CLP1
7096
7097                    ;LEAVING FETCT H ASSERTED HIGH, PULSE THE SIGNAL INVD L BY SETTING AND
7098                    ;CLEARING VDAL2 H IN THE VDAL REGISTER. A PULSE ON INVD L WILL
7099                    ;INITIALIZE THOSE FLIP-FLOPS ON THE MODULE NOT CLEARED BY BRKRES L.
7100                    ;A PULSE ON INVD L WILL ALSO PRESET THE SINGLE STEP SYNC FLIP-FLOP
7101                    ;SO THAT THE SIGNAL PSM L WILL BE ASSERTED HIGH.
7102
7103 017452 004737 007712 14$: JSR    PC,CLRPSM      ;PULSE INVD L AND LEAVE FETCT H SET
7104
7105                    ;TO CHECK THAT INVD L PRESET THE PAUSE STATE SYNC FLIP-FLOP, THE TEST
7106                    ;WILL PULSE XRAS H AND EXPECT THE SINGLE STEP BREAK FLIP-FLOP TO BE
7107                    ;SET TO A ONE AS A RESULT OF FETCT H, ADAL5 H AND PSM L BEING ASSERTED
7108                    ;HIGH WHEN XRAS H IS PULSED.
7109
7110 017456 004737 007272 JSR    PC,XRAS        ;GO PULSE XRAS H VIA HDAL12 H
7111
7112                    ;READ GDAL REG TO CHECK THAT THE SINGLE STEP BREAK F/F WAS SET TO A ONE.
7113
7114 017462 052737 000200 002322 BIS    #SSBRK,ROGOOD ;EXPECT SSBRK H TO BE SET HIGH
7115 017470 004737 006570 JSR    PC,READR0      ;READ AND CHECK GDAL REGISTER
7116 017474 001405             BEQ    15$           ;IF SET THEN CONTINUE
7117 017476             ERRDF  1,CDALRG,ROEROR ;INVD L PROBABLY DIDN'T PRESET PSM F/F
7118 017476 104455      TRAP   C$ERDF
7119 017500 000001      .WORD  1
7120 017502 002406      .WORD  GDALRG
7121 017504 004754      .WORD  ROEROR
7122 017506             CKLOOP
7123 017506 104406      TRAP   C$CLP1
7124
7125                    ;CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP WAS SET TO A ONE AS A
7126                    ;RESULT OF EDFET H BEING ASSERTED HIGH AND SOP H BEING ASSERTED HIGH
7127                    ;VIA BRK H AND SSBRK H.
7128
7129 017510 052737 001000 002336 15$: BIS    #VDAL9,R4GOOD ;EXPECT PSMW H TO BE A ONE
7130 017516 004737 006654 JSR    PC,READR4      ;READ AND CHECK VDAL REGISTER
7131 017522 001405             BEQ    16$           ;IF OK THEN CONTINUE
7132 017524             ERRDF  3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7133 017524 104455      TRAP   C$ERDF
7134 017526 000003      .WORD  3
7135 017530 002537      .WORD  VDALRG

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7136 017532 005004          .WORD R4EROR
7137 017534                CKLOOP
7138 017534 104406          TRAP C$CLP1
7139
7140                        :PULSE THE SIGNALS BRKRES L AND INV D L BY SETTING AND CLEARING THE
7141                        :SIGNALS ADALO H AND VDAL2 H. BRKRES L WILL CLEAR THE SINGLE STEP
7142                        :BREAK FLIP-FLOP. INV D L WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
7143                        :AND PRESET THE PSM FLIP-FLOP TO A ONE.
7144
7145 017536 004737 007772    16$: JSR PC,BRKRES          :PULSE BRKRES L VIA ADALO H
7146 017542 004737 007712    JSR PC,CLRPSM        :PULSE INV D L VIA VDAL2 H
7147
7148                        :READ GDAL REG TO CHECK THAT BRKRES L CLEARED SINGLE STEP BREAK F/F.
7149
7150 017546 042737 000200 002322 BIC #SSBRK,ROGOOD    :EXPECT SSBRK H TO BE ASSERTED LOW
7151 017554 004737 006570    JSR PC,READRO        :READ AND CHECK GDAL REGISTER
7152 017560 001405          BEQ 17$              :IF CLEARED THEN CONTINUE
7153 017562                ERRDF 1,GDALRG,ROEROR      :GDAL REGISTER NOT EQUAL EXPECTED
7154 017562 104455          TRAP C$ERDF
7155 017564 000001          .WORD 1
7156 017566 002406          .WORD GDALRG
7157 017570 004754          .WORD ROEROR
7158 017572                CKLOOP
7159 017572 104406          TRAP C$CLP1
7160
7161                        :TOGGLE THE SIGNAL XCAS H TO CLOCK THE OUTPUT OF THE PAUSE STATE
7162                        :WORKING FLIP-FLOP, WHICH IS HIGH, INTO THE SINGLE STEP SYNC FLIP-FLOP.
7163                        :THIS SHOULD CAUSE THE SIGNAL PSM L, WHICH IS ALREADY HIGH, TO BE
7164                        :CLOCKED HIGH. THIS IS DONE TO CHECK THAT THE DATA INPUT LEAD TO THE
7165                        :PSM FLIP-FLOP IS NOT FLOATING.
7166
7167 017574 004737 007376    17$: JSR PC,XCAS          :GO PULSE XCAS H VIA HDAL13 H
7168
7169                        :TO CHECK THAT THE PSM FLIP-FLOP WAS SET TO A ONE, TOGGLE THE SIGNAL
7170                        :XCRAS H TO SET THE SINGLE STEP BREAK FLIP-FLOP TO A ONE. THE SIGNALS
7171                        :PSM L, ADAL5 H AND FETCT H SHOULD ALL BBE ASSERTED HIGH.
7172
7173 017600 004737 007272    JSR PC,XRAS          :GO PULSE XCRAS H VIA HDAL12 H
7174
7175                        :READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP WAS
7176                        :SET TO A ONE.
7177
7178 017604 052737 000200 002322 BIS #SSBRK,ROGOOD    :EXPECT SSBRK H TO BE ASSERTED HIGH
7179 017612 004737 006570    JSR PC,READRO        :READ AND CHECK GDAL REGISTER
7180 017616 001405          BEQ 18$              :IF OK THEN CONTINUE
7181 017620                ERRDF 1,GDALRG,ROEROR      :XCAS H FAILED TO CLOCK PSM L F/F TO 1
7182 017620 104455          TRAP C$ERDF
7183 017622 000001          .WORD 1
7184 017624 002406          .WORD GDALRG
7185 017626 004754          .WORD ROEROR
7186 017630                CKLOOP
7187 017630 104406          TRAP C$CLP1
7188
7189                        :PULSE THE SIGNALS BRKRES L AND INV D L BY SETTING AND CLEARING ADALO H
7190                        :AND VDAL2 H. BRKRES L WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP.
7191                        :INV D L WILL INITIALIZE ALL FLIP-FLOPS NOT CLEARED BY BRKRES L. THE

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7192                                     ;PSM FLIP-FLOP WILL BE PRESET TO A ONE VIA THE SIGNAL INVD L. THE SIGNAL
7193                                     ;FETCT H WILL BE SET LOW BY CLEARING VDAL7 H IN THE VDAL REGISTER
7194
7195 017632 004737 007772                18$: JSR      PC, BRKRES                ;PULSE BRKRES L VIA ADALO H
7196
7197 017636 005037 002334                CLR      R4LOAD                ;SET FETCT H TO THE LOW STATE
7198 017642 004737 007712                JSR      PC, CLRPSM            ;GO PULSE INVD L VIA VDAL2 H
7199
7200                                     ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
7201                                     ;WAS CLEARED BY BRKRES L.
7202
7203 017646 042737 000200 002322          BIC      #SSBRK, ROGOOD        ;EXPECT SSBRK H TO BE A 0
7204 017654 004737 006570                JSR      PC, READRO            ;READ AND CHECK GDAL REGISTER
7205 017660 001405                        BEQ      19$                   ;IF OK THEN CONTINUE
7206 017662                                ERRDF   1, GDALRG, ROEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
7207 017662 104455                        TRAP    C$ERDF
7208 017664 000001                        .WORD   1
7209 017666 002406                        .WORD   GDALRG
7210 017670 004754                        .WORD   ROEROR
7211 017672                                CKLOOP
7212 017672 104406                        TRAP    C$CLP1
7213
7214                                     ;PULSE THE SIGNAL XRAS H TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
7215                                     ;WILL NOT GET SET TO A ONE WHEN THE SIGNAL FETCT H IS ASSERTED LOW AND
7216                                     ;THE SIGNALS ADALS H AND PSM L ARE ASSERTED HIGH.
7217
7218 017674 004737 007272                19$: JSR      PC, XRAS                ;GO PULSE XRAS H VIA HDAL12 H
7219
7220                                     ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
7221                                     ;DID NOT GET SET TO A ONE WHEN FETCT H WAS SET LOW, PSM L AND ADALS H
7222                                     ;WERE ASSERTED HIGH AND A PULSE WAS ISSUED ON THE SIGNAL XRAS H.
7223
7224 017700 004737 006570                JSR      PC, READRO            ;READ AND CHECK GDAL REGISTER
7225 017704 001405                        BEQ      20$                   ;IF OK THEN CONTINUE
7226 017706                                ERRDF   1, GDALRG, ROEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
7227 017706 104455                        TRAP    C$ERDF
7228 017710 000001                        .WORD   1
7229 017712 002406                        .WORD   GDALRG
7230 017714 004754                        .WORD   ROEROR
7231 017716                                CKLOOP
7232 017716 104406                        TRAP    C$CLP1
7233
7234                                     ;SET THE SIGNAL FETCT H TO THE HIGH STATE AND CHECK ALL THE OTHER BITS
7235                                     ;IN THE VDAL REGISTER TO BE CLEARED.
7236
7237 017720 012737 000200 002334 20$:    MOV      #VDAL7, R4LOAD        ;SETUP BIT TO SET FETCT H TO HIGH STATE
7238 017726 004737 006640                JSR      PC, LDRDR4            ;LOAD, READ AND CHECK VDAL REGISTER
7239 017732 001405                        BEQ      21$                   ;IF OK THEN CONTINUE
7240 017734                                ERRDF   3, VDALRG, R4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
7241 017734 104455                        TRAP    C$ERDF
7242 017736 000003                        .WORD   3
7243 017740 002537                        .WORD   VDALRG
7244 017742 005004                        .WORD   R4EROR
7245 017744                                CKLOOP
7246 017744 104406                        TRAP    C$CLP1
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7248                                     ;SET ADAL REGISTER BIT 5 TO A ZERO. WHEN THIS BIT IS SET TO A ZERO,
7249                                     ;THE SINGLE STEP BREAK FLIP-FLOP SHOULD NOT GET SET TO A ONE WHEN
7250                                     ;A PULSE IS ISSUED ON THE SIGNAL XRAS H.
7251
7252 017746 042737 000040 002330 21$: BIC #ADAL5,R2LOAD ;SETUP TO CLEAR ADAL REGISTER BIT 5
7253 017754 004737 006614 JSR PC,LDRDR2 ;IF LOADED OK THEN CONTINUE
7254 017760 001405 BEQ 22$ ;IF LOADED OK THEN CONTINUE
7255 017762 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
7256 017762 104455 TRAP C$ERDF
7257 017764 000002 .WORD 2
7258 017766 002513 .WORD ADALRG
7259 017770 004770 .WORD R2EROR
7260 017772 CKLOOP
7261 017772 104406 TRAP C$CLP1
7262
7263                                     ;PULSE THE SIGNAL XRAS H TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
7264                                     ;WILL NOT GET SET WHEN ADAL5 H IS ASSERTED LOW AND FETCT H AND PSM L
7265                                     ;ARE ASSERTED HIGH.
7266
7267 017774 004737 007272 22$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
7268
7269                                     ;READ GDAL REGISTER TO CHECK THAT SINGLE STEP BREAK FLIP-FLOP DID NOT
7270                                     ;GET SET TO A ONE.
7271
7272 020000 004737 006570 JSR PC,READRO ;READ AND CHECK GDAL REGISTER
7273 020004 001405 BEQ 23$ ;IF OK THEN CONTINUE
7274 020006 ERRDF 1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
7275 020006 104455 TRAP C$ERDF
7276 020010 000001 .WORD 1
7277 020012 002406 .WORD GDALRG
7278 020014 004754 .WORD ROEROR
7279 020016 CKLOOP
7280 020016 104406 TRAP C$CLP1
7281
7282                                     ;READ VDAL REGISTER TO CHECK THAT NO CHANGES OCCURED AS A RESULT OF
7283                                     ;PULSING XRAS H WHEN ADAL5 H WAS SET TO A ZERO. SET THE SIGNAL FETCT H
7284                                     ;TO THE LOW STATE.
7285
7286 020020 005037 002334 23$: CLR R4LOAD ;SETUP TO CLEAR FETCT H
7287 020024 004737 006640 JSR PC,LDRDR4 ;LOAD, READ AND CHECK VDAL REGISTER
7288 020030 001404 BEQ 24$ ;IF NO CHANGE THEN CONTINUE
7289 020032 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7290 020032 104455 TRAP C$ERDF
7291 020034 000003 .WORD 3
7292 020036 002537 .WORD VDALRG
7293 020040 005004 .WORD R4EROR
7294 020042 24$: ENDSEG
7295 020042 10000$:
7296 020042 104405 TRAP L$ESEG
7297 020044 ENDTST
7298 020044 L10061:
7299 020044 104401 TRAP C$ETST

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TEST 32: CHECK EDFET F/F TO BE CLEARED VIA XPI L

.SBTTL TEST 32: CHECK EDFET F/F TO BE CLEARED VIA XPI L

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:++
: THIS TEST WILL CHECK THAT THE EDFET FLIP-FLOP CAN BE CLEARED WHEN A PULSE IS
: ISSUED OF THE SIGNAL XPI L. THE TEST WILL SET ADAL4 H TO A ZERO TO CAUSE
: THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN A PULSE IS ISSUED
: ON THE SIGNAL XRAS H. THE TEST WILL SET THE SIGNAL FETCT H TO THE HIGH STATE
: BY SETTING VDAL7 H TO A ONE. THE TEST WILL THEN PULSE XRAS H TO SET THE
: EDFET FLIP-FLOP TO A ONE AND TO SET THE PAUSE MODE FLIP-FLOP TO THE PAUSE MODE.
: WHEN EDFET FLIP-FLOP IS SET TO A ONE AND THE PAUSE MODE FLIP-FLOP IS SET TO
: THE PAUSE MODE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
: THE TEST WILL NOW PULSE THE SIGNAL XPI L TO CLEAR THE EDFET FLIP-FLOP. WHEN
: THE EDFET FLIP-FLOP IS CLEARED, THE SIGNAL PB H WILL BE ASSERTED LOW. THE
: SIGNAL PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE WORKING FLIP-FLOP. THE
: TEST WILL NOW PULSE THE SIGNAL XCAS H. WHEN A PULSE IS ISSUED ON THE SIGNAL
: XCAS H AND THE SIGNAL PB H IS ASSERTED LOW, THE PAUSE STATE SYNC FLIP-FLOP WILL
: BE CLOCKED TO A ZERO. THE SIGNAL XCAS H WILL ALSO CLOCK THE PAUSE STATE WORK-
: ING FLIP-FLOP TO A ONE.
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020046 004737 005510
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020052 104404
020054 004737 007006
020060 005037 002342
020064 004737 006672
020070 001405
020072 104455
020074 000004
020076 002631
020100 005020
020102 104406
020104 005037 002330
020110 004737 007772
020114 005037 002334
020120 004737 007712

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T32:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR

BGNSEG
TRAP C$BSEG
;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

JSR PC,SLMODR ;SELECT MODE REG VIA GDAL BITS 2:0
;LOAD, READ AND CHECK MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES

CLR R6LOAD ;SETUP TO CLEAR ALL BITS IN MODE REG
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO ZERO
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C$CLP1

;GO PULSE BRKRES L BY SETTING AND CLEARING ADALO IN THE ADAL REGISTER.
;ALL OTHER ADAL REGISTER BITS WILL BE SET TO A ZERO.

1$: CLR R2LOAD ;SETUP TO CLEAR ALL ADAL BITS
JSR PC,BRKRES ;GO 0 ADAL REG AND PULSE ADALO H

;PULSE INVD L BY SETTING AND CLEARING VDAL2 H IN THE VDAL REGISTER. THE
;SIGNAL INVD L WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
;CLEARED.

CLR R4LOAD ;SETUP TO CLEAR ALL OTHER R.W BITS
JSR PC,CLRPSM ;GO PULSE INVD L VIA VDAL2 H

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7357
7358           :SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
7359 020124 004737 006754 JSR      PC,SLHDAL           :SELECT HDAL REGISTER VIA GDAL BITS 2:0
7360
7361           :LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL2 H SET TO A ONE.
7362           :HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING
7363           :AND CONTROL SIGNALS.
7364
7365 020130 012737 000004 002342 MOV      #HDAL2,R6LOAD           :SETUP BIT TO BE LOADED
7366 020136 004737 006672 JSR      PC,LDRDR6           :GO LOAD, READ AND CHECK THE HDAL REG
7367 020142 001405 BEQ      2$                  :IF LOADED OK THEN CONTINUE
7368 020144 ERRDF 4,HDALRG,R06ERR :HDAL REGISTER NOT EQUAL EPXECTED
7369 020144 104455 TRAP    C$ERRDF
7370 020146 000004 .WORD 4
7371 020150 002605 .WORD HDALRG
7372 020152 005020 .WORD R06ERR
7373 020154 CKLOOP
7374 020154 104406 TRAP    C$CLP1
7375
7376           :SET VDAL7 H TO A ONE TO CAUSE THE SIGNAL FETCT H TO BE ASSERTED HIGH.
7377
7378 020156 012737 000200 002334 2$: MOV      #VDAL7,R4LOAD           :SETUP BIT TO BE LOADED
7379 020164 004737 006640 JSR      PC,LDRDR4           :GO LOAD, READ AND CHECK THE VDAL REG
7380 020170 001405 BEQ      3$                  :IF LOADED OK THEN CONTINUE
7381 020172 ERRDF 3,VDALRG,R4EROR :VDAL OR PAUSE STATE MACHINE ERROR
7382 020172 104455 TRAP    C$ERRDF
7383 020174 000003 .WORD 3
7384 020176 002537 .WORD VDALRG
7385 020200 005004 .WORD R4EROR
7386 020202 CKLOOP
7387 020202 104406 TRAP    C$CLP1
7388
7389           :TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THE SIGNAL
7390           :XRAS H WILL CLOCK THE STATE OF FETCT H, WHICH IS HIGH, INTO THE EDFET
7391           :FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE. THE
7392           :SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH IS LOW, INTO THE
7393           :PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE HIGH STATE.
7394           :THE SIGNAL SOP H WILL BE ASSERTED HIGH AS A RESULT OF PAUSE L BEING
7395           :ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED HIGH, THE PAUSE
7396           :STATE WORKING FLIP-FLOP WILL BE SET TO A ONE. WHEN SOP H AND EDFET H
7397           :ARE ASSERTED HIGH, THE SIGNAL PB H WILL BE ASSERTED HIGH. THE SIGNAL
7398           :PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
7399
7400 020204 004737 007272 3$: JSR      PC,XRAS           :GO PULSE XRAS H VIA HDAL12 H
7401
7402           :SET VDAL7 H TO A ZERO TO CAUSE THE SIGNAL FETCT H TO BE ASSERTED LOW.
7403           :CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP WAS SET TO A ONE AS A
7404           :RESULT OF SOP H AND EDFET H BEING ASSERTED HIGH.
7405
7406 020210 042737 000200 002334 BIC      #VDAL7,R4LOAD           :SETUP TO CLEAR FETCT H
7407 020216 013737 002334 002336 MOV      R4LOAD,R4GOOD           :COPY DATA LOADED TO DATA EXPECTED
7408 020224 052737 001000 002336 BIS      #VDAL9,R4GOOD           :SETUP TO EXPECT PSMW H TO BE A ONE
7409 020232 004737 006646 JSR      PC,LDRD4R           :GO LOAD, READ AND CHECK VDAL REG
7410 020236 001405 BEQ      4$                  :IF LOADED AND CHECK OK THEN CONTINUE
7411 020240 ERRDF 3,VDALRG,R4EROR :VDAL OR PAUSE STATE MACHINE ERROR

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7412 020240 104455          TRAP  C$ERDF
7413 020242 000003        .WORD 3
7414 020244 002537        .WORD VDALRG
7415 020246 005004        .WORD R4EROR
7416 020250                CKLOOP
7417 020250 104406          TRAP  C$CLP1
7418
7419
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7422
7423
7424
7425 020252 004737 007502    4$: JSR   PC,XPI                :GO PULSE XPI L VIA HDAL15 H
7426
7427
7428
7429
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7431
7432
7433 020256 004737 007376    JSR   PC,XCAS                :GO PULSE XCAS H VIA HDAL13 H
7434
7435
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7437
7438
7439
7440 020262 004737 006654    JSR   PC,READR4              :GO READ AND CHECK THE VDAL REGISTER
7441 020266 001405          BEQ   $$                     :IF NO CHANGE THE CONTINUE
7442 020270                ERRDF 3,VDALRG,R4EROR        :XPI L PROBABLY FAILED TO ZERO EDFET F/F
7443 020270 104455          TRAP  C$ERDF
7444 020272 000003        .WORD 3
7445 020274 002537        .WORD VDALRG
7446 020276 005004        .WORD R4EROR
7447 020300                CKLOOP
7448 020300 104406          TRAP  C$CLP1
7449
7450
7451
7452 020302 005037 002334    5$: CLR   R4LOAD                :SETUP TO EXPECT ALL READ ONLY BITS A 0
7453 020306 004737 007712    JSR   PC,CLRPSM              :GO PULSE INVD L VIA VDAL2 H
7454
7455 020312                ENDSEG
7456 020312                10000$:
7457 020312 104405          TRAP  C$ESEG
7458 020314                ENDTST
7459 020314                L10062:
7460 020314 104401          TRAP  C$ETST
  
```

TEST 33: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - OLD FJA

.SBTTL TEST 33: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - OLD FJA

```

:++
: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE
: PAUSE STATE WORKING FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE
: STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL
: BE CLOCKED TO CNES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND
: CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND
: AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL
: PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE
: TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADALO H WILL BE SET AND CLEARED TO
: CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC
: CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE
: IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.
  
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: THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD
: FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS
: MODE. THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA
: PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000.
: THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS
: REGISTER WHICH IS ENABLED TO THE ADDRESS BUS DURING THIS TEST.
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020316
020316
020316 004737 005510
020322 012701 021562
020326 012702 000010
020332
020332 104404
020334 004737 007006
020340 012737 004000 002342
020346 005037 002346
020352 004737 006672
020356 001405
020360
020360 104455
020362 000004
020364 002631
020366 005020
020370
020370 104406
020372 004737 006754
  
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BGNTST
T33::
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #20$,R1 ;GET ADDRESS OF OLD FJA DATA TABLE
MOV #8.,R2 ;NUMBER OF DATA PATTERNS TO BE TESTED

1$: BGNSEG
TRAP CSBSEG

;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO
;TO A ZERO.

JSR PC,SLMODR ;GO SELECT MODE REG VIA CONTROL REG 0

;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000. MR BIT 11
;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

MOV #MR11,R6LOAD ;SETUP TO SET MR BIT 11
CLR R6MASK ;SETUP TO CHECK ALL 16 BITS
JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
TRAP CSERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP CSCLP1

;SET GDAL1 AND GDALO TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

2$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
  
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7524 020376 012737 001004 002342
7525 020404 004737 006672
7526 020410 001405
7527 020412
7528 020412 104455
7529 020414 000004
7530 020416 002605
7531 020420 005020
7532 020422
7533 020422 104406
7534
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7536
7537
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7539 020424 004737 007072 3$:
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7541
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7545 020430 011137 002342
7546 020434 004737 006672
7547 020440 001405
7548 020442
7549 020442 104455
7550 020444 000004
7551 020446 002735
7552 020450 005020
7553 020452
7554 020452 104406
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7561
7562 020454 005037 002330 4$:
7563 020460 004737 007772
7564
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7569 020464 005037 002334
7570 020470 004737 007712
7571
7572
  
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;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
 ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
 ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
 ;BUS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
 ;TIMING AND CONTROL SIGNALS.

MOV #HDAL9!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
 BEQ 3\$;IF LOADED OK THEN CONTINUE
 ERRDF 4,HDALRG,R06ERR ;HDAL REG NOT EQUAL TO EXPECTED
 TRAP C\$ERDF
 .WORD 4
 .WORD HDALRG
 .WORD R06ERR
 CKLOOP
 TRAP C\$CLP1

;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
 ;ZEROS. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
 ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.

JSR PC,SLDADR ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0

;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
 ;FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252,
 ;052525, 177777 AND 000000.

MOV (R1),R6LOAD ;GET DATA PATTERN FROM TABLE
 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK DIAG ADDR REG
 BEQ 4\$;IF LOADED OK THEN CONTINUE
 ERRDF 4,ADDRRG,R06ERR ;DIAG ADDRESS REG NOT EQUAL EXPECTED
 TRAP C\$ERDF
 .WORD 4
 .WORD ADDR RG
 .WORD R06ERR
 CKLOOP
 TRAP C\$CLP1

;LOAD, READ AND CHECK ADAL REGISTER. ADALO WILL BE SET AND CLEARED
 ;TO CLEAR THE BREAK LOGIC. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
 ;BREAK SIGNAL FROM CAUSING A BREAK CONDITION. ADAL4 H ON A ZERO WILL
 ;CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
 ;SIGNAL XRAS H IS PULSED.

CLR R2LOAD ;SETUP ALL BITS TO BE CLEARED
 JSR PC,BRKRES ;GO PULSE ADALO H TO CLEAR BREAK LOGIC

;SET VDAL2 H TO A ONE AND THEN ZERO. VDAL2 H ON A ONE WILL CLEAR THE
 ;PAUSE STATE MACHINE FLIP-FLOPS AND THE FLIP-FLOPS, TAKE NEW FORCE JUMP
 ;ADDRESS AND THIS CYCLE GETS NEW ADDRESS.

CLR R4LOAD ;SETUP TO CLEAR ALL VDAL BITS
 JSR PC,CLRPSM ;GO PULSE VDAL2 H TO 0 PAUSE STATE F/F'S

;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A ONE

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7573                                     :AND GDAL BITS 2 AND 0 TO ZEROES. ON A WRITE COMMAND TO CONTROL REG 6,
7574                                     :DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS REGISTER AND THE
7575                                     :TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
7576
7577 020474 004737 007040                JSR      PC,SLFJAR                      :SELECT NEW FJA VIA GDAL BITS 2:0
7578
7579                                     :ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA PATTERN
7580 :146063 INTO THE NEW FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB
7581 :H AND WPT1 HB H. THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO
7582 :GET SET VIA THE SIGNAL WPT1 LB H. THE NEW FORCE JUMP ADDRESS REGISTER
7583 :IS WRITTEN WITH DATA TO CHECK THAT THE CORRECT FORCE JUMP ADDRESS REG-
7584 :ISTER IS ENABLED TO THE EODAL BUS WHEN THE 8 BIT ADDRESS FLIP-FLOPS
7585 :ARE SET TO ONES. THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED
7586 :TO THE EODAL BUS DURING THIS TEST.
7587
7588 020500 012777 146063 161600          MOV      #146063,@REG6                  :WRITE NEW FJA WITH DATA VIA WPT1
7589
7590                                     :READ THE VDAL REGISTER TO CHECK THAT THE TAKE NEW FORCE JUMP ADDRESS
7591 :FLIP-FLOP WAS SET TO A ONE VIA WPT1 LB H. THE FLIP-FLOP WILL BE READ
7592 :BACK AS THE SIGNAL TNFJ H.
7593
7594 020506 052737 100000 002336          BIS      #VDAL15,R4GOOD                :SETUP TO EXPECT TNFJ H TO BE A 1
7595 020514 004737 006654                JSR      PC,READR4                      :GO READ VDAL AND PAUSE STATE MACHINE
7596 020520 001405                        BEQ      $$                             :IF TNFJ H SET THEN CONT
7597 020522                                ERRDF   3,VDALRG,R4EROR                :TNFJ H PROBABLY NOT SET
7598 020522 104455                        TRAP    C$ERDF
7599 020524 000003                        .WORD   3
7600 020526 002537                        .WORD   VDALRG
7601 020530 005004                        .WORD   R4EROR
7602 020532                                CKLOOP
7603 020532 104406                        TRAP    C$CLP1
7604
7605                                     :SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
7606 :SET VDAL2 H TO A ONE AND THEN ZERO TO CLEAR THE PAUSE STATE MACHINE
7607 :AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP.
7608
7609 020534 012737 000200 002334 5$:      MOV      #VDAL7,R4LOAD                  :SETUP BIT TO SET FETCT H TO HIGH STATE
7610 020542 004737 007712                JSR      PC,CLRPSM                      :SET FETCT H HIGH AND PULSE VDAL2 H
7611
7612                                     :SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
7613 :TO ONES. BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
7614 :THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L.
7615
7616 020546 004737 006754                JSR      PC,SLHDAL                      :GO SELECT HDAL REG VIA GDAL 2:0
7617
7618                                     :TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
7619 :THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
7620 :HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
7621 :HIGH STATE. THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
7622 :IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
7623 :TO THE HIGH STATE. THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
7624 :SIGNAL PAUSE L IS ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED
7625 :HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
7626 :WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
7627 :PSMW H WILL BE ASSERTED HIGH. THE SIGNAL PSMW H IS READ IN THE VDAL
7628 :REGISTER AS VDAL9 H. WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE

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7629 ;SIGNAL PB H WILL BE ASSERTED HIGH. THE SIGNAL PB H IS THE DATA INPUT
7630 ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
7631 ;
7632 ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED. WHEN THE
7633 ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
7634 ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H. THE SIGNAL DFET H WILL
7635 ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER. AT THE
7636 ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
7637 ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
7638 ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.
7639
7640 020552 012737 001004 002342 MOV #HDAL9,HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
7641 020560 004737 007272 JSR PC,XRAS ;GO PULSE XRAS H VIA SIGNAL HDAL12
7642
7643 ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
7644 ;THE LOW STATE. CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
7645 ;STATE AS A RESULT OF FETCT H AND SOP H BEING ASSERTED HIGH.
7646 ; PAUSE STATE WORKING - PSMW H - 1
7647 ; PAUSE STATE SYNC - EPSF H - 0
7648 ; 8 BIT INSTRUCTION HB - EP8F H - 0
7649 ; 8 BIT ADDRESS LB H - EP8G H - 0
7650 ; 8 BIT ADDRESS HB H - EP8N H - 0
7651
7652 020564 042737 000200 002334 BIC #VDAL7,R4LOAD ;SETUP TO CLEAR FETCT H
7653 020572 013737 002334 002336 MOV R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
7654 020600 052737 001000 002336 BIS #VDAL9,R4GOOD ;EXPECT PSMW H TO BE SET TO A 1
7655 020606 004737 006646 JSR PC,LDRD4R ;GO LOAD, READ AND CHECK VDAL REG
7656 020612 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
7657 020614 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
7658 020614 104455 TRAP C$ERDF
7659 020616 000003 .WORD 3
7660 020620 002537 .WORD VDALRG
7661 020622 005004 .WORD R4EROR
7662 020624 CKLOOP
7663 020624 104406 TRAP C$CLP1
7664
7665 ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
7666 ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
7667 ;SIGNAL 'PB H', WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP,
7668 ;THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE. THE SIGNAL
7669 ;XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-
7670 ;FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS CLOCKING THAT
7671 ;FLIP-FLOP TO A ZERO.
7672
7673 020626 004737 007410 6$: JSR PC,XCASH ;SET XCAS H TO HIGH STATE VIA HDAL13 H
7674
7675 ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
7676 ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET HIGH.
7677 ; PAUSE STATE WORKING - PSMW H - 1
7678 ; PAUSE STATE SYNC - EPSF H - 1
7679 ; 8 BIT INSTRUCTION HB - EP8F H - 0
7680 ; 8 BIT ADDRESS LB - EP8G H - 0
7681 ; 8 BIT ADDRESS HB - EP8N H - 0
7682
7683 020632 052737 002000 002336 BIS #VDAL10,R4GOOD ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
7684 020640 004737 006654 JSR PC,READR4 ;GO READ AND CHECK PAUSE STATE MACHINE

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7685 020644 001405      BEQ      7$                ;IF LOADED OK THEN CONTINUE
7686 020646              ERRDF    3,VDALRG,R4EROR      ;EPSF H PROBABLE NOT SET IN VDAL REG
7687 020646 104455      TRAP    C$ERDF
7688 020650 000003      .WORD   3
7689 020652 002537      .WORD   VDALRG
7690 020654 005004      .WORD   R4EROR
7691 020656              CKLOOP
7692 020656 104406      TRAP    C$CLP1
7693
7694                      ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE LOW
7695                      ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
7696                      ;EODAL BUS AT THE SAME TIME. ON A READ COMMAND TO CONTROL REGISTER 6,
7697                      ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
7698
7699 020660 004737 007122  7$:   JSR      PC,SEODAL                ;SELECT EODAL BUS VIA GDAL BITS 2:0
7700
7701                      ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE SIGNAL PSMW H IS
7702                      ;ASSERTED TO THE HIGH STATE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
7703                      ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH, THE PAUSE STATE SYNC FLIP-
7704                      ;FLOP IS SET TO A ONE, AND MODE REGISTER BIT 11 IS A ONE (8 BIT MODE),
7705                      ;THE SIGNAL EDRL H WILL BE ASSERTED LOW, THUS ENABLING THE LOW BYTE OF
7706                      ;THE 16 BIT INSTRUCTION REGISTER ONTO THE EODAL BUS. THE HIGH BYTE OF
7707                      ;THE 16 BIT INSTRUCTION REGISTER WILL BE DISABLED ON THE EODAL BUS.
7708                      ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH GDAL BITS 2:0
7709                      ;SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL RPT7 L. THE SIGNAL
7710                      ;RPT7 L WILL READBACK THE EODAL BUS ONTO THE LSI-11 BUS.
7711
7712 020664 012737 000137 002342  MOV     #137,R6LOAD          ;SETUP EXPECTED LOW BYTE DATA
7713 020672 012737 177400 002346  MOV     #177400,R6MASK      ;SETUP TO IGNORE HIGH BYTE
7714 020700 004737 006700          JSR     PC,READR6          ;GO READ LOW BYTE OF INSTR REG ON EODAL
7715 020704 001405          BEQ     8$                ;IF INSTR = "JMP" THEN CONTINUE
7716 020706              ERRDF    4,IEODAL,R06ERR      ;EODAL BUS ERROR OR 8 BIT LB INSTR ERROR
7717 020706 104455      TRAP    C$ERDF
7718 020710 000004      .WORD   4
7719 020712 003034      .WORD   IEODAL
7720 020714 005020      .WORD   R06ERR
7721 020716              CKLOOP
7722 020716 104406      TRAP    C$CLP1
7723
7724                      ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
7725                      ;1 AND 0 TO A ONE.
7726
7727 020720 004737 006754  8$:   JSR     PC,SLHDAL                ;SELECT HDAL REG VIA GDAL BITS 2:0
7728
7729                      ;SET THE SIGNAL XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL
7730                      ;REGISTER.
7731
7732 020724 012737 021004 002342  MOV     #HDAL13!HDAL9!HDAL2,R6LCAD ;BITS THAT WERE PREVIOUSLY SET
7733 020732 005037 002346          CLR     R6MASK            ;SETUP TO CHECK ALL BITS
7734 020736 004737 007442          JSR     PC,XCASL          ;SET XCAS H TO LOW STATE VIA HDAL13 H
7735
7736                      ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H. THIS IS DONE
7737                      ;TO SIMULATE A MACHINE CYCLE
7738
7739 020742 004737 007502  JSR     PC,XPI                ;GO PULSE XPI H VIA HDAL15 H
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7741 :TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
7742 :WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
7743 :EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
7744 :EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
7745 :PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
7746 :AND RASP L WILL BE PULSED.
7747 :THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
7748 :SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
7749
7750 020746 004737 007272 JSR PC,XRAS ;GO PULSE XRAS H BY HDAL12
7751
7752 :READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
7753 :TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
7754 : PAUSE STATE WORKING - PSMW H - 1
7755 : PAUSE STATE SYNC - EPSF H - 1
7756 : 8 BIT INSTRUCTION HB - EP8F H - 0
7757 : 8 BIT ADDRESS LB - EP8G H - 0
7758 : 8 BIT ADDRESS HB - EP8N H - 0
7759
7760 020752 004737 006654 JSR PC,READR4 ;CHECK VDAL AND PAUSE STATE MACHINE
7761 020756 001405 BEQ 9$ ;IF OK THEN CONTINUE
7762 020760 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
7763 020760 104455 TRAP C$ERRDF
7764 020762 000003 .WORD 3
7765 020764 002537 .WORD VDALRG
7766 020766 005004 .WORD R4EROR
7767 020770 CKLOOP
7768 020770 104406 TRAP C$CLP1
7769
7770 :SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
7771 :SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE LEVEL OF THE
7772 :SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
7773 :CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO. THE SIGNAL XCAS H
7774 :WILL CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
7775 :INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THAT FLIP-FLOP
7776 :TO A ONE. THE SIGNAL XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE
7777 :8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-FLOP,
7778 :THUS CLOCKING THAT FLIP-FLOP TO A ZERO.
7779
7780 020772 004737 007410 9$: JSR PC,XCASH ;SET XCAS H TO HIGH STATE VIA HDAL13 H
7781
7782 :READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
7783 :FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH
7784 : PAUSE STATE WORKING - PSMW H - 1
7785 : PAUSE STATE SYNC - EPSF H - 0
7786 : 8 BIT INSTRUCTION HB - EP8F H - 1
7787 : 8 BIT ADDRESS LB - EP8G H - 0
7788 : 8 BIT ADDRESS HB - EPFN H - 0
7789
7790 020776 042737 002000 002336 BIC #VDAL10,R4GOOD ;CLEAR BIT FOR EPSF H
7791 021004 052737 010000 002336 BIS #VDAL12,R4GOOD ;SET BIT FOR EP8F H
7792 021012 004737 006654 JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
7793 021016 001405 BEQ 10$ ;IF OK THEN CONTINUE
7794 021020 ERRDF 3,VDALRG,R4EROR ;EP8F H PROBABLY NOT SET IN VDAL REG
7795 021020 104455 TRAP C$ERRDF
7796 021022 000003 .WORD 3

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7797 021024 002537      .WORD  VDALRG
7798 021026 005004      .WORD  R4EROR
7799 021030              CKLOOP
7800 021030 104406      TRAP   C$CLP1
7801
7802                      ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE HIGH
7803                      ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
7804                      ;EODAL BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6,
7805                      ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
7806
7807 021032 004737 007122 10$: JSR    PC,SEODAL      ;SELECT EODAL BUS VIA GDAL BITS 2:0
7808
7809                      ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
7810                      ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
7811                      ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE 8 BIT INSTRUCTION HB
7812                      ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ED8H H WILL BE ASSERTED HIGH,
7813                      ;THUS ENABLING THE HIGH BYTE OF THE 16 BIT INSTRUCTION REGISTER (000)
7814                      ;ONTO THE LOW BYTE OF THE EODAL BUS. WHEN A READ COMMAND IS ISSUED TO
7815                      ;CONTROL REGISTER 6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE
7816                      ;ISSUED ON THE SIGNAL RPT7 L. THE SIGNAL RPT7 L WILL READBACK THE
7817                      ;EODAL BUS ONTO THE LSI-11 BUS.
7818
7819 021036 005037 002342  CLR    R6LOAD      ;EXPECT HIGH BYTE TO BE ZERO
7820 021042 012737 177400  MOV    #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE ON READ
7821 021050 004737 006700  JSR    PC,READR6     ;GO READ 8 BIT HIGH BYTE INSTRUCTION
7822                      ;ON THE EODAL BUS AS LOW BYTE
7823 021054 001405      BEQ    11$          ;IF INSTRUCTION EQUALS 0 THEN CONT
7824 021056      ERRDF  4,IEODAL,R06ERR ;EODAL BUS OR 8 BIT HB INSTR ERROR
7825 021056 104455      TRAP   C$ERRDF
7826 021060 000004      .WORD  4
7827 021062 003034      .WORD  IEODAL
7828 021064 005020      .WORD  R06ERR
7829 021066      CKLOOP
7830 021066 104406      TRAP   C$CLP1
7831
7832                      ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
7833                      ;1 AND 0 TO ONES.
7834
7835 021070 004737 006754 11$: JSR    PC,SLHDAL     ;GO SELECT HDAL REG VIA GDAL BITS 2:0
7836
7837                      ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN THE HDAL
7838                      ;REGISTER.
7839
7840 021074 012737 021004  MOV    #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
7841 021102 005037 002346  CLR    R6MASK      ;SETUP TO CHECK ALL BITS
7842 021106 004737 007442  JSR    PC,XCASL     ;SET XCAS H TO LOW STATE VIA HDAL13 H
7843
7844                      ;TOGGLE THE SIGNAL XPI H BY PULSING THE SIGNAL HDAL15 H. THIS IS DONE
7845                      ;TO SIMULATE A MACHINE CYCLE.
7846
7847 021112 004737 007502  JSR    PC,XPI       ;GO PULSE XPI H VIA HDAL15 H
7848
7849                      ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
7850                      ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
7851                      ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
7852                      ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL

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7853                                     ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
7854                                     ;AND RASP L WILL BE PULSED.
7855                                     ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
7856                                     ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
7857
7858 021116 004737 007272                JSR      PC,XRAS                      ;PULSE XRAS VIA THE SIGNAL HDAL12
7859
7860                                     ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
7861                                     ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
7862                                     ;NO CHANGES SHOULD OCCUR IN THE PAUSE STATE MACHINE WHEN XRAS H PULSED.
7863                                     :      PAUSE STATE WORKING - PSMW H - 1
7864                                     :      PAUSE STATE SYNC - EPSF H - 0
7865                                     :      8 BIT INSTRUCTION HB - EP8F H - 1
7866                                     :      8 BIT ADDRESS LB - EP8G H - 0
7867                                     :      8 BIT ADDRESS HB - EP8N H - 0
7868
7869 021122 004737 006654                JSR      PC,READR4                    ;GO READ VDAL AND PAUSE STATE MACHINE
7870 021126 001405                        BEQ      12$                          ;IF OK THEN CONTINUE
7871 021130                                ERRDF   3,VDALRG,R4EROR              ;PAUSE STATE REGISTERS CHANGED
7872 021130 104455                        TRAP    C$ERDF
7873 021132 000003                        .WORD   3
7874 021134 002537                        .WORD   VDALRG
7875 021136 005004                        .WORD   R4EROR
7876 021140                                CKLOOP
7877 021140 104406                        TRAP    C$CLP1
7878
7879                                     ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
7880                                     ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
7881                                     ;PAUSE STATE SYNC FLIP-FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-
7882                                     ;FLOP, THUS CLEARING THE 8 BIT INSTRUCTION HB FLIP-FLOP. THE PREVIOUS
7883                                     ;OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-FLOP (1) WILL BE CLOCKED INTO
7884                                     ;THE 8 BIT ADDRESS LB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS LB F/F.
7885
7886 021142 004737 007410                12$:   JSR      PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
7887
7888                                     ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
7889                                     ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH.
7890                                     :      PAUSE STATE WORKING - PSMW H - 1
7891                                     :      PAUSE STATE SYNC - EPSF H - 0
7892                                     :      8 BIT INSTRUCTION HB - EP8F H - 0
7893                                     :      8 BIT ADDRESS LB - EP8G H - 1
7894                                     :      8 BIT ADDRESS HB - EP8N H - 0
7895
7896 021146 042737 010000 002336          RIC      #VDAL12,R4GOOD              ;SETUP TO EXPECT EP8F H TO BE 0
7897 021154 052737 020000 002336          BIS      #VDAL13,R4GOOD              ;SETUP TO EXPECT EP8G H TO BE 1
7898 021162 004737 006654                JSR      PC,READR4                    ;GO READ VDAL AND PAUSE STATE MACHINE
7899 021166 001405                        BEQ      13$                          ;IF OK THEN CONTINUE
7900 021170                                ERRDF   ?,VDALRG,R4EROR              ;EP8F H PROBABLY NOT 0 OR EP8G H NOT SET
7901 021170 104455                        TRAP    C$ERDF
7902 021172 000003                        .WORD   3
7903 021174 002537                        .WORD   VDALRG
7904 021176 005004                        .WORD   R4EROR
7905 021200                                CKLOOP
7906 021200 104406                        TRAP    C$CLP1
7907
7908                                     ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE LOW BYTE

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7909                                     ;OF THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
7910                                     ;BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
7911                                     ;BUS WILL BE READBACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
7912
7913 021202 004737 007122                13$: JSR      PC,SEODAL                ;SELECT EODAL BUS VIA GDAL BITS 2:0
7914
7915                                     ;ON THE FIRST PULSE OF XRAS H IN THIS TEST WHEN THE SIGNAL EDFET H WAS
7916                                     ;SET HIGH, THE OLD FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED
7917                                     ;WITH THE DATA PATTERN IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE
7918                                     ;CLOCKING SIGNAL DFET H. AT THIS POINT IN TIME, THE LOW BYTE OF
7919                                     ;THE OLD FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS
7920                                     ;VIA THE SIGNAL OEARL L. THIS SIGNAL IS ASSERTED LOW AS A RESULT OF
7921                                     ;THE "GET NEW ADDRESS" FLIP - FLOP BEING CLEARED AND THE SIGNAL
7922                                     ;EARL H BEING ASSERTED HIGH. THE "GET NEW ADDRESS" FLIP - FLOP
7923                                     ;WAS CLEARED AT THE BEGINNING OF THIS TEST WHEN VDAL2 H WAS SET HIGH.
7924                                     ;THE SIGNAL EARL H IS ASSERTED HIGH AS A RESULT OF THE 8 BIT ADDRESS LB
7925                                     ;FLIP-FLOP BEING SET AND THE SIGNAL ACAS H BEING ASSERTED HIGH. THE
7926                                     ;FOLLOWING SECTION WILL READ AND CHECK THAT THE LOW BYTE OF THE OLD
7927                                     ;FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS. THE EODAL BUS
7928                                     ;WILL BE READ BACK VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED
7929                                     ;TO CONTROL REGISTER 6.
7930
7931                                     ;IF THE LOW BYTE DATA READ BACK FROM THE EODAL BUS EQUALS 063, THEN
7932                                     ;THE NEW FORCE JUMP ADDRESS REGISTER WAS PROBABLY ENABLED TO THE EODAL
7933                                     ;BUS INSTEAD OF THE OLD FORCE JUMP ADDRESS REGISTER. THE DATA PATTERN
7934                                     ;146063 WAS WRITTEN INTO THE NEW FORCE JUMP ADDRESS REGISTER AT THE
7935                                     ;BEGINNING OF THE TEST.
7936
7937 021206 011137 002342                MOV      (R1),R6LOAD                ;GET THE DATA LOADED INTO THE DIAG
7938                                     ;ADDRESS REGISTER
7939 021212 042737 177400 002342        BIC      #177400,R6LOAD            ;CLEAR UPPER BYTE
7940 021220 012737 177400 002346        MOV      #177400,R6MASK           ;SETUP TO IGNORE HIGH BYTE
7941 021226 004737 006700                JSR      PC,READR6                ;READ LB OF OLD FJA ON EODAL BUS
7942 021232 001405                        BEQ      14$                      ;IF OLD FLA OK THEN CONTINUE
7943 021234                                ERRDF   4,FEODAL,R06ERR           ;OLD FJA TO EODAL BUS ERROR
7944 021234 104455                        TRAP    C$ERRDF
7945 021236 000004                        .WORD   4
7946 021240 003147                        .WORD   FEODAL
7947 021242 005020                        .WORD   R06ERR
7948 021244                                CKLOOP
7949 021244 104406                        TRAP    C$CLP1
7950
7951                                     ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
7952                                     ;GDAL BITS 1 AND 0 TO ONES.
7953
7954 021246 004737 006754                14$: JSR      PC,SLHDAL                ;GO SELECT HDAL REG VIA GDAL BITS 2:0
7955
7956                                     ;SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
7957
7958 021252 012737 021004 002342        MOV      #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
7959 021260 005037 002346                CLR      R6MASK                  ;SETUP TO COMPARE ALL BITS
7960 021264 004737 007442                JSR      PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
7961
7962                                     ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H. THIS IS
7963                                     ;DONE TO SIMULATE A MACHINE CYCLE.
7964

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7965 021270 004737 007502      JSR      PC,XPI                ;GO PULSE XPI H VIA HDAL15 H
7966
7967                               ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
7968                               ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
7969                               ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
7970                               ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
7971                               ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
7972                               ;AND RASP L WILL BE PULSED.
7973                               ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
7974                               ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
7975
7976 021274 004737 007272      JSR      PC,XRAS               ;GO PULSE XRAS VIA HDAL12 H
7977
7978                               ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
7979                               ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
7980                               ; PAUSE STATE WORKING - PSMW H - 1
7981                               ; PAUSE STATE SYNC - EPSF H - 0
7982                               ; 8 BIT INSTRUCTION HB - EP8F H - 0
7983                               ; 8 BIT ADDRESS LB - EP8G H - 1
7984                               ; 8 BIT ADDRESS HB - EP8N H - 0
7985
7986 021300 004737 006654      JSR      PC,READR4             ;GO READ VDAL AND PAUSE STATE MACHINE
7987 021304 001405              BEQ      15$                   ;IF OK THEN CONTINUE
7988 021306                      ERRDF   3,VDALRG,R4EROR             ;PAUSE STATE MACHINE CHANGED BY XRAS H
7989 021306 104455              TRAP    C$ERDF
7990 021310 000003              .WORD   3
7991 021312 002537              .WORD   VDALRG
7992 021314 005004              .WORD   R4EROR
7993 021316                      CKLOOP
7994 021316 104406              TRAP    C$CLP1
7995
7996                               ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
7997                               ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
7998                               ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-
7999                               ;FLOP THUS CLEARING THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP. THE
8000                               ;PREVIOUS OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP (1) WILL BE
8001                               ;CLOCKED INTO THE 8 BIT ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT
8002                               ;ADDRESS HB FLIP-FLOP TO A ONE.
8003
8004 021320 004737 007410      15$: JSR      PC,XCASH             ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8005
8006                               ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8007                               ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH.
8008                               ; PAUSE STATE WORKING - PSMW H - 1
8009                               ; PAUSE STATE SYNC - EPSF H - 0
8010                               ; 8 BIT INSTRUCTION HB - EP8F H - 0
8011                               ; 8 BIT ADDRESS LB - EP8F H - 0
8012                               ; 8 BIT ADDRESS HB - EP8N H - 1
8013
8014 021324 042737 020000 002336 BIC      #VDAL13,R4GOOD        ;SETUP TO EXPECT EP8G H TO BE A 0
8015 021332 052737 040000 002336 BIS      #VDAL14,R4GOOD        ;SETUP TO EXPECT EP8N H TO BE A 1
8016 021340 004737 006654      JSR      PC,READR4             ;GO READ VDAL AND PAUSE STATE MACHINE
8017 021344 001405              BEQ      16$                   ;IF OK THEN CONTINUE
8018 021346                      ERRDF   3,VDALRG,R4EROR             ;EP8G H NOT 0 OR EP8N H NOT A 1
8019 021346 104455              TRAP    C$ERDF
8020 021350 000003              .WORD   3

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8021	021352	002537			.WORD	VDALRG	
8022	021354	005004			.WORD	R4EROR	
8023	021356				CKLOOP		
8024	021356	104406			TRAP	C\$CLP1	
8025							
8026							:SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE HIGH BYTE
8027							:OF THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
8028							:BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
8029							:BUS WILL BE READBACK TO THE LSI-11 VIA THE SIGNAL RPT7 L.
8030							
8031	021360	004737	007122	16\$:	JSR	PC,SEODAL	:SELECT EODAL BUS VIA GDAL BITS 2:0
8032							
8033							:ON THE FIRST PULSE OF XRAS H IN THIS TEST WHEN THE SIGNAL EDFET H
8034							:WAS SET HIGH, THE OLD FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN
8035							:LOADED WITH THE DATA PATTERN IN THE DIAGNOSTIC ADDRESS REGISTER VIA
8036							:THE CLOCKING SIGNAL DFET H. AT THIS POINT IN TIME, THE HIGH BYTE
8037							:OF THE OLD FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL
8038							:BUS VIA THE SIGNAL OEABH L. THIS SIGNAL IS ASSERTED LOW AS A RESULT
8039							:OF THE 'GET NEW ADDRESS' FLIP - FLOP BEING CLEARED AND THE
8040							:THE SIGNAL EABH H BEING ASSERTED HIGH. THE 'GET NEW ADDRESS'
8041							:FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THIS TEST BY THE SIGNAL
8042							:VDAL2 H BEING SET AND CLEARED. THE SIGNAL EABH H IS ASSERTED HIGH
8043							:AS A RESULT OF THE 8 BIT ADDRESS HB FLIP-FLOP BEING SET TO A ONE AND
8044							:THE SIGNAL ACAS H BEING ASSERTED HIGH. THE FOLLOWING SECTION WILL
8045							:READ AND CHECK THAT THE HIGH BYTE OF THE OLD FORCE JUMP ADDRESS REG-
8046							:ISTER IS ENABLED TO THE EODAL BUS. THE EODAL BUS WILL BE READ BY
8047							:THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
8048							:
8049							:IF THE DATA READ ON THE EODAL BUS EQUALS 314 THEN THE NEW FORCE JUMP
8050							:ADDRESS REGISTER WAS PROBABLY READ INSTEAD OF THE OLD FORCE JUMP
8051							:ADDRESS REGISTER. THE DATA PATTERN 146063 WAS WRITTEN INTO THE
8052							:NEW FORCE JUMP ADDRESS REGISTER AT THE BEGINNING OF THIS TEST.
8053							
8054	021364	011137	002342		MOV	(R1),R6LOAD	:GET DIAG ADDRESS REG DATA
8055	021370	000337	002342		SWAB	R6LOAD	:SWAP HIGH BYTE WITH LOW BYTE
8056	021374	042737	177400	002342	BIC	#177400,R6LOAD	:CLEAR LOW BYTE IN HIGH BYTE POSITION
8057	021402	012737	177400	002346	MOV	#177400,R6MASK	:SETUP TO IGNORE HIGH BYTE ON READ
8058	021410	004737	006700		JSR	PC,READR6	:READ OLD FJA HB ON EODAL BUS
8059	021414	001405			BEQ	17\$:OF OLD FLA OK THEN CONTINUE
8060	021416				ERRDF	4,FEODAL,R06ERR	:OLD FLA HB TO EODAL BUS ERROR
8061	021416	104455			TRAP	C\$ERDF	
8062	021420	000004			.WORD	4	
8063	021422	003147			.WORD	FEODAL	
8064	021424	005020			.WORD	R06ERR	
8065	021426				CKLOOP		
8066	021426	104406			TRAP	C\$CLP1	
8067							
8068							:RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8069							:GDAL BITS 1 AND 0 TO ONES
8070							
8071	021430	004737	006754	17\$:	JSR	PC,SLHDAL	:GO SELECT HDAL REG VIA GDAL BITS 2:0
8072							
8073							:SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8074							
8075	021434	012737	021004	002342	MOV	#HDAL13!HDAL9!HDAL2,R6LOAD	:SETUP BITS PREVIOUSLY LOADED
8076	021442	005037	002346		CLR	R6MASK	:SETUP TO CHECK ALL BITS

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8077 021446 004737 007442 JSR PC,XCASL ;SET XCAS L TO LOW STATE VIA HDAL13 H
8078
8079 ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H. THIS IS DONE
8080 ;TO SIMULATE A MACHINE CYCLE.
8081
8082 021452 004737 007502 JSR PC,XPI ;GO PULSE XPI H VIA HDAL15 H
8083
8084 ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8085 ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8086 ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
8087 ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8088 ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8089 ;AND RASP L WILL BE PULSED.
8090 ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L
8091 ;WHEN THE SIGNALS EPFN L AND PSMW H ARE ASSERTED HIGH AND EP8N L IS
8092 ;ASSERTED LOW. A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H WILL BE
8093 ;ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING
8094 ;CLEARED.
8095
8096 021456 004737 007272 JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
8097
8098 ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8099 ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8100 : PAUSE STATE WORKING - PSMW H - 0
8101 : PAUSE STATE SYNC - EPSF H - 0
8102 : 8 BIT INSTRUCTION HB - EP8F H - 0
8103 : 8 BIT ADDRESS LB - EP8G H - 0
8104 : 8 BIT ADDRESS HB - EP8N H - 1
8105
8106 021462 042737 001000 002336 BIC #VDAL9,R4GOOD ;SETUP TO EXPECT PSMW H TO BE A 0
8107 021470 004737 006654 JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
8108 021474 001405 BEQ 18$ ;IF OK THEN CONTINUE
8109 021476 ERRDF 3,VDALRG,R4EROR ;PSMW H F/F PROBABLY NOT 0
8110 021476 104455 TRAP C$ERRDF
8111 021500 000003 .WORD 3
8112 021502 002537 .WORD VDALRG
8113 021504 005004 .WORD R4EROR
8114 021506 CKLOOP
8115 021506 104406 TRAP C$CLP1
8116
8117 ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. THE SIGNAL
8118 ;XCAS H WILL CLOCK THE OUTPUT OF 8 BIT ADDRESS LB FLIP-FLOP (0) INTO THE
8119 ;8 ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS HB FLIP-FLOP TO
8120 ;A ZERO.
8121
8122 021510 004737 007376 18$: JSR PC,XCAS ;GO PULSE XCAS H VIA HDAL13 H
8123
8124 ;READ THE VDAL REGISTER AND THE PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
8125 ;THE FOLLOWING STATES AS A RESULT OF XCAS H BEING PULSED.
8126 : PAUSE STATE WORKING - PSMW H - 0
8127 : PAUSE STATE SYNC - EPSF H - 0
8128 : 8 BIT INSTRUCTION HB - EP8F H - 0
8129 : 8 BIT ADDRESS LB - EP8G H - 0
8130 : 8 BIT ADDRESS HB - EP8N H - 0
8131
8132 021514 042737 040000 002336 BIC #VDAL14,R4GOOD ;SETUP TO EXPECT EP8N H TO BE A 0

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TEST 33: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - OLD FJA

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8133 021522 004737 006654      JSR    PC,READR4      ;GO READ VDAL AND PAUSE STATE MACHINE
8134 021526 001405              BEQ    19$            ;IF OK THEN CONTINUE
8135 021530                    ERRDF  3,VDALRG,R4EROR ;EP8N H PROBABLY NOT CLEARED
8136 021530 104455              TRAP  C$ERDF
8137 021532 000003              .WORD 3
8138 021534 002537              .WORD VDALRG
8139 021536 005004              .WORD R4EROR
8140 021540                    CKLOOP
8141 021540 104406              TRAP  C$CLP1
8142
8143
8144                    ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
8145                    ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
8146 021542 004737 007502      19$:  JSR    PC,XPI      ;GO PULSE XPI VIA HDAL15 H
8147
8148 021546                    ENDSEG
8149 021546                    10000$:
8150 021546 104405              TRAP  C$ESEG
8151 021550 005721              TST   (R1)+          ;UPDATE TABLE POINTER
8152 021552 005302              DEC   R2              ;CHECK IF ALL PATTERNS DONE
8153 021554 001412              BEQ   21$            ;IF YES THEN EXIT
8154 021556 000137 020332      JMP   1$              ;DO NEXT PATTERN
8155
8156 021562 125125              20$:  .WORD 125125
8157 021564 052652              .WORD 052652
8158 021566 000377              .WORD 000377
8159 021570 177400              .WORD 177400
8160 021572 125252              .WORD 125252
8161 021574 052525              .WORD 052525
8162 021576 177777              .WORD 177777
8163 021600 000000              .WORD 000000
8164
8165 021602                    21$:  ENDTST
8166 021602                    L10063:
8167 021602 104401              TRAP  C$ETST
8168

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TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

.SBTTL TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

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: THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE
: PAUSE STATE MACHINE FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE
: STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL
: BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND
: CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND
: AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL
: PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE
: TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADALO H WILL BE SET AND CLEARED TO
: CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC
: CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE
: IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.
  
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: THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW
: FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS
: MODE. THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA
: PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000.
: THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED WITH THE DATA AT THE BEGINNING
: OF THE TEST.
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021604 004737 005510
021610 012701 023134
021614 012702 000010
021620
021620 104404
021622 004737 007006
021626 012737 004000 002342
021634 005037 002346
021640 004737 006672
021644 001405
021646
021646 104455
021650 000004
021652 002631
021654 005020
021656
021656 104406
021660 004737 006754
  
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BGNTST
T34::
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #22$,R1 ;GET ADDRESS OF OLD FJA DATA TABLE
MOV #8.,R2 ;NUMBER OF DATA PATTERNS TO BE TESTED

1$: BGNSEG
TRAP C$BSEG
;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO
;TO A ZERO.

JSR PC,SLMODR ;GO SELECT MODE REG VIA CONTROL REG 0
;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000. MR BIT 11
;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

MOV #MR11,R6LOAD ;SETUP TO SET MR BIT 11
CLR R6MASK ;SETUP TO CHECK ALL 16 BITS
JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C$CLP1

;SET GDAL1 AND GDALO TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

2$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2 0
  
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8225
8226      :LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
8227      :HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
8228      :REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
8229      :BUS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
8230      :TIMING AND CONTROL SIGNALS.
8231
8232 021664 012737 001004 002342      MOV      #HDAL9!HDAL2,R6LOAD      ;SETUP BITS TO BE LOADED
8233 021672 004737 006672      JSR      PC,LDRDR6                ;GO LOAD, READ AND CHECK HDAL REGISTER
8234 021676 001405      BEQ      3$                       ;IF LOADED OK THEN CONTINUE
8235 021700      ERRDF  4,HDALRG,R06ERR        ;HDAL REG NOT EQUAL TO EXPECTED
8236 021700 104455      TRAP    C$ERDF
8237 021702 000004      .WORD   4
8238 021704 002605      .WORD   HDALRG
8239 021706 005020      .WORD   R06ERR
8240 021710      CKLOOP
8241 021710 104406      TRAP    C$CLP1
8242
8243      :SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
8244      :ZEROS. ON A WRITE OR REPT? COMMAND TO CONTROL REGISTER 6, THE DIAG-
8245      :NOSTIC ADDRESS REGISTER WILL BE SELECTED.
8246
8247 021712 004737 007072      3$:    JSR      FC,SLDADR                ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0
8248
8249      :LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA
8250      :PATTERN OF 146063. THE DIAGNOSTIC ADDRESS REGISTER IS WRITTEN WITH
8251      :DATA TO CHECK THAT THE CORRECT FORCE JUMP ADDRESS REGISTER IS ENABLED
8252      :TO THE EODAL BUS WHEN THE 8 BIT ADDRESS FLIP-FLOPS ARE SET. THE NEW
8253      :FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE BUS DURING THIS
8254      :TEST.
8255
8256 021716 012737 146063 002342      MOV      #146063,R6LOAD          ;SETUP DATA PATTERN
8257 021724 004737 006672      JSR      PC,LDRDR6                ;GO LOAD, READ AND CHECK DIAG ADDR REG
8258 021730 001405      BEQ      4$                       ;IF LOADED OK THEN CONTINUE
8259 021732      ERRDF  4,ADDRRG,R06ERR          ;DIAG ADDRESS REG NOT EQUAL EXPECTED
8260 021732 104455      TRAP    C$ERDF
8261 021734 000004      .WORD   4
8262 021736 002735      .WORD   ADDR RG
8263 021740 005020      .WORD   R06ERR
8264 021742      CKLOOP
8265 021742 104406      TRAP    C$CLP1
8266
8267      :LOAD, READ AND CHECK ADAL REGISTER. ADALO WILL BE SET AND CLEARED
8268      :TO CLEAR THE BREAK LOGIC. ADAL4 ON A ZERO WILL PUT THE PAUSE STATE
8269      :MACHINE IN THE PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
8270      :BREAK SIGNAL FROM CAUSING A BREAK CONDITION. ADAL4 H ON A ZERO WILL
8271      :CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
8272      :SIGNAL XRAS H IS PULSED.
8273
8274 021744 005037 002330      4$:    CLR      R2LOAD                ;SETUP TO CLEAR ALL ADAL REGISTER BITS
8275 021750 004737 007772      JSR      PC,BRKRES                ;PULSE BRKRES L VIA ADALO H
8276
8277      :SET VDAL2 H TO A ONE AND THEN ZERO. VDAL2 H ON A ONE WILL CLEAR THE
8278      :PAUSE STATE MACHINE FLIP-FLOPS AND THE FLIP-FLOPS, TAKE NEW FORCE JUMP
8279      :ADDRESS AND GET NEW ADDRESS.
8280

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TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

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8281 021754 005037 002334 CLR R4LOAD ;SETUP TO CLEAR ALL VDAL REGISTER BITS
8282 021760 004737 007712 JSR PC,CLRPSM ;SET AND CLEAR VDAL2 H TO 0 PAUSE STATE
8283
8284 ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A ONE
8285 ;AND GDAL BITS 2 AND 0 TO ZEROES. ON A WRITE COMMAND TO CONTROL REG 6,
8286 ;DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS REGISTER AND THE
8287 ;TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
8288
8289 021764 004737 007040 JSR PC,SLFJAR ;SELECT NEW FJA VIA GDAL BITS 2:0
8290
8291 ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA INTO THE
8292 ;NEW FORCE JUMP ADDRESS REGISTER. THE DATA WILL BE LOADED INTO THE
8293 ;FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB H AND WPT1 HB H.
8294 ;THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO BE SET TO A ONE
8295 ;BY THE SIGNAL WPT1 LB H. THE DATA PATTERNS LOADED WILL BE ONE OF THE
8296 ;FOLLOWING: 125125, 052652, 000377, 177400, 125252, 052525, 177777 AND
8297 ;000000.
8298
8299 021770 011177 160312 MOV (R1),@REG6 ;WRITE DATA FROM THE TABLE INTO NEW FJA
8300
8301 ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
8302 ;CHECK THAT THE SIGNAL WPT1 LB H CLOCKED THE TAKE NEW FORCE JUMP ADDRESS
8303 ;FLIP-FLOP TO A ONE.
8304
8305 021774 012737 000200 002334 MOV #VDAL7,R4LOAD ;SETUP BIT TO BE LOADED
8306 022002 013737 002334 002336 MOV R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
8307 022010 052737 100000 002336 BIS #VDAL15,R4GOOD ;SETUP TO EXPECT TNFJ H TO BE A 1
8308 022016 004737 006646 JSR PC,LDRD4R ;GO LOAD READ AND CHECK VDAL REG
8309 022022 001405 BEQ $$ ;IF LOADED OK THEN CONTINUE
8310 022024 ERRDF 3,VDALRG,R4EROR ;TNFJ H PROBABLY NOT SET IN VDAL REG
8311 022024 104455 TRAP C$ERDF
8312 022026 000003 .WORD 3
8313 022030 002537 .WORD VDALRG
8314 022032 005004 .WORD R4EROR
8315 022034 CKLOOP
8316 022034 104406 TRAP C$CLP1
8317
8318 ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
8319 ;TO ONES. BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
8320 ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L.
8321
8322 022036 004737 006754 5$: JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL 2:0
8323
8324 ;SFT HDAL12 H TO A ONE TO SET THE SIGNALS XRAS H AND XRAS L TO THE
8325 ;HIGH AND LOW STATE RESPECTIVELY. THEY WILL REMAIN SET TO THESE STATES
8326 ;UNTIL THE PROGRAM PULSES THE SIGNALS XPI H AND XPI L.
8327
8328 ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
8329 ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
8330 ;HIGH STATE. THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
8331 ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
8332 ;TO THE HIGH STATE. THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
8333 ;SIGNAL PAUSE L IS ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED
8334 ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
8335 ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
8336 ;PSMW H WILL BE ASSERTED HIGH. THE SIGNAL PSMW H IS DEAD IN THE VDAL

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8337 :REGISTER AS VDAL9 H. WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
8338 :SIGNAL PB H WILL BE ASSERTED HIGH. THE SIGNAL PB H IS THE DATA INPUT
8339 :LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
8340 :
8341 :THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED. WHEN THE
8342 :SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
8343 :PULSE WILL BE ISSUED ON THE SIGNAL DFET H. THE SIGNAL DFET H WILL
8344 :CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER. AT THE
8345 :PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
8346 :ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
8347 :LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.
8348 :
8349 022042 012737 001004 002342 MOV #HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8350 022050 004737 007304 JSR PC,XRASH ;SET XRAS H HIGH + XRAS L VIA HDAL12 H
8351 :
8352 :CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
8353 :THE LOW STATE. CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
8354 :STATE AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
8355 : PAUSE STATE WORKING - PSMW H - 1
8356 : PAUSE STATE SYNC - EPSF H - 0
8357 : 8 BIT INSTRUCTION HB - EP8F H - 0
8358 : 8 BIT ADDRESS LB H - EP8G H - 0
8359 : 8 BIT ADDRESS HB H - EP8N H - 0
8360 : TAKE NEW FJ ADDRESS - TNFJ H - 1
8361 : GET NEW ADDRESS - OUTNEW H - 0
8362 :
8363 022054 042737 000200 002334 BIC #VDAL7,R4LOAD ;SETUP TO CLEAR FETCT H
8364 022062 013737 002334 002336 MOV R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
8365 022070 052737 101000 002336 BIS #VDAL15!VDAL9,R4GOOD ;EXPECT PSMW H AND TNFJ H F/F'S
8366 022076 004737 006646 JSR PC,LDRD4R ;GO LOAD, READ AND CHECK VDAL REG
8367 022102 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
8368 022104 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
8369 022104 104455 TRAP C$ERDF
8370 022106 000003 .WORD 3
8371 022110 002537 .WORD VDALRG
8372 022112 005004 .WORD R4EROR
8373 022114 CKLOOP
8374 022114 104406 TRAP C$CLP1
8375 :
8376 :THE SIGNALS XRAS H AND XRAS L ARE STILL ASSERTED TO THE HIGH AND LOW
8377 :STATE RESPECTIVELY BY HDAL12 H BEING SET TO A ONE. THEY WILL REMAIN
8378 :SET TO THESE STATES UNTIL THE SIGNALS XPI H AND XPI L ARE PULSED.
8379 :
8380 :SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
8381 :SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
8382 :SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP,
8383 :THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE. THE SIGNAL
8384 :XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-
8385 :FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS CLOCKING THAT
8386 :FLIP-FLOP TO A ZERO.
8387 :
8388 022116 004737 007410 6$: JSR PC,XCASH ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8389 :
8390 :READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
8391 :IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING PULSED.
8392 : PAUSE STATE WORKING - PSMW H - 1

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TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

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8393      : PAUSE STATE SYNC - EPSF H - 1
8394      : 8 BIT INSTRUCTION HB - EP8F H - 0
8395      : 8 BIT ADDRESS LB - EP8G H - 0
8396      : 8 BIT ADDRESS HB - EP8N H - 0
8397      : TAKE NEW FJ ADDRESS - TNFJ H - 1
8398      : GET NEW ADDRESS - OUTNEW H - 0
8399
8400 022122 052737 002000 002336  BIS #VDAL10,R4GOOD ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
8401 022130 004737 006654  JSR PC,READR4 ;CO READ AND CHECK PAUSE STATE MACHINE
8402 022134 001405  BEQ 7$ ;IF LOADED OK THEN CONTINUE
8403 022136  ERRDF 3,VDALRG,R4EROR ;EPSF H PROBABLE NOT SET IN VDAL REG
8404 022136 104455  TRAP C$ERDF
8405 022140 000003  .WORD 3
8406 022142 002537  .WORD VDALRG
8407 022144 005004  .WORD R4EROR
8408 022146  CKLOOP
8409 022146 104406  TRAP C$CLP1
8410
8411      :SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE LOW
8412      :BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
8413      :EODAL BUS AT THE SAME TIME. ON A READ COMMAND TO CONTROL REGISTER 6,
8414      :THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
8415
8416 022150 004737 007122 7$: JSR PC,SEODAL ;SELECT EODAL BUS VIA GDAL BITS 2:0
8417
8418      :WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
8419      :FLIP-FLOP IS SET TO A ONE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
8420      :WHEN THE SIGNAL ACAS H IS ASSERTED HIGH, THE PAUSE STATE SYNC FLIP-
8421      :FLOP IS SET TO A ONE, AND MODE REGISTER BIT 11 IS A ONE (8 BIT MODE),
8422      :THE SIGNAL EDRL H WILL BE ASSERTED LOW, THUS ENABLING THE LOW BYTE OF
8423      :THE 16 BIT INSTRUCTION REGISTER ONTO THE EODAL BUS. THE HIGH BYTE OF
8424      :THE 16 BIT INSTRUCTION REGISTER WILL BE DISABLED ON THE EODAL BUS.
8425      :WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH GDAL BITS 2:0
8426      :SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL RPT7 L. THE SIGNAL
8427      :RPT7 L WILL READBACK THE EODAL BUS ONTO THE LSI-11 BUS.
8428
8429 022154 012737 000137 002342  MOV #137,R6LOAD ;SETUP EXPECTED LOW BYTE DATA
8430 022162 012737 177400 002346  MOV #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE
8431 022170 004737 006700  JSR PC,READR6 ;GO READ LOW BYTE OF INSTR REG ON EODAL
8432 022174 001405  BEQ 8$ ;IF INSTR = "JMP" THEN CONTINUE
8433 022176  ERRDF 4,IEODAL,R06ERR ;EODAL BUS ERROR OR 8 BIT LB INSTR ERROR
8434 022176 104455  TRAP C$ERDF
8435 022200 000004  .WORD 4
8436 022202 003034  .WORD IEODAL
8437 022204 005020  .WORD R06ERR
8438 022206  CKLOOP
8439 022206 104406  TRAP C$CLP1
8440
8441      :RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL B'TS
8442      :1 AND 0 TO A ONE.
8443
8444 022210 004737 006754 8$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0
8445
8446      :SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER.
8447      :
8448      :THE SIGNALS XRAS H AND XRAS L WILL REMAIN ASSERTED TO THE HIGH AND LOW
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8505
8506 022262 052737 000400 002336      BIS      #VDAL8,R4GOOD      :EXPECT OUTNEW H TO BE SET TO A ONE
8507 022270 004737 006654              JSR      PC,READR4        :READ VDAL AND PAUSE STATE MACHINE
8508 022274 001405                      BEQ      10$              :IF OK THEN CONTINUE
8509 022276                      ERRDF    3,VDALRG,R4EROR   :VDAL REG NOT EQUAL EXPECTED
8510 022276 104455                      TRAP    C$ERDF
8511 022300 000003                      .WORD   3
8512 022302 002537                      .WORD   VDALRG
8513 022304 005004                      .WORD   R4EROR
8514 022306                      CKLOOP
8515 022306 104406                      TRAP    C$CLP1
8516
8517
8518      :TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8519      :WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8520      :EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8521      :EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8522      :PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8523      :AND RASP L WILL BE PULSED.
8524      :THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8525      :SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8526 022310 004737 007272      10$:    JSR      PC,XRAS      :GO PULSE XRAS H BY HDAL12
8527
8528      :READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
8529      :TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8530      :
8531      : PAUSE STATE WORKING - PSMW H - 1
8532      : PAUSE STATE SYNC - EPSF H - 1
8533      : 8 BIT INSTRUCTION HB - EP8F H - 0
8534      : 8 BIT ADDRESS LB - EP8G H - 0
8535      : 8 BIT ADDRESS HB - EP8N H - 0
8536      : TAKE NEW FJ ADDRESS - TNFJ H - 1
8537      : GET NEW ADDRESS - OUTNEW H - 1
8538 022314 004737 006654      JSR      PC,READR4        :CHECK VDAL AND PAUSE STATE MACHINE
8539 022320 001405                      BEQ      11$              :IF OK THEN CONTINUE
8540 022322                      ERRDF    3,VDALRG,R4EROR   :VDAL OR PAUSE STATE MACHINE ERROR
8541 022322 104455                      TRAP    C$ERDF
8542 022324 000003                      .WORD   3
8543 022326 002537                      .WORD   VDALRG
8544 022330 005004                      .WORD   R4EROR
8545 022332                      CKLOOP
8546 022332 104406                      TRAP    C$CLP1
8547
8548      :SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
8549      :SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE LEVEL OF THE
8550      :SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
8551      :CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO. THE SIGNAL XCAS H
8552      :WILL CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
8553      :INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THAT FLIP-FLOP
8554      :TO A ONE. THE SIGNAL XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE
8555      :8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-FLOP,
8556      :THUS CLOCKING THAT FLIP-FLOP TO A ZERO.
8557      :THE SIGNAL XCAS H WILL ALSO CAUSE THE "TAKE NEW FORCE JUMP ADDRESS"
8558      :FLIP-FLOP TO BE CLEARED WHEN THE "GET NEW ADDRESS" FLIP-FLOP IS SET
8559      :TO A ONE.
8560

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8561 022334 004737 007410      11$: JSR    PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8562
8563                               ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-
8564                               ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH
8565                               ; PAUSE STATE WORKING - PSMW H - 1
8566                               ; PAUSE STATE SYNC - EPSF H - 0
8567                               ; 8 BIT INSTRUCTION HB - EP8F H - 1
8568                               ; 8 BIT ADDRESS LB - EP8G H - 0
8569                               ; 8 BIT ADDRESS HB - EPFN H - 0
8570                               ; TAKE NEW FJ ADDRESS - TNFJ H - 0
8571                               ; GET NEW ADDRESS - OUTNEW H - 1
8572
8573 022340 042737 102000 002336  BIC    #VDAL15,VDAL10,R4GOOD    ;CLEAR BIT FOR EPSF H AND TNFJ H
8574 022346 052737 010000 002336  BIS    #VDAL12,R4GOOD          ;SET BIT FOR EP8F H
8575 022354 004737 006654          JSR    PC,READR4              ;GO READ VDAL AND PAUSE STATE MACHINE
8576 022360 001405          BEQ    12$                    ;IF OK THEN CONTINUE
8577 022362          ERRDF  3,VDALRG,R4EROR    ;EP8F H PROBABLY NOT SET IN VDAL REG
8578 022362 104455          TRAP  C$ERDF
8579 022364 000003          .WORD  3
8580 022366 002537          .WORD  VDALRG
8581 022370 005004          .WORD  R4EROR
8582 022372          CKLCOP
8583 022372 104406          TRAP  C$CLP1
8584
8585                               ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE HIGH
8586                               ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
8587                               ;EODAL BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6,
8588                               ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
8589
8590 022374 004737 007122      12$: JSR    PC,SEODAL              ;SELECT EODAL BUS VIA GDAL BITS 2:0
8591
8592                               ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
8593                               ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
8594                               ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE 8 BIT INSTRUCTION HB
8595                               ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ED8H H WILL BE ASSERTED HIGH,
8596                               ;THUS ENABLING THE HIGH BYTE OF THE 16 BIT INSTRUCTION REGISTER (000)
8597                               ;ONTO THE LOW BYTE OF THE EODAL BUS. WHEN A READ COMMAND IS ISSUED TO
8598                               ;CONTROL REGISTER 6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE
8599                               ;ISSUED ON THE SIGNAL RPT7 L. THE SIGNAL RPT7 L WILL READBACK THE
8600                               ;EODAL BUS ONTO THE LSI-11 BUS.
8601
8602 022400 005037 002342          CLR    R6LOAD                ;EXPECT HIGH BYTE TO BE ZERO
8603 022404 012737 177400 002346  MOV    #177400,R6MASK        ;SETUP TO IGNORE HIGH BYTE ON READ
8604 022412 004737 006700          JSR    PC,READR6            ;GO READ 8 BIT HIGH BYTE INSTRUCTION
8605                               ;ON THE EODAL BUS AS LOW BYTE
8606 022416 001405          BEQ    13$                    ;IF INSTRUCTION EQUALS 0 THEN CONT
8607 022420          ERRDF  4,IEODAL,R06ERR    ;EODAL BUS OR 8 BIT HB INSTR ERROR
8608 022420 104455          TRAP  C$ERDF
8609 022422 000004          .WORD  4
8610 022424 003034          .WORD  IEODAL
8611 022426 005020          .WORD  R06ERR
8612 022430          CKLOOP
8613 022430 104406          TRAP  C$CLP1
8614
8615                               ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
8616                               ;1 AND 0 TO ONES.

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8617
8618 022432 004737 006754      138:  JSR      PC,SLHDAL          ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8619
8620                               ;SET THE SIGNAL XCAS H TO LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER
8621
8622 022436 012737 021004 002342  MOV      #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8623 022444 005037 002346          CLR      R6MASK              ;SETUP TO CHECK ALL BITS
8624 022450 004737 007442          JSR      PC,XCASL            ;SET XCAS H TO LOW STATE VIA HDAL13 H
8625
8626                               ;TOGGLE THE SIGNAL XPI H BY PULSING THE SIGNAL HDAL15 H. THIS IS DONE
8627                               ;TO SIMULATE A MACHINE CYCLE.
8628
8629 022454 004737 007502          JSR      PC,XPI              ;GO PULSE XPI H VIA HDAL15 H
8630
8631                               ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8632                               ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8633                               ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8634                               ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8635                               ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8636                               ;AND RASP L WILL BE PULSED.
8637                               ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8638                               ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8639
8640 022460 004737 007272          JSR      PC,XRAS            ;PULSE XRAS VIA THE SIGNAL HDAL12
8641
8642                               ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
8643                               ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8644                               ;NO CHANGES SHOULD OCCUR IN THE PAUSE STATE MACHINE WHEN XRAS H PULSED.
8645                               ; PAUSE STATE WORKING - PSMW H - 1
8646                               ; PAUSE STATE SYNC - EPSF H - 0
8647                               ; 8 BIT INSTRUCTION HB - EP8F H - 1
8648                               ; 8 BIT ADDRESS LB - EP8G H - 0
8649                               ; 8 BIT ADDRESS HB - EP8N H - 0
8650                               ; TAKE NEW FJ ADDRESS - TNFJ H - 0
8651                               ; GET NEW ADDRESS - OUTNEW H - 1
8652
8653 022464 004737 006654          JSR      PC,READR4          ;GO READ VDAL AND PAUSE STATE MACHINE
8654 022470 001405                BEQ      14$                ;IF OK THEN CONTINUE
8655 022472                        ERRDF   3,VDALRG,R4EROR          ;PAUSE STATE REGISTERS CHANGED
8656 022472 104455                TRAP    C$ERRDF
8657 022474 000003                .WORD   3
8658 022476 002537                .WORD   VDALRG
8659 022500 005004                .WORD   R4EROR
8660 022502
8661 022502 104406                CKLOOP
8662                                TRAP    C$CLP1
8663
8664                               ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
8665                               ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
8666                               ;PAUSE STATE SYNC FLIP-FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-
8667                               ;FLOP, THUS CLEARING THE 8 BIT INSTRUCTION HB FLIP-FLOP. THE PREVIOUS
8668                               ;OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-FLOP (1) WILL BE CLOCKED INTO
8669                               ;THE 8 BIT ADDRESS LB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS LB F/F.
8670 022504 004737 007410      14$:  JSR      PC,XCASH          ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8671
8672                               ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN

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8673                                     ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
8674                                     ; PAUSE STATE WORKING - PSMW H - 1
8675                                     ; PAUSE STATE SYNC - EPSF H - 0
8676                                     ; 8 BIT INSTRUCTION HB - EP8F H - 0
8677                                     ; 8 BIT ADDRESS LB - EP8G H - 1
8678                                     ; 8 BIT ADDRESS HB - EP8N H - 0
8679                                     ; TAKE NEW FJ ADDRESS - TNFJ H - 0
8680                                     ; GET NEW ADDRESS - OUTNEW H - 1
8681
8682 022510 042737 010000 002336      BIC      #VDAL12,R4GOOD      ;SETUP TO EXPECT EP8F H TO BE 0
8683 022516 052737 020000 002336      BIS      #VDAL13,R4GOOD      ;SETUP TO EXPECT EP8G H TO BE 1
8684 022524 004737 006654              JSR      PC,READR4          ;GO READ VDAL AND PAUSE STATE MACHINE
8685 022530 001405                      BEQ      15$                ;IF OK THEN CONTINUE
8686 022532                               ERRDF    3,VDALRG,R4EROR      ;EP8F H PROBABLY NOT 0 OR EP8G H NOT SET
8687 022532 104455                      TRAP    C$ERDF
8688 022534 000003                      .WORD   3
8689 022536 002537                      .WORD   VDALRG
8690 022540 005004                      .WORD   R4EROR
8691 022542                               CKLOOP
8692 022542 104406                      TRAP    C$CLP1
8693
8694                                     ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE LOW BYTE
8695                                     ;OF THE NEW FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
8696                                     ;BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
8697                                     ;BUS WILL BE READBACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
8698
8699 022544 004737 007122      15$:   JSR      PC,SEODAL          ;SELECT EODAL BUS VIA GDAL BITS 2:0
8700
8701                                     ;AT THIS POINT IN TIME, THE LOW BYTE OF THE NEW FORCE JUMP ADDRESS REG-
8702                                     ;ISTER WILL BE ENABLED TO THE EODAL BUS VIA THE SIGNAL NEARL L. THIS
8703                                     ;SIGNAL IS ASSERTED LOW AS A RESULT OF "GET NEW ADDRESS"
8704                                     ;FLIP-FLOP BEING SET AND THE SIGNAL EARL H BEING ASSERTED HIGH. THE
8705                                     ;"GET NEW ADDRESS" FLIP - FLOP WAS SET WHEN THE PAUSE STATE SYNC FLIP-
8706                                     ;FLOP WAS A ONE, A PULSE ISSUED ON XRAS L, AND THE TAKE NEW FORCE
8707                                     ;JUMP ADDRESS FLIP-FLOP WAS SET TO A ONE. THE SIGNAL EARL H IS ASSERTED
8708                                     ;HIGH AS A RESULT OF THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP BEING SET TO A
8709                                     ;ONE AND THE SIGNAL ACAS H BEING ASSERTED HIGH. THE FOLLOWING SECTION
8710                                     ;WILL READ AND CHECK THAT THE LOW BYTE OF THE NEW FORCE JUMP ADDRESS
8711                                     ;REGISTER IS ENABLED TO THE EODAL BUS. THE EODAL BUS WILL BE READBACK
8712                                     ;VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
8713
8714                                     ;
8715                                     ;IF THE LOW BYTE DATA READ FROM THE EODAL BUS EQUALS 063, THEN THE OLD
8716                                     ;FORCE JUMP ADDRESS WAS PROBABLY ENABLED TO THE EODAL BUS INSTEAD OF THE
8717                                     ;NEW FORCE JUMP ADDRESS REGISTER. THE OLD FORCE JUMP ADDRESS REGISTER
8718                                     ;WAS LOADED WITH DATA FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL
8719                                     ;DFET H. THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH A DATA PATTERN
8720                                     ;OF 146063 AT THE BEGINNING OF THE TEST.
8721 022550 011137 002342      MOV      (R1),R6LOAD        ;GET THE DATA LOADED INTO THE DIAG
8722                                     ;ADDRESS REGISTER
8723 022554 042737 177400 002342      BIC      #177400,R6LOAD      ;CLEAR UPPER BYTE
8724 022562 012737 177400 002346      MOV      #177400,R6MASK      ;SETUP TO IGNORE HIGH BYTE
8725 022570 004737 006700              JSR      PC,READR6          ;READ LB OF OLD FJA ON EODAL BUS
8726 022574 001405                      BEQ      16$                ;IF OLD FLA OK THEN CONTINUE
8727 022576                               ERRDF    4,FEODAL,R06ERR      ;OLD FJA TO EODAL BUS ERROR
8728 022576 104455                      TRAP    C$ERDF

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8729 022600 000004          .WORD 4
8730 022602 003147          .WORD FEODAL
8731 022604 005020          .WORD R06ERR
8732 022606                CKLOOP
8733 022606 104406          TRAP C$CLP1
8734
8735                          ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8736                          ;GDAL BITS 1 AND 0 TO ONES.
8737
8738 J22610 004737 006754    16$: JSR    PC,SLHDAL          ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8739
8740                          ;SET THE SIGNAL XCAS H TO LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8741
8742 022614 012737 021004 002342 MOV    #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8743 022622 005037 002346 CLR    R6MASK                ;SETUP TO CHECK ALL BITS
8744 022626 004737 007442 JSR    PC,XCASL              ;SET XCAS H TO LOW STATE VIA HDAL13 H
8745
8746                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H. THIS IS
8747                          ;DONE TO SIMULATE A MACHINE CYCLE.
8748
8749 022632 004737 007502    JSR    PC,XPI                ;GO PULSE XPI H VIA HDAL15 H
8750
8751                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8752                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8753                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8754                          ;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8755                          ;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8756                          ;AND RASP L WILL BE PULSED.
8757                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8758                          ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8759
8760 022636 004737 007272    JSR    PC,XRAS                ;GO PULSE XRAS VIA HDAL12 H
8761
8762                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8763                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8764                          ;
8765                          ; PAUSE STATE WORKING - PSMW H - 1
8766                          ;
8767                          ; PAUSE STATE SYNC - EPSF H - 0
8768                          ;
8769                          ; 8 BIT INSTRUCTION HB - EP8F H - 0
8770                          ;
8771                          ; 8 BIT ADDRESS LB - EP8G H - 1
8772                          ;
8773                          ; 8 BIT ADDRESS HB - EP8N H - 0
8774                          ;
8775                          ; TAKE NEW FJ ADDRESS - TNFJ H - 0
8776                          ;
8777                          ; GET NEW ADDRESS - OUTNEW H - 1
8778
8779
8780 022642 004737 006654    JSR    PC,READR4              ;GO READ VDAL AND PAUSE STATE MACHINE
8781 022646 001405 BEQ    17$                    ;IF OK THEN CONTINUE
8782 022650 ERRDF 3,VDALRG,R4EROR ;PAUSE STATE MACHINE CHANGED BY XRAS H
8783 022652 104455 TRAP  C$ERRDF
8784 022654 000003          .WORD 3
8785 022656 002537          .WORD VDALRG
8786 022660 005004          .WORD R4EROR
8787 022660                CKLOOP
8788 022660 104406          TRAP  C$CLP1
8789
8790                          ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
8791                          ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
8792                          ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-

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TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

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8785                                     :FLOP THUS CLEARING THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP. THE
8786                                     :PREVIOUS OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP (1) WILL BE
8787                                     :CLOCKED INTO THE 8 BIT ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT
8788                                     :ADDRESS HB FLIP-FLOP TO A ONE.
8789
8790 022662 004737 007410                17$: JSR      PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 h
8791
8792                                     :READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8793                                     :BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
8794                                     :   PAUSE STATE WORKING - PSMW H - 1
8795                                     :   PAUSE STATE SYNC - EPSF H - 0
8796                                     :   8 BIT INSTRUCTION HB - EPBF H - 0
8797                                     :   8 BIT ADDRESS LB - EPBF H - 0
8798                                     :   8 BIT ADDRESS HB - EP8N H - 1
8799                                     :   TAKE NEW FJ ADDRESS - TNFJ H - 0
8800                                     :   GET NEW ADDRESS - OUTNEW H - 1
8801
8802 022666 042737 020000 002336          BIC      #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE A 0
8803 022674 052737 040000 002336          BIS      #VDAL14,R4GOOD          ;SETUP TO EXPECT EP8N H TO BE A 1
8804 022702 004737 006654                JSR      PC,READR4              ;GO READ VDAL AND PAUSE STATE MACHINE
8805 022706 001405                        BEQ      18$                    ;IF OK THEN CONTINUE
8806 022710                                ERRDF   3,VDALRG,R4EROR          ;EP8G H NOT 0 OR EP8N H NOT A 1
8807 022710 104455                        TRAP    C$ERDF
8808 022712 000C03                        .WORD   3
8809 022714 002537                        .WORD   VDALRG
8810 022716 005004                        .WORD   R4EROR
8811 022720                                CKLOOP
8812 022720 104406                        TRAP    C$CLP1
8813
8814                                     :SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE HIGH BYTE
8815                                     :OF THE NEW FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
8816                                     :BUS AT THIS TIME. ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
8817                                     :BUS WILL BE READBACK TO THE LSI-11 VIA THE SIGNAL RPi7 L.
8818
8819 022722 004737 007122                18$: JSR      PC,SEODAL              ;SELECT EODAL BUS VIA GDAL BITS 2:0
8820
8821                                     :AT THIS POINT IN TIME, THE HIGH BYTE OF THE NEW FORCE JUMP ADDRESS REG-
8822                                     :ISTER WILL BE ENABLED TO THE EODAL BUS VIA THE SIGNAL NEA8H L. THIS
8823                                     :SIGNAL IS ASSERTED LOW AS A RESULT OF "GET NEW ADDRESS"
8824                                     :FLIP-FLOP BEING SET AND THE SIGNAL EABH H BEING ASSERTED HIGH. THE
8825                                     : "GET NEW ADDRESS" FLIP-FLOP WAS SET WHEN THE PAUSE STATE SYNC FLIP
8826                                     :FLOP WAS A ONE, A PULSE ISSUED ON XRAS L, AND THE TAKE NEW FORCE
8827                                     :JUMP ADDRESS FLIP-FLOP WAS SET TO A ONE. THE SIGNAL EABH H IS ASSERTED
8828                                     :HIGH AS A RESULT OF THE 8 BIT ADDRESS HIGH BYTE FLIP-FLOP BEING SET TO A
8829                                     :ONE AND THE SIGNAL ACAS H BEING ASSERTED HIGH. THE FOLLOWING SECTION
8830                                     :WILL READ AND CHECK THAT THE HIGH BYTE OF THE NEW FORCE JUMP ADDRESS
8831                                     :REGISTER IS ENABLED TO THE EODAL BUS. THE EODAL BUS WILL BE READBACK
8832                                     :VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
8833                                     :
8834                                     :IF THE HIGH BYTE DATA READ FROM THE EODAL BUS EQUALS 314, THEN THE OLD
8835                                     :FORCE JUMP ADDRESS WAS PROBABLY ENABL'D TO THE EODAL BUS INSTEAD OF THE
8836                                     :NEW FORCE JUMP ADDRESS REGISTER. THE OLD FORCE JUMP ADDRESS REGISTER
8837                                     :WAS LOADED WITH DATA FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL
8838                                     :DFET H. THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH A DATA PATTERN
8839                                     :OF 146063 AT THE BEGINNING OF THE TEST.
8840

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8841	022726	011137	002342		MOV	(R1),R6LOAD	:GET DIAG ADDRESS REG DATA
8842	022732	000337	002342		SWAB	R6LOAD	:SWAP HIGH BYTE WITH LOW BYTE
8843	022736	042737	177400	002342	BIC	#177400,R6LOAD	:CLEAR LOW BYTE IN HIGH BYTE POSITION
8844	022744	012737	177400	002346	MOV	#177400,R6MASK	:SETUP TO IGNORE HIGH BYTE ON READ
8845	022752	004737	006700		JSR	PC,READR6	:READ OLD FJA HB ON EODAL BUS
8846	022756	001405			BEQ	19\$:OF OLD FLA OK THEN CONTINUE
8847	022760				ERRDF	4,FEODAL,R06ERR	:OLD FLA HB TO EODAL BUS ERROR
8848	022760	104455			TRAP	C\$EPDF	
8849	022762	000004			.WORD	4	
8850	022764	003147			.WORD	FEODAL	
8851	022766	005020			.WORD	R06ERR	
8852	022770				CKLOOP		
8853	022770	104406			TRAP	C\$CLP1	
8854							
8855							:RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8856							:GDAL BITS 1 AND 0 TO ONES
8857							
8858	022772	004737	006754		19\$: JSR	PC,SLHDAL	:GO SELECT HDAL REG VIA GDAL BITS 2:0
8859							
8860							:SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8861							
8862	022776	012737	021004	002342	MOV	#HDAL13!HDAL9!HDAL2,R6LOAD	:SETUP BITS PREVIOUSLY LOADED
8863	023004	005037	002346		CLR	R6MASK	:SETUP TO CHECK ALL BITS
8864	023010	004737	007442		JSR	PC,XCASL	:SET XCAS H TO LOW STATE VIA HDAL13 H
8865							
8866							:TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H. THIS IS DONE
8867							:TO SIMULATE A MACHINE CYCLE.
8868							
8869	023014	004737	007502		JSR	PC,XPI	:GO PULSE XPI H VIA HDAL15 H
8870							
8871							:TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8872							:WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8873							:EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
8874							:EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL PB H
8875							:WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H AND
8876							:RASP L WILL BE PULSED.
8877							:THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L WHEN
8878							:THE SIGNALS EPFN L AND PSMW H ARE ASSERTED HIGH AND THE THE SIGNAL
8879							:EP8N L IS ASSERTED LOW. A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H
8880							:WILL BE ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP
8881							:BEING CLEARED.
8882							
8883	023020	004737	007272		JSR	PC,XRAS	:GGO PULSE XRAS H AND XRAS L VIA HDAL12
8884							
8885							:READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE TO BE IN THE
8886							:FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8887							: PAUSE STATE WORKING - PSMW H - 0
8888							: PAUSE STATE SYNC - EPSF H - 0
8889							: 8 BIT INSTRUCTION HB - EP8F H - 0
8890							: 8 BIT ADDRESS HB - EP8G H - 0
8891							: 8 BIT ADDRESS LB - EP8N H - 0
8892							: TAKE NEW FJ ADDRESS - TNFJ H - 0
8893							: GET NEW ADDRESS - OUTNEW H - 1
8894							
8895	023024	042737	001000	002336	BIC	#VDAL9,R4GOOD	:EXPECT PSMW H TO BE A ZERO
8896	023032	004737	006654		JSR	PC,READR4	:READ VDAL AND PAUSE STATE MACHINE

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8897 023036 001405      BEQ      20$                ;IF OK THEN CONTINUE
8898 023040              ERRDF    3,VDALRG,R4EROR      ;PSMW H F/F PROBABLY NOT CLEARED
8899 023040 104455      TRAP     C$ERDF
8900 023042 000003      .WORD   3
8901 023044 002537      .WORD   VDALRG
8902 023046 005004      .WORD   R4EROR
8903 023050              CKLOOP
8904 023050 104406      TRAP     C$CLP1
8905
8906                      ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. THE
8907                      ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT ADDRESS LB FLIP-
8908                      ;FLOP (0) INTO THE 8 BIT ADDRESS HB FLIP-FLOP, THUS SETTING THE 8 BIT
8909                      ;ADDRESS HB FLIP-FLOP TO A ZERO.
8910
8911 023052 004737 007376 20$: JSR      PC,XCAS                ;GO PULSE XCAS H VIA HDAL13 H
8912
8913                      ;READ THE VDAL REGISTER AND THE PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
8914                      ;THE FOLLOWING STATES AS A RESULT OF XCAS H BEING PULSED.
8915                      ;
8916                      ; PAUSE STATE WORKING - PSMW H - 0
8917                      ;
8918                      ; PAUSE STATE SYNC - EPSF H - 0
8919                      ;
8920                      ; 8 BIT INSTRUCTION HB - EP8F H - 0
8921                      ;
8922                      ; 8 BIT ADDRESS LB - EP8G H - 0
8923                      ;
8924                      ; 8 BIT ADDRESS HB - EP8N H - 0
8925                      ;
8926                      ; TAKE NEW FJ ADDRESS - TNFJ H - 0
8927                      ;
8928                      ; GET NEW ADDRESS - OUTNEW H - 1
8929
8923 023056 042737 040000 002336 BIC     #VDAL14,R4GOOD      ;EXPECT EP8N H TO BE A ZERO
8924 023064 004737 006654          JSR     PC,READR4          ;GO READ VDAL AND PAUSE STATE MACHINE
8925 023070 001405          BEQ     21$                ;IF OK THEN CONTINUE
8926 023072              ERRDF    3,VDALRG,R4EROR      ;EP8N H PROBABLY NOT CLEARED
8927 023072 104455      TRAP     C$ERDF
8928 023074 000003      .WORD   3
8929 023076 002537      .WORD   VDALRG
8930 023100 005004      .WORD   R4EROR
8931 023102              CKLOOP
8932 023102 104406      TRAP     C$CLP1
8933
8934                      ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
8935                      ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
8936
8937 023104 004737 007502 21$: JSR      PC,XPI                ;GO PULSE XPI VIA HDAL15 H
8938
8939                      ;SET VDAL2 H TO A ONE AND THEN ZERO TO CLEAR THE "GET NEW ADDRESS" FLIP-
8940                      ;FLOP.
8941
8942 023110 005037 002334 CLR     R4LOAD              ;SETUP TO EXPECT ALL BITS CLEARED
8943 023114 004737 007712 JSR     PC,CLRPSM          ;GO CLEAR PAUSE STATE MACHINE F/F'S
8944
8945                      ENDSEG
8946                      10000$:
8947 023120 104405      TRAP     C$ESEG
8948
8949 023122 005721          TST     (R1)+             ;UPDATE TABLE POINTER
8950 023124 005302          DEC     R2              ;CHECK IF ALL PATTERNS DONE
8951 023126 001412          BEQ     23$             ;IF YES THEN EXIT
8952 023130 000137 021620 JMP     1$                ;DO NEXT PATTERN

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8953				
8954	023134	125125	22\$:	.WORD 125125
8955	023136	052652		.WORD 052652
8956	023140	000377		.WORD 000377
8957	023142	177400		.WORD 177400
8958	023144	125252		.WORD 125252
8959	023146	052525		.WORD 052525
8960	023150	177777		.WORD 177777
8961	023152	000000		.WORD 000000
8962				
8963	023154		23\$:	ENDTST
8964	023154		L10064:	
8965	023154	104401		TRAP CSETST
8966				

TEST 35: CLEAR PAUSE STATE MACHINE VIA VDAL2 H - 8 BIT ADDRESS

.SBTTL TEST 35: CLEAR PAUSE STATE MACHINE VIA VDAL2 H - 8 BIT ADDRESS

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:++
: THIS TEST WILL CHECK THAT THE PAUSE STATE MACHINE FLIP - FLOPS,
: PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT
: ADDRESS LB, AND 8 BIT ADDRESS HB, CAN BE CLEARED WHEN THE SIGNAL VDAL2 H IS
: ASSERTED HIGH. ALL THE ABOVE FLIP-FLOPS ARE SET TO A ONE BY SETTING THE
: SIGNAL FETCT H TO A ONE, SETTING THE SIGNAL ADAL4 H TO A ZERO, AND PULSING
: THE SIGNALS XRAS H AND XCAS H. ONCE ALL THE FLIP-FLOPS ARE SET TO ONES, THE
: TEST WILL SET THE SIGNAL VDAL2 H AND CHECK THAT ALL THE PAUSE STATE MACHINE
: FLIP-FLOPS CLEARED.
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023156
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023156 004737 005510

023162
023162 104404

023164 004737 007006

023170 012737 004000 002342
023176 004737 006672
023202 001405
023204
023204 104455
023206 000004
023210 002631
023212 005020
023214
023214 104406

023216 005037 002330
023222 004737 007772

023226 012737 000200 002334
023234 004737 007712

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T35::  BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR

      BGNSEG
      TRAP   C$BSEG

      ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO
      ;TO A ZERO.

      JSR    PC,SLMODR          ;GO SELECT MODE REG VIA CONTROL REG 0

      ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000. MR BIT 11
      ;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

      MOV    #MR11,R6LOAD      ;SETUP TO SET MR BIT 11
      JSR    PC,LDRDR6         ;LOAD, READ AND CHECK MODE REGISTER
      BEQ    1$                ;IF LOADED OK THEN CONTINUE
      ERRDF  4,MODREG,R06ERR   ;MODE REGISTER NOT EQUAL TO 0
      TRAP   C$ERRDF

      .WORD  4
      .WORD  MODREG
      .WORD  R06ERR
      CKLOOP
      TRAP   C$CLP1

      ;LOAD, READ AND CHECK ADAL REGISTER. ADALO WILL BE SET AND CLEARED
      ;TO CLEAR THE BREAK LOGIC. ADAL4 ON A ZERO WILL PUT THE PAUSE STATE
      ;MACHINE IN THE PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
      ;BREAK SIGNAL FROM CAUSING A BREAK CONDITION. ADAL4 H ON A ZERO WILL
      ;CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
      ;SIGNAL XRAS H IS PULSED.

      1$: CLR    R2LOAD          ;SETUP TO CLEAR ALL ADAL REG BITS
          JSR    PC,BRKRES      ;PULSE BRKRES L VIA ADALO H

      ;SET VDAL7 AND VDAL2 TO ONES IN THE VDAL REGISTER. VDAL7 ON A ONE WILL
      ;SET THE SIGNAL FETCT H TO THE HIGH STATE. VDAL2 ON A ONE WILL CLEAR
      ;THE PAUSE STATE MACHINE FLIP-FLOPS. VDAL2 WILL BE RESET TO 0 AFTER
      ;BEING SET TO A ONE.

      MOV    #VDAL7,R4LOAD     ;SETUP BIT TO SET FETCT H
      JSR    PC,CLRPSM        ;SET FETCT H AND PULSE INVD L VIA VDAL2 H
  
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TEST 35: CLEAR PAUSE STATE MACHINE VIA VDAL2 H - 8 BIT ADDRESS

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9023
9024           ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
9025           ;TO ONES. BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
9026           ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L.
9027
9028 023240 004737 006754 JSR    PC,SLHDAL           ;GO SELECT HDAL REG VIA GDAL 2:0
9029
9030           ;CLEAR ALL BITS IN THE HDAL REGISTER EXCEPT HDAL2 H. HDAL2 H ON A ONE
9031           ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
9032           ;THE HDAL BITS ARE CLEARED HERE TO INSURE THAT ALL SIGNALS ARE IN A
9033           ;KNOWN STATE WHEN SCOPE LOOPING IS INVOKED BY THE USER
9034
9035 023244 012737 000004 002342 MOV    #HDAL2,R6LOAD       ;SETUP BIT TO BE SET TO A ONE
9036 023252 004737 006672 JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
9037 023256 001405 BEQ    2$                ;IF LOADED OK THEN CONTINUE
9038 023260 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
9039 023260 104455 TRAP  C$ERDF
9040 023262 000004 .WORD 4
9041 023264 002605 .WORD HDALRG
9042 023266 005020 .WORD R06ERR
9043 023270 CKLOOP
9044 023270 104406 TRAP  C$CLP1
9045
9046           ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING THE SIGNAL HDAL12 H.
9047           ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
9048           ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
9049           ;HIGH STATE. THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
9050           ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
9051           ;TO THE HIGH STATE. THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
9052           ;SIGNAL PAUSE L IS ASSERTED HIGH. WHEN SOP H AND EDFET H ARE ASSERTED
9053           ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
9054           ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
9055           ;PSMW H WILL BE ASSERTED HIGH. THE SIGNAL PSMW H IS READ IN THE VDAL
9056           ;REGISTER AS VDAL9 H. WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
9057           ;SIGNAL PB H WILL BE ASSERTED HIGH. THE SIGNAL PB H IS THE DATA INPUT
9058           ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
9059
9060 023272 004737 007272 2$: JSR    PC,XRAS           ;PULSE XRAS H VIA HDAL12 H
9061
9062           ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
9063           ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNALS EDFET H AND SOP H
9064           ;BEING ASSERTED HIGH.
9065           ; PAUSE STATE WORKING - PSMW H - 1
9066           ; PAUSE STATE SYNC - EPSF H - 0
9067           ; 8 BIT INSTRUCTION HB - EP8F H - 0
9068           ; 8 BIT ADDRESS LB H - EP8G H - 0
9069           ; 8 BIT ADDRESS HB H - EP8N H - 0
9070
9071 023276 052737 001000 002336 BIS    #VDAL9,R4GOOD       ;EXPECT PSMW H TO BE SET
9072 023304 004737 006654 JSR    PC,READR4          ;CHECK VDAL AND PAUSE STATE MACHINE
9073 023310 001405 BEQ    3$                ;IF LOADED OK THEN CONTINUE
9074 023312 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
9075 023312 104455 TRAP  C$ERDF
9076 023314 000003 .WORD 3
9077 023316 002537 .WORD VDALRG
9078 023320 005004 .WORD R4EROR

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9079 023322          CKLOOP
9080 023322 104406   TRAP    C$CLP1
9081
9082                ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13. THE SIGNAL
9083                ;XCAS H WILL CLOCK THE PAUSE STATE SYNC FLIP-FLOP WITH THE LEVEL OF THE
9084                ;SIGNAL 'PB H', WHICH IS HIGH, THUS SETTING THE PAUSE STATE SYNC
9085                ;FLIP-FLOP TO A ONE. THE SIGNAL XCAS H WILL ALSO CLOCK THE 8 BIT
9086                ;INSTRUCTION HB FLIP-FLOP WITH THE OUTPUT OF THE PAUSE STATE SYNC F/F
9087                ;WHICH WAS 0 BEFORE IT WAS SET TO A ONE BY XCAS H. THEREFORE 8 BIT
9088                ;INSTRUCTION HB FLIP-FLOP WILL BE CLOCKED TO A ZERO STATE.
9089
9090 023324 004737 007376   3$: JSR    PC,XCAS          ;GO PULSE XCAS H VIA HDAL13
9091
9092                ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
9093                ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING PULSED.
9094                ; PAUSE STATE WORKING - PSMW H - 1
9095                ; PAUSE STATE SYNC - EPSF H - 1
9096                ; 8 BIT INSTRUCTION HB - EP8F H - 0
9097                ; 8 BIT ADDRESS LB - EP8G H - 0
9098                ; 8 BIT ADDRESS HB - EP8N H - 0
9099
9100 023330 052737 002000 002336   BIS    #VDAL10,R4GOOD      ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
9101 023336 004737 006654          JSR    PC,READR4          ;GO READ AND CHECK PAUSE STATE MACHINE
9102 023342 001405          BEQ    4$                ;IF LOADED OK THEN CONTINUE
9103 023344          ERRDF 3,VDALRG,R4EROR      ;EPSF H PROBABLE NOT SET IN VDAL REG
9104 023344 104455          TRAP  C$ERDF
9105 023346 000003          .WORD 3
9106 023350 002537          .WORD VDALRG
9107 023352 005004          .WORD R4EROR
9108 023354          CKLOOP
9109 023354 104406          TRAP  C$CLP1
9110
9111                ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H. THE
9112                ;SIGNAL XCASH WILL CLOCK THE OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
9113                ;INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THE 8 BIT INSTRUC-
9114                ;TION HB FLIP-FLOP TO A ONE.
9115
9116 023356 004737 007376   4$: JSR    PC,XCAS          ;GO PULSE XCAS H VIA HDAL13 H
9117
9118                ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
9119                ;IN THE FOLLOWING STATE AS A RESULT OF PULSING THE SIGNAL XCAS H
9120                ; PAUSE STATE WORKING - PSMW H - 1
9121                ; PAUSE STATE SYNC - EPSF H - 1
9122                ; 8 BIT INSTRUCTION HB - EP8F H - 1
9123                ; 8 BIT ADDRESS LB - EP8G H - 0
9124                ; 8 BIT ADDRESS HB - EP8N H - 0
9125
9126 023362 052737 010000 002336   BIS    #VDAL12,R4GOOD      ;SETUP TO EXPECT EP8F H TO BE A 1
9127 023370 004737 006654          JSR    PC,READR4          ;GO READ VDAL AND PAUSE STATE MACHINE
9128 023374 001405          BFO    5$                ;IF OK THEN CONTINUE
9129 023376          ERRDF 3,VDALRG,R4EROR      ;EP8F H PROBABLY NOT SET TO A 1
9130 023376 104455          TRAP  C$ERDF
9131 023400 000003          .WORD 3
9132 023402 002537          .WORD VDALRG
9133 023404 005004          .WORD R4EROR
9134 023406          CKLOOP

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9135 023406 104406 TRAP C$CLP1
9136
9137 ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H. THE
9138 ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-
9139 ;FLOP (1) INTO THE 8 BIT ADDRESS LB FLIP-FLOP, THUS SETTING THE 8 BIT
9140 ;ADDRESS LB FLIP-FLOP TO A ONE.
9141
9142 023410 004737 007376 5$: JSR PC,XCAS ;GO PULSE XCAS H VIA HDAL13 H
9143
9144 ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
9145 ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
9146 ; PAUSE STATE WORKING - PSMW H - 1
9147 ; PAUSE STATE SYNC - EPSF H - 1
9148 ; 8 BIT INSTRUCTION HB - EP8F H - 1
9149 ; 8 BIT ADDRESS LB - EP8G H - 1
9150 ; 8 BIT ADDRESS HB - EP8N H - 0
9151
9152 023414 052737 020000 002336 BIS #VDAL13,R4GOOD ;SETUP TO EXPECT EP8G H TO BE A ONE
9153 023422 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
9154 023426 001405 BEQ 6$ ;IF OK THEN CONTINUE
9155 023430 ERRDF 3,VDALRG,R4EROR ;EP8G H PROBABLY NOT SET
9156 023430 104455 TRAP C$ERDF
9157 023430 000003 .WORD 3
9158 023434 002537 .WORD VDALRG
9159 023436 005004 .WORD R4EROR
9160 023440 CKLOOP
9161 023440 104406 TRAP C$CLP1
9162
9163 ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H. THE
9164 ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP
9165 ;(1) INTO THE 8 BIT ADDRESS HB FLIP-FLOP, THUS SETTING THE 8 BIT ADDRESS
9166 ;HB FLIP-FLOP TO A ONE
9167
9168 023442 004737 007376 6$: JSR PC,XCAS ;GO PULSE XCAS H VIA HDAL13 H
9169
9170 ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
9171 ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
9172 ; PAUSE STATE WORKING - PSMW H - 1
9173 ; PAUSE STATE SYNC - EPSF H - 1
9174 ; 8 BIT INSTRUCTION HB - EP8F H - 1
9175 ; 8 BIT ADDRESS LB - EP8G H - 1
9176 ; 8 BIT ADDRESS HB - EP8N H - 1
9177
9178 023446 052737 040000 002336 BIS #VDAL14,R4GOOD ;SETUP TO EXPECT EP8N H TO BE A 1
9179 023454 004737 006654 JSR PC,READR4 ;GO CHECK VDAL AND PAUSE STATE MACHINE
9180 023460 001405 BEQ 7$ ;IF OK THEN CONTINUE
9181 023462 ERRDF 3,VDALRG,R4EROR ;EP8N H PROBABLY NOT SET TO A 1
9182 023462 104455 TRAP C$ERDF
9183 023464 000003 .WORD 3
9184 023466 002537 .WORD VDALRG
9185 023470 005004 .WORD R4EROR
9186 023472 CKLOOP
9187 023472 104406 TRAP C$CLP1
9188
9189 ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL15 H. A PULSE
9190 ;ON THE SIGNAL XPI L WILL CLEAR THE EDFET FLIP-FLOP, THUS DISABLING
  
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TEST 35: CLEAR PAUSE STATE MACHINE VIA VDAL2 H - 8 BIT ADDRESS

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9191 ;THE DIRECT SET INPUT TO THE PAUSE STATE WORKING FLIP-FLOP.
9192
9193 023474 004737 007502 7$: JSR PC,XPI ;GO PULSE XPI L VIA HDAL15 H
9194
9195 ;READ THE VDAL AND PAUSE STATE MACHINE FLIP-FLOPS TO CHECK THAT XPI L
9196 ;DID NOT CLEAR ANY OF THE PAUSE STATE MACHINE FLIP-FLOPS.
9197
9198 023500 004737 006654 JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
9199 023504 001405 BEQ 8$ ;IF NO CHANGES THEN CONTINUE
9200 023506 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE EROR
9201 023506 104455 TRAP C$ERDF
9202 023510 000003 .WORD 3
9203 023512 002537 .WORD VDALRG
9204 023514 005004 .WORD R4EROR
9205 023516 CKLOOP
9206 023516 104406 TRAP C$CLP1
9207
9208 ;SET THE SIGNAL VDAL2 H TO A ONE AND CHECK THE PAUSE STATE MACHINE FLIP-
9209 ;FLOPS TO BE A ZERO. VDAL2 H WILL THEN BE CLEARED.
9210
9211 023520 005037 002334 8$: CLR R4LOAD ;SETUP TO EXPECT PAUSE STATE CLEARED
9212 023524 004737 007712 JSR PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
9213
9214 023530 ENDSEG
9215 023530 10000$: TRAP C$ESEG
9216 023530 104405 ENDTST
9217 023532
9218 023532 L10065: TRAP C$ETST
9219 023532 104401
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TEST 36: EOAI REG TO CAI, EIAI, CTL AND TO CTL REG TEST

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 023534 004737 005510
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 023542
 023542 104404
 023544 004737 007006
 023550 005037 002342
 023554 004737 006672
 023560 001405
 023562 104455
 023564 000004
 023566 002631
 023570 005020
 023572 104406
 023600 012737 000004 002342
 023606 004737 006672
 023612 001405
 023614 104455
 023616 000004
 023620 002605
 023622 005020
 023624

.SBTTL TEST 36: EOAI REG TO CAI, EIAI, CTL AND TO CTL REG TEST

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: THIS TEST WILL CHECK THAT THE EOAI REGISTER BITS 7:0 CAN BE LOADED AND READ
: BACK CORRECTLY. THE TEST WILL ALSO CHECK THE DATA PATH TO BE CONNECTED AND
: FUNCTIONING PROPERLY FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS,
: TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE TEST WILL CHECK
: THE DATA PATH FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE
: TAI BUS, TO THE TAI DIAGNOSTIC LATCH, AND BACK FROM THE TAI DIAGNOSTIC LATCH
: TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE
: DATA PATTERN USED DURING THIS TEST WILL BE AN INCREMENTING BINARY COUNT PATTERN.
: THE DATA READBACK FROM THE CTL REGISTER WILL BE THE ONES COMPLEMENT OF THE DATA
: LOADED INTO THE EOAI REGISTER.
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T36::  BGNTST
      JSR  PC,INITTE      ;SELECT AND INITIALZE TARGET EMULATOR
      CLR  R1             ;START DATA PATTERN AT ZERO

1$:   BGNSEG
      TRAP C$BSEG
      ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0

      JSR  PC,SLMODR     ;SELECT MODE REG VIA GDAL BITS 2:0
      ;CLEAR ALL BITS IN THE MODE REGISTER AND CHECK THAT ALL BITS ARE CLEARED

      CLR  R6LOAD        ;SETUP TO CLEAR ALL BITS
      JSR  PC,LDRDR6     ;GO LOAD, READ AND CHECK MODE REGISTER
      BEQ  2$            ;IF LOADED OK THEN CONTINUE
      ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
      TRAP C$ERRDF
      .WORD 4
      .WORD MODREG
      .WORD R06ERR
      CKLOOP
      TRAP C$CLP1

      ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

2$:   JSR  PC,SLHDAL     ;SELECT HDAL REG VIA GDAL BITS 2:0
      ;SET HDAL2 H TO A ONE IN THE HDAL REGISTER TO ALLOW THE PROGRAM TO
      ;CONTROL THE T-11 TIMING AND CONTROL SIGNALS.

      MOV  #HDAL2,R6LOAD ;SETUP BIT TO BE LOADED
      JSR  PC,LDRDR6     ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ  3$            ;IF LOADED OK THEN CONTINUE
      ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL TO EXPECTED
      TRAP C$ERRDF
      .WORD 4
      .WORD HDALRG
      .WORD R06ERR
      CKLOOP
  
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9277 023624 104406          TRAP    C$CLP1
9278
9279                          ;SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4. VDAL2 H BEING PULSED
9280                          ;WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS TO BE CLEARED VIA THE
9281                          ;SIGNALS INV D L AND INV D H.
9282
9283 023626 005037 002334    3$:   CLR    R4LOAD          ;SETUP TO CLEAR ALL OTHER VDAL R/W BITS
9284 023632 004737 007712          JSR    PC,CLRPSM      ;GO PULSE INV D L VIA VDAL2 H
9285
9286                          ;SET ADAL13 H AND ADAL10 H TO ONES IN THE ADAL REGISTER. THE SIGNAL
9287                          ;ATC L WILL BE ASSERTED HIGH WHEN ADAL13 H IS A ONE, ADAL11 H IS A ZERO,
9288                          ;THE PAUSE STATE WORKING FLIP-FLOP IS A ZERO, AND PPI L IS ASSERTED HIGH.
9289                          ;ADAL10 H ON A ONE WILL ENABLE THE EIAI 7:0 BUS TO THE CTL 7:0 BUS.
9290
9291 023636 012737 022000 002330  MOV    #ADAL13!ADAL10,R2LOAD ;SETUP BITS TO BE LOADED
9292 023644 004737 006614          JSR    PC,LDRDR2     ;GO LOAD, READ AND CHECK ADAL REGISTER
9293 023650 001405          BEQ    4$           ;IF LOADED OK THEN CONTINUE
9294 023652          ERRDF  2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
9295 023652 104455          TRAP  C$ERDF
9296 023654 000002          .WORD 2
9297 023656 002513          .WORD ADALRG
9298 023660 004770          .WORD R2EROR
9299 023662          CKLOOP
9300 023662 104406          TRAP  C$CLP1
9301
9302                          ;SELECT FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9303
9304 023664 004737 007154    4$:   JSR    PC,SLFDAL      ;GO SELECT FDAL REG VIA GDAL BITS 2:0
9305
9306                          ;LOAD, READ AND CHECK EOAI REGISTER WITH A BINARY COUNT PATTERN. THE
9307                          ;EOAI REGISTER IS THE HIGH BYTE OF THE FAL REGISTER. THE DATA
9308                          ;PATTERN WILL BE LOADED INTO THE EOAI REGISTER VIA THE SIGNAL WPT2 HB H
9309                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6. FDALO H WILL
9310                          ;BE WRITTEN TO A ONE IN THE FDAL REGISTER AT THE SAME TIME THE EOAI
9311                          ;REGISTER IS WRITTEN. FDALO H ON A ONE WILL ENABLE THE EOAI REGISTER
9312                          ;TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE
9313                          ;CTL REGISTER. THE EOAI REGISTER IS READBACK VIA THE SIGNAL RAT2 L.
9314
9315 023670 010137 002342    MOV    R1,R6LOAD      ;GET THE BINARY DATA PATTERN
9316 023674 005237 002342    INC    R6LOAD         ;SET FDALO H TO A ONE
9317 023700 004737 006672    JSR    PC,LDRDR6     ;LOAD, READ AND CHECK EOAI AND FDAL REG
9318 023704 001405    BEQ    5$           ;IF LOADED OK THEN CONTINUE
9319 023706    ERRDF  4,EOAIFD,R06ERR ;EOAI OR FDAL REGISTER ERROR
9320 023706 104455    TRAP  C$ERDF
9321 023710 000004    .WORD 4
9322 023712 002676    .WORD EOAIFD
9323 023714 005020    .WORD R06ERR
9324 023716    CKLOOP
9325 023716 104406    TRAP  C$CLP1
9326
9327                          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9328
9329 023720 004737 006754    5$:   JSR    PC,SLHDAL      ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
9330
9331                          ;SET PPI L AND XPI L TO THE LOW STATE BY SETTING HDAL15 H TO A ONE.
9332                          ;PPI L BEING SET LOW WILL CAUSE THE SIGNAL ATC L TO BE ASSERTED LOW.

```

TEST 36: EOAI REG TO CAI, EIAI, CTL AND TO CTL REG TEST

```

9333      ;ATC L ASSERTED LOW WILL ENABLE THE EOAI BUS ONTO THE CAI 7:0 BUS. THE
9334      ;CAI BUS WILL BE ENABLED TO THE EIAI 7:0 BUS UNCONDITIONALLY. THE
9335      ;EIAI BUS WILL BE ENABLED TO THE CTL 7:0 BUS VIA ADAL10 H ON A ONE.
9336      ;THE CAI 7:0 BUS WILL ALSO BE ENABLED TO THE TAI 7:0 BUS BY THE SIGNAL
9337      ;ATT L BEING ASSERTED LOW. THE SIGNAL ATT L IS ASSERTED LOW AS A RESULT
9338      ;OF THE SIGNALS CPI L, MR9 L, AND DMG L BEING ASSERTED HIGH.
9339
9340 023724 012737 000004 002342      MOV      #HDAL2,R6LOAD      ;SETUP BIT PREVIOUSLY LOADED
9341 023732 004737 007514              JSR      PC,XPIH           ;SET PPI L AND XPI L TO LOW STATE
9342
9343      ;SET AND CLEAR VDAL2 H IN THE VDAL REGISTER TO CLOCK THE TAI 7:0 BUS
9344      ;INTO THE TAI 7:0 DIAGNOSTIC LATCH. THE DATA CLOCKED INTO THE TAI
9345      ;DIAGNOSTIC LATCH SHOULD BE THAT WHICH WAS WRITTEN INTO THE EOAI REG.
9346
9347 023736 004737 007712      JSR      PC,CLRPSM        ;GO PULSE VDAL2 H TO CLOCK TAI INTO LATCH
9348
9349      ;AT THIS TIME, THE EOAI BUS IS ENABLED TO THE CAI BUS VIA THE SIGNAL
9350      ;ATC L. THE CAI BUS IS ENABLED TO THE EIAI BUS UNCONDITIONALLY. THE
9351      ;EIAI BUS IS ENABLED TO THE CTL BUS VIA ADAL10 H ON A ONE. TO CHECK
9352      ;THAT THE EOAI BUS IS ENABLED TO THE CTL BUS, THE TEST MUST FIRST
9353      ;CLOCK THE CTL BUS DATA INTO THE CTL REGISTER BY PULSING THE SIGNAL
9354      ;XCAS L. THE SIGNAL XCAS L IS PULSED BY SETTING AND CLEARING HDAL13 H.
9355
9356 023742 004737 007376      JSR      PC,XCAS          ;PULSE XCAS L VIA HDAL REGISTER BIT 13
9357
9358      ;SET PPI L AND XPI L TO THE HIGH STATE BY CLEARING THE SIGNAL HDAL15 H.
9359      ;THE EOAI BUS WILL BE DISABLED FROM THE CAI BUS BY ATC L BEING SET
9360      ;HIGH WHEN THE SIGNAL PPI L IS RETURNED TO THE HIGH STATE.
9361
9362 023746 004737 007546      JSR      PC,XPIL          ;GO SET PPI L AND XPI L TO HIGH STATE
9363
9364      ;SELECT FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9365
9366 023752 004737 007154      JSR      PC,SLFDAL        ;GO SELECT FDAL REG VIA GDAL BITS 2:0
9367
9368      ;WRITE THE DATA PATTERN 314 INTO THE EOAI REGISTER VIA THE SIGNAL WPT2
9369      ;HB H. THIS IS DONE TO CHECK THAT THE CTL REGISTER IS READBACK ON A
9370      ;READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE EOAI REGISTER. THE
9371      ;SIGNAL FDALO H WILL BE WRITTEN TO A ZERO TO SELECT THE CTL REGISTER
9372      ;TO BE READ VIA THE SIGNAL ROT2 L WHEN A READ COMMAND IS ISSUED TO
9373      ;CONTROL REGISTER 6.
9374
9375 023756 012777 146000 156322      MOV      #146000,@REG6    ;WRITE EOAI AND FDAL REGISTER
9376
9377      ;READ THE CTL AND FDAL REGISTER TO CHECK THAT XCAS L CLOCKED THE CTL
9378      ;7:0 BUS INTO THE CTL REGISTER. THE CTL REGISTER WILL BE READBACK VIA
9379      ;THE SIGNAL ROT2 L WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
9380      ;THE DATA READBACK WILL BE THE ONES COMPLEMENT OF THE DATA WHICH WAS
9381      ;WRITTEN INTO THE EOAI REGISTER AT THE BEGINNING OF THIS TEST.
9382
9383 023764 010137 002342      MOV      R1,R6LOAD        ;SETUP DATA LOADED INTO EOAI
9384 023770 005137 002342      COM      R6LOAD           ;MAKE THE 1'S COMPLEMENT FOR READBACK
9385 023774 042737 000377 002342      BIC      #377,R6LOAD      ;CLEAR THE FDAL REGISTER BITS
9386 024002 004737 006700      JSR      PC,READR6        ;GO READ CTL AND FDAL REGISTER
9387 024006 001405      BEQ      6$              ;IF DATA OK THEN CONTINUE
9388 024010      ERRDF 4,CTLFDL,R026ER    ;CTL OR FDAL REGISTER ERROR

```

9389	024010	104455			TRAP	C\$ERDF	
9390	024012	000004			.WORD	4	
9391	024014	003232			.WORD	CTLFDL	
9392	024016	005034			.WORD	R026ER	
9393	024020				CKLOOP		
9394	024020	104406			TRAP	C\$CLP1	
9395							
9396							
9397							
9398							
9399							
9400							
9401							
9402	024022	010137	002342				
9403	024026	005137	002342	6\$:	MOV	R1,R6_OAD	:GET THE DATA PATTERN JUST LOADED
9404	024032	042737	000376	002342	COM	R6LOAD	:MAKE THE 1'S COMPLEMENT OF IT
9405	024040	004737	006672		BIC	#376,R6LOAD	:CLEAR FDAL BITS 7:1 - FDALO H = 1
9406	024044	001405			JSR	PC,LDRDR6	:LOAD, READ AND CHECK EOAI AND FDAL REG
9407	024046				BEQ	7\$:IF LOADED OK THEN CONTINUE
9408	024046	104455			ERRDF	4,EOAIFD,R06ERR	:EOAI OR FDAL REGISTER ERROR
9409	024050	000004			TRAP	C\$ERDF	
9410	024052	002676			.WORD	4	
9411	024054	005020			.WORD	EOAIFD	
9412	024056				.WORD	R06ERR	
9413	024056	104406			CKLOOP		
9414					TRAP	C\$CLP1	
9415							
9416							
9417	024060	004737	006754	7\$:	JSR	PC,SLHDAL	:SELECT HDAL REGISTER VIA GDAL BITS 2:0
9418							
9419							
9420							
9421							
9422							
9423							
9424							
9425	024064	012737	000004	002342	MOV	#HDAL2,R6LOAD	:SETUP BIT PREVIOUSLY LOADED
9426	024072	004737	007514		JSR	PC,XPIH	:SET PPI L AND XPI L TO LOW STATE
9427							
9428							
9429							
9430							
9431							
9432	024076	004737	007376		JSR	PC,XCAS	:GO PULSE XCAS L VIA HDAL13 H
9433							
9434							
9435							
9436							
9437							
9438	024102	004737	007546		JSR	PC,XPIL	:SET PPI L AND XPI L TO HIGH STATE
9439							
9440							
9441							
9442	024106	004737	007154		JSR	PC,SLFDAL	:GO SELECT FDAL REG VIA GDAL BITS 2:0
9443							
9444							

:WRITE THE DATA PATTERN 063 INTO THE EOAI REGISTER VIA THE SIGNAL WPT2

```

9445 ;HB H. THIS IS DONE TO CHECK THAT THE CTL REGISTER IS READBACK VIA
9446 ;THE SIGNAL ROT2 L INSTEAD OF THE EOAI REGISTER. FDALO H WILL BE WRITTEN
9447 ;TO A ZERO TO SELECT THE CTL REGISTER
9448
9449 024112 012777 031400 156166 MOV #031400,@REG6 ;WRITE EOAI AND FDAL REGISTER
9450
9451 ;READ THE CTL AND FDAL REGISTERS TO CHECK THAT XCAS L CLOCKED THE CTL
9452 ;BUS INTO THE CTL REGISTER. THE DATA PATTERN READBACK WILL BE THE
9453 ;ONES COMPLEMENT OF THAT WHICH WAS WRITTEN INTO THE EOAI REGISTER.
9454
9455 024120 010137 002342 MOV R1,R6LOAD ;GET THE 1'S COMPLEMENT OF DATA LOADED
9456 024124 004737 006700 JSR PC,READR6 ;GO READ CTL AND FDAL REGISTER
9457 024130 001405 BEQ 8$ ;IF DATA OK THEN CONTINUE
9458 024132 ERRDF 4,CTLFDL,R026ER ;CTL OR FDAL REGISTER ERROR
9459 024132 104455 TRAP C$ERDF
9460 024134 000004 .WORD 4
9461 024136 003232 .WORD CTLFDL
9462 024140 005034 .WORD R026ER
9463 024142 CKLOOP
9464 024142 104406 TRAP C$CLP1
9465
9466 ;SET ADAL13 H TO A ZERO IN THE ADAL REGISTER. ADAL13 H ON A ZERO WILL
9467 ;ALLOW THE SIGNALS ABT H AND ABT L TO BE ASSERTED HIGH AND LOW RESPEC-
9468 ;TIVELY WHEN THE SIGNAL PPI L IS ASSERTED LOW. THE SIGNALS ABT H AND
9469 ;ABT L WILL ENABLE THE TAI BUS TO THE CAI BUS WHEN ASSERTED.
9470
9471 024144 042737 020000 002330 8$: BIC #ADAL13,R2LOAD ;SETUP TO ZERO ADAL13
9472 024152 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
9473 024156 001405 BEQ 9$ ;IF LOADED OK THEN CONTINUE
9474 024160 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
9475 024160 104455 TRAP C$ERDF
9476 024162 000002 .WORD 2
9477 024164 002513 .WORD ADALRG
9478 024166 004770 .WORD R2EROR
9479 024170 CKLOOP
9480 024170 104406 TRAP C$CLP1
9481
9482 ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9483
9484 024172 004737 007006 9$: JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0
9485
9486 ;SET MODE REGISTER BIT 9 TO A ONE. THIS IS DONE TO SET THE SIGNAL ATT L
9487 ;TO THE HIGH STATE. WHEN THE SIGNAL ATT L IS ASSERTED HIGH, THE CAI
9488 ;BUS WILL BE DISABLED TO THE TAI BUS AND THE TAI DIAGNOSTIC LATCH WILL
9489 ;BE ALLOWED TO DRIVE THE TAI BUS.
9490
9491 024176 012737 001000 002342 MOV #MR9,R6LOAD ;SETUP BIT TO BE LOADED
9492 024204 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
9493 024210 001405 BEQ 10$ ;IF LOADED OK THEN CONTINUE
9494 024212 ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL EXPECTED
9495 024212 104455 TRAP C$ERDF
9496 024214 000004 .WORD 4
9497 024216 002631 .WORD MODREG
9498 024220 005020 .WORD R06ERR
9499 024222 CKLOOP
9500 024222 104406 TRAP C$CLP1

```

```

9501
9502
9503
9504
9505
9506 024224 052737 000001 002334 10$: BIS #VDALO,R4LOAD ;SETUP BIT TO BE LOADED
9507 024232 004737 006640 JSR PC,LDRDR4 ;GO LOAD, READ AND CHECK VDAL REGISTER
9508 024236 001405 BEQ 11$ ;IF LOADED OK THEN CONTINUE
9509 024240 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
9510 024240 104455 TRAP C$ERDF
9511 024242 000003 .WORD 3
9512 024244 002537 .WORD VDALRG
9513 024246 005004 .WORD R4EROR
9514 024250 CKLOOP
9515 024250 104406 TRAP C$CLP1
9516
9517
9518 ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9519 024252 004737 006754 11$: JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL BITS 2:0
9520
9521 ;SET THE SIGNALS PPI L AND XPI L TO THE LOW STATE BY SETTING HDAL
9522 ;REGISTER BIT 15 TO A ONE IN THE HDAL REGISTER. WHEN PPI L IS ASSERTED
9523 ;LOW THE SIGNALS ABT H AND ABT L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY.
9524 ;THESE TWO SIGNALS WILL ENABLE THE TAI BUS, WHICH CONTAINS THE TAI
9525 ;DIAGNOSTIC LATCH DATA, ONTO THE CAI BUS. THE CAI BUS WILL BE ENABLED
9526 ;TO THE EIAI BUS. THE EIAI BUS WILL BE ENABLED TO THE CTL BUS VIA THE
9527 ;SIGNAL ADAL10 H BEING SET TO A ONE.
9528
9529 024256 012737 000004 002342 MOV #HDAL2,R6LOAD ;SETUP BIT PREVIOUSLY LOADED
9530 024264 004737 007514 JSR PC,XPIH ;SET PPI L AND XPI L TO LOW STATE
9531
9532 ;TO CLOCK THE CTL BUS DATA, WHICH CONTAINS THE TAI DIAGNOSTIC LATCH
9533 ;DATA, INTO THE CTL REGISTER, THE TEST WILL PULSE THE SIGNAL XCAS L
9534 ;BY SETTING AND CLEARING THE SIGNAL HDAL13 H.
9535
9536 024270 004737 007376 JSR PC,XCAS ;GO PULSE XCAS L VIA HDAL13 H
9537
9538 ;SET THE SIGNALS PPI L AND XPI L TO THE HIGH STATE BY CLEARING HDAL15 H.
9539 ;WHEN PPI L AND XPI L ARE ASSERTED HIGH, THE TAI BUS WILL BE DISABLED
9540 ;FROM THE CAI BUS.
9541
9542 024274 004737 007546 JSR PC,XPIL ;SET PPI L AND XPI L TO HIGH STATE
9543

```



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9544
9545
9546
9547 024300 004737 007154
9548
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9553 024304 010137 002342
9554 024310 005137 002342
9555 024314 042737 000377 002342
9556 024322 004737 006700
9557 024326 001404
9558 024330
9559 024330 104455
9560 024332 000004
9561 024334 003232
9562 024336 005034
9563 024340
9564 024340
9565 024340 104405
9566
9567 024342 062701 000400
9568 024346 001402
9569 024350 000137 023542
9570 024354
9571 024354
9572 024354 104401

```

```

;SELECT THE FDAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
JSR PC,SLFDAL ;SELECT FDAL REGISTER VIA GDAL BITS 2:0
;READ THE CTL AND FDAL REGISTER TO CHECK THAT XCAS L CLOCKED THE CTL
;BUS WHICH CONTAINED THE TAI DIAGNOSTIC LATCH DATA INTO THE CTL
;REGISTER.
MOV R1,R6LOAD ;GET THE FIRST EOAI DATA PATTERN
COM R6LOAD ;SETUP 1'S COMPLEMENT FOR READJACK
BIC #377,R6LOAD ;SETUP FDAL BITS TO BE ZERO
JSR PC,READR6 ;GO READ CTL AND FDAL REGISTERS
BEQ 12$ ;IF DATA OK THEN CONTINUE
ERRDF 4,CTLFDL,R026ER ;TAI LATCH TO CTL REGISTER ERROR
TRAP C$ERDF
.WORD 4
.WORD CTLFDL
.WORD R026ER
12$:
10000$:
ENDSEG
TRAP C$ESFG
ADD #BIT8,R1 ;UPDATE THE TEST PATTERN BY ONE
BEQ 13$ ;IF DONE THEN EXIT
JMP 1$ ;GO DO NEXT TEST PATTERN
13$:
L10066:
ENDTST
TRAP C$ETST

```

TEST 37: MODE REG TO ADDRESS BUS VIA EODAL, CDAL AND EIDAL BUS

.SBTTL TEST 37: MODE REG TO ADDRESS BUS VIA EODAL, CDAL AND EIDAL BUS

```

:++
: THIS TEST WILL CHECK THE DATA PATH FROM THE MODE REGISTER TO THE ADDRESS BUS.
: TO DO THIS, THE TEST WILL ENABLE THE DATA PATH FROM THE MODE REGISTER TO THE
: EODAL BUS, TO THE CDAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS. THIS IS
: DONE BY SETTING XBCLR H AND PBCLR H TO THE HIGH STATE AND BY SETTING ADAL12 H
: AND ADAL10 H TO ONES. THE TARGET MODE READBACK REGISTER WILL ALSO BE CHECKED
: TO HAVE BEEN LOADED WITH THE EIDAL BUS DATA WHEN THE SIGNAL XBCLR L IS SET TO
: THE HIGH STATE FROM THE LOW STATE. THE MODE REGISTER WILL BE LOADED WITH THE
: FOLLOWING DATA PATTERNS, 146063, 031714, 125252, 052525, 177777 AND 000000.
: FOR EACH DATA PATTERN LOADED, THE PROGRAM WILL CHECK THE DATA TO BE PRESENT ON
: THE THE EODAL BUS, THE EIDAL BUS, AND THE ADDRESS BUS. THE TEST WILL ALSO
: CHECK THAT EACH PATTERN CAN BE LOADED INTO THE TARGET MODE READBACK REGISTER.
:--
  
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024356
024356
024356 004737 005510
024362 012701 024670
024366 012702 000006
024372
024372 104404
024374 005037 002334
024400 004737 007712
024404 004737 006754
024410 012737 000004 002342
024416 004737 007620
024422 012737 012000 002330
024430 004737 006614
  
```

```

T37::      BGNTST
           JSR      PC,INITTE      ;SELECT AND INITIALIZE TARGET EMULATOR
           MOV      #8$,R1        ;SETUP DATA TABLE POINTER
           MOV      #6,R2         ;SETUP DATA PATTERN COUNTER

1$:        BGNSEG
           TRAP     C$BSEG

           ;SET VDAL2 H TO A ONE AND THEN ZERO TO PULSE THE SIGNALS INV D L AND
           ;INV D H. THESE SIGNALS WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS.

           CLR      R4LOAD        ;SETUP TO CLEAR ALL VDAL REG BITS
           JSR      PC,CLRPSM     ;GO PULSE INV D L VIA VDAL2 H

           ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

           JSR      PC,SLHDAL     ;SELECT HDAL REG VIA GDAL BITS 2:0

           ;SET HDAL2 H AND HDAL7 H TO ONES IN THE HDAL REGISTER. ALL OTHER HDAL
           ;BITS WILL BE SET TO ZEROES. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM
           ;TO MANIPULATE THE T-11 TIMING AND CONTROL SIGNALS. HDAL7 H ON A ONE
           ;WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED HIGH. HDAL9 H
           ;ON A ZERO WILL ENABLE THE EIDAL BUS TO THE ADDRESS BUS WHEN ADAL10 H IS
           ;SET TO A ONE.

           MOV      #HDAL2,R6LOAD ;SETUP DIAGNOSTIC CONTROL BIT
           JSR      PC,XBCLRH     ;SET XBCLR H AND PBCLR H TO HIGH STATE

           ;SET ADAL12 H AND ADAL10 H TO ONES IN THE ADAL REGISTER. ADAL12 H BEING
           ;SET HIGH WITH XBCLR H ASSERTED HIGH WILL ENABLE THE MODE REGISTER DATA
           ;TO THE EODAL BUS. ADAL12 H BEING SET HIGH WITH PBCLR H ASSERTED HIGH
           ;WILL CAUSE THE SIGNALS COMB L AND COLB L TO BE ASSERTED LOW. THESE
           ;TWO SIGNALS WILL ENABLE THE EODAL BUS TO THE CDAL BUS. THE CDAL BUS
           ;WILL BE ENABLED TO THE EIDAL BUS UNCONDITIONALLY. ADAL10 H BEING SET
           ;TO A ONE WITH HDAL9 H BEING SET TO A ZERO WILL ENABLE THE EIDAL BUS TO
           ;THE ADDRESS BUS.

           MOV      #ADAL12!ADAL10,R2LOAD ;SETUP BITS TO BE LOADED
           JSR      PC,LDRDR2    ;GO LOAD, READ AND CHECK ADAL REGISTER
  
```

TEST 37: MODE REG TO ADDRESS BUS VIA EODAL, CDAL AND EIDAL BUS

```

9629 024434 001405      BEQ      2$                ;IF LOADED OK THEN CONTINUE
9630 024436              ERRDF    2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
9631 024436 104455      TRAP    C$ERDF
9632 024440 000002      .WORD   2
9633 024442 002513      .WORD   ADALRG
9634 024444 004770      .WORD   R2EROR
9635 024446              CKLOOP
9636 024446 104406      TRAP    C$CLP1
9637
9638              ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9639
9640 024450 004737 007006      2$:    JSR      PC,SLMODR                ;SELECT MODE REG VIA GDAL BITS 2:0
9641
9642              ;LOAD, READ AND CHECK MODE REGISTER WITH DATA PATTERN FROM DATA TABLE.
9643
9644 024454 011137 002342      MOV     (R1),R6LOAD        ;GET THE DATA FROM THE DATA TABLE
9645 024460 004737 006672      JSR     PC,LDRDR6         ;GO LOAD, READ AND CHECK MODE REGISTER
9646 024464 001405      BEQ     3$                ;IF LOADED OK THEN CONTINUE
9647 024466              ERRDF    4,MODREG,R06ERR    ;MODE REGISTER NOT EQUAL EXPECTED
9648 024466 104455      TRAP    C$ERDF
9649 024470 000004      .WORD   4
9650 024472 002631      .WORD   MODREG
9651 024474 005020      .WORD   R06ERR
9652 024476              CKLOOP
9653 024476 104406      TRAP    C$CLP1
9654
9655              ;SELECT EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9656
9657 024500 004737 007122      3$:    JSR     PC,SEODAL                ;SELECT EODAL BUS VIA GDAL BITS 2:0
9658
9659              ;THE MODE REGISTER IS ENABLED TO THE EODAL BUS WHEN XBCLR H IS
9660              ;ASSERTED HIGH AND ADAL12 H IS SET TO A ONE. READ AND CHECK THE EODAL
9661              ;BUS TO CONTAIN THE DATA LOADED INTO THE MODE REGISTER.
9662
9663 024504 011137 002342      MOV     (R1),R6LOAD        ;GET THE MODE REGISTER DATA
9664 024510 004737 006700      JSR     PC,READR6         ;READ AND CHECK EODAL BUS TO = MODE REG
9665 024514 001405      BEQ     4$                ;IF DATA = MODE REG THEN CONTINUE
9666 024516              ERRDF    4,MEODAL,R026ER    ;MODE REG TO EODAL BUS ERROR
9667 024516 104455      TRAP    C$ERDF
9668 024520 000004      .WORD   4
9669 024522 003102      .WORD   MEODAL
9670 024524 005034      .WORD   R026ER
9671 024526              CKLOOP
9672 024526 104406      TRAP    C$CLP1
9673
9674              ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9675
9676 024530 004737 007240      4$:    JSR     PC,SEIDAL                ;SELECT EIDAL BUS VIA GDAL BITS 2:0
9677
9678              ;AT THIS POINT IN TIME, THE MODE REGISTER IS ENABLED TO THE EODAL BUS
9679              ;VIA XBCLR H AND ADAL12 H. THE EODAL BUS IS ENABLED TO THE CDAL BUS
9680              ;VIA THE SIGNALS COHB L AND COLB L. THE SIGNALS COHB L AND COLB L ARE
9681              ;ASSERTED LOW AS A RESULT OF PBCLR H BEING ASSERTED HIGH AND ADAL12 H
9682              ;BEING SET TO A ONE. THE CDAL BUS IS ENABLED TO THE EIDAL BUS UNCON-
9683              ;DITIONALLY. READ AND CHECK THE EIDAL BUS TO CONTAIN THE MODE REGISTER
9684              ;DATA.

```

9685					
9686	024534	011137	002342		
9687	024540	004737	006700		
9688	024544	001405			
9689	024546				
9690	024546	104455			
9691	024550	000004			
9692	024552	003270			
9693	024554	005034			
9694	024556				
9695	024556	104406			
9696					
9697					
9698					
9699	024560	004737	007072	5\$:	
9700					
9701					
9702					
9703					
9704					
9705	024564	011137	002342		
9706	024570	004737	006700		
9707	024574	001405			
9708	024576				
9709	024576	104455			
9710	024600	000004			
9711	024602	003377			
9712	024604	005034			
9713	024606				
9714	024606	104406			
9715					
9716					
9717					
9718	024610	004737	006754	6\$:	
9719					
9720					
9721					
9722					
9723					
9724					
9725					
9726	024614	012737	000204	002342	
9727	024622	004737	007652		
9728					
9729					
9730					
9731	024626	004737	007206		
9732					
9733					
9734					
9735					
9736					
9737					
9738					
9739					
9740	024632	011137	002342		

```

MOV (R1),R6LOAD ;GET THE MODE REGISTER DATA LOADED
JSR PC,READR6 ;CHECK EIDAL BUS TO = MODE REG DATA
BEQ 5$ ;IF DATA = MODE REG DATA THEN CONT
ERRDF 4,MEIDAL,R026ER ;MODE REG TO EIDAL BUS ERROR
TRAP C$ERDF
.WORD 4
.WORD MEIDAL
.WORD R026ER
CKLOOP
TRAP C$CLP1

```

:SELECT THE ADDRESS BUS VIA THE GDAL BITS 2:0 IN CONTROL REGISTER 0

```

5$: JSR PC,SLDADR ;SELECT ADDRESS BUS VIA GDAL BITS 2:0

```

:THE EIDAL BUS WILL BE ENABLED TO THE ADDRESS BUS AT THIS TIME AS A
 :RESULT OF HDAL9 H BEING A ZERO AND ADAL10 H BEING A ONE. THE EIDAL
 :BUS PRESENTLY CONTAINS THE MODE REGISTER DATA.

```

MOV (R1),R6LOAD ;GET THE MODE REGISTER DATA
JSR PC,READR6 ;CHECK ADDRESS BUS TO = MODE REG DATA
BEQ 6$ ;IF ADDRESS BUS = MODE REG DATA THEN CONT
ERRDF 4,MADDRS,R026ER ;MODE REG TO ADDRESS BUS ERROR
TRAP C$ERDF
.WORD 4
.WORD MADDRS
.WORD R026ER
CKLOOP
TRAP C$CLP1

```

:SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

```

6$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

```

:SET THE SIGNAL XBCLR L, WHICH IS PRESENTLY ASSERTED LOW, TO THE HIGH
 :STATE BY CLEARING HDAL7 H IN THE HDAL REGISTER. SETTING XBCLR L TO THE
 :HIGH STATE WILL CLOCK THE EIDAL BUS, WHICH CONTAINS MODE REGISTER DATA,
 :INTO THE TARGET MODE READBACK REGISTER. SETTING XBCLR H TO THE LOW
 :STATE WILL DISABLE THE MODE REGISTER DATA FROM THE EODAL BUS.

```

MOV #HDAL7!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
JSR PC,XBCLRL ;SET XBCLR H TO THE LOW STATE

```

:SELECT THE TARGET MODE READBACK REGISTER VIA GDAL BITS 2:0

```

JSR PC,SELTMR ;SELECT TARGET MODE READBACK REG VIA GDAL BITS 2

```

:READ AND CHECK THE TARGET MODE READBACK REGISTER TO CHECK THAT THE
 :EIDAL BUS DATA WAS CLOCKED INTO IT WHEN THE SIGNAL XBCLR L WAS SET TO
 :THE HIGH STATE. THE EIDAL BUS CONTAINED THE MODE REGISTER DATA AT THE
 :TIME THE SIGNAL XBCLR L WAS SET HIGH. THE TARGET MODE READBACK REGIS-
 :TER WILL BE READBACK TO THE LSI-17 VIA THE SIGNAL RPT5 L WHEN A READ
 :COMMAND IS ISSUED TO CONTROL REGISTER 6.

```

MOV (R1),R6LOAD ;GET THE MODE REGISTER DATA

```

TEST 37: MODE REG TO ADDRESS BUS VIA EODAL, CDAL AND EIDAL BUS

9741	024636	004737	006700	JSR	PC,READR6		
9742	024642	001404		BEQ	7\$;CHECK TMR TO = MODE REG DATA
9743	024644			ERRDF	4,MTOTMR,R026ER		;IF DATA = MODE REG THEN CONTINUE
9744	024644	104455		TRAP	C\$ERDF		;MODE REGISTER TO TARGET MODE REG ERROR
9745	024646	000004		.WORD	4		
9746	024650	003335		.WORD	MTOTMR		
9747	024652	005034		.WORD	R026ER		
9748	024654			7\$:	ENDSEG		
9749	024654			10000\$:			
9750	024654	104405		TRAP	C\$ESEG		
9751							
9752	024656	005721		TST	(R1)+		;UPDATE DATA TABLE POINTER
9753	024660	005302		DEC	R2		;DECREMENT DATA TABLE COUNTER
9754	024662	001410		BEQ	9\$;IF 0 THEN ALL PATTERNS DONE
9755	024664	000137	024372	JMP	1\$;GO DO NEXT PATTERN
9756							
9757	024670	146063		8\$:	.WORD	146063	
9758	024672	031714			.WORD	031714	
9759	024674	125252			.WORD	125252	
9760	024676	052525			.WORD	052525	
9761	024700	177777			.WORD	177777	
9762	024702	000000			.WORD	000000	
9763							
9764	024704			9\$:	ENDTST		
9765	024704			L10067:			
9766	024704	104401		TRAP	C\$ETST		
9767							

TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSSES

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024706
 024706
 024706 004737 005510
 024712 012701 026114
 024716 012702 000006
 024722
 024722 104404
 024724 005037 002346
 024730 004737 007006
 024734 005037 002342
 024740 004737 006672
 024744 001405
 024746 104455
 024750 000004
 024752 002631
 024754 005020
 024756 104406
 024760 004737 006754
 024764 012737 001004 002342
 024772 004737 006672

.SBTTL TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSSES

```

:++
: THIS TEST WILL CHECK THE DATA PATH FROM THE DIAGNOSTIC ADDRESS REGISTER TO THE
: OLD FORCE JUMP ADDRESS REGISTER, TO THE EODAL BUS, TO THE EIDAL BUS, AND TO
: THE ADDRESS BUS. THIS PART OF THE TEST USES THE PAUSE STATE MACHINE LOGIC TO
: LOAD THE OLD FORCE JUMP ADDRESS REGISTER AND TO PLACE THE OLD FORCE JUMP
: ADDRESS REGISTER DATA ONTO THE EODAL BUS. WHEN THE OLD FORCE JUMP ADDRESS
: REGISTER DATA IS ENABLED TO THE EODAL BUS, THE TEST WILL ENABLE THE DATA TO
: THE TDAL BUS AND LATCH THE DATA INTO THE TDAL DIAGNOSTIC LATCHES. THE NEXT
: PART OF THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC LATCHES CAN BE ENABLED
: TO THE EIDAL BUS AND THAT THE EIDAL BUS CAN BE ENABLED TO THE EODAL BUS THROUGH
: THE DATA BUS.
:--
  
```

T38:: BGNTST

```

JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
MOV #238,R1 ;GET ADDRESS OF DATA TABLE
MOV #6,R2 ;COUNTER FOR NUMBER OF DATA PATTERNS
  
```

1\$: BGNSEG

```

TRAP C$BSEG
CLR R6MASK ;CLEAR MASK FOR REG 6

;SELECT THE MODE REG BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDALO TO A ZERO.
JSR PC,SLMODR ;GO SELECT MODE REG VIA CONTROL REG 0

;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH ZEROES. MR BIT 11
;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE
  
```

```

CLR R6LOAD ;SETUP DATA TO BE ZERO
JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO 0
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C$CLP1
  
```

```

;SET GDAL1 AND GDALO TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 5.
  
```

2\$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0

```

;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
;BUS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
;TIMING AND CONTROL SIGNALS.
  
```

```

MOV #HDAL9!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
  
```

TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSES

```

9824 024776 001405      BEQ      3$                ;IF LOADED OK THEN CONTINUE
9825 025000              ERRDF    4,HDALRG,R06ERR  ;HDAL REGISTER NOT EQUAL EXPECTED
9826 025000 104455      TRAP    C$ERDF
9827 025002 000004      .WORD   4
9828 025004 002605      .WORD   HDALRG
9829 025006 005020      .WORD   R06ERR
9830 025010              CKLOOP
9831 025010 104406      TRAP    C$CLP1
9832
9833                    ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
9834                    ;ZEROS. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
9835                    ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
9836
9837 025012 004737 007072 3$: JSR      PC,SLDADR          ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0
9838
9839                    ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
9840                    ;FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, + 000000.
9841
9842 025016 011137 002342  MOV     (R1),R6LOAD        ;GET DATA PATTERN FROM TABLE
9843 025022 004737 006672  JSR     PC,LDRDR6         ;GO LOAD READ AND CHECK DIAG ADDRESS REG
9844 025026 001405      BEQ     4$                ;IF LOADED OK THEN CONTINUE
9845 025030              ERRDF    4,ADDRRG,R06ERR  ;DIAG ADDRESS REG NOT EQUAL EXPECTED
9846 025030 104455      TRAP    C$ERDF
9847 025032 000004      .WORD   4
9848 025034 002735      .WORD   ADDR RG
9849 025036 005020      .WORD   R06ERR
9850 025040              CKLOOP
9851 025040 104406      TRAP    C$CLP1
9852
9853                    ;SET ADAL13 H, ADAL10 H AND ADALO H TO 1'S AND ALL OTHER ADAL BITS TO 0.
9854                    ;ADALO ON A ONE WILL HOLD THE BREAK LOGIC CLEARED. ADAL4 ON A ZERO
9855                    ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
9856                    ;WHEN THE SIGNAL XRAS H IS PULSED. ADAL10 H ON A ONE WILL ENABLE THE
9857                    ;EIDAL BUS TO THE ADDRESS BUS WHEN HDAL9 H IS SET TO A 0 LATER ON IN THE TEST.
9858
9859 025042 012737 022001 002330 4$: MOV     #ADAL13!ADAL10!ADALO,R2LOAD ;SETUP BITS TO BE LOADED
9860 025050 004737 006614  JSR     PC,LDRDR2         ;GO LOAD, READ AND CHECK ADAL REG
9861 025054 001405      BEQ     5$                ;IF LOADED OK THEN CONTINUE
9862 025056              ERRDF    2,ADALRG,R2EROR  ;ADAL REGISTER NOT EQUAL 1
9863 025056 104455      TRAP    C$ERDF
9864 025060 000002      .WORD   2
9865 025062 002513      .WORD   ADALRG
9866 025064 004770      .WORD   R2EROR
9867 025066              CKLOOP
9868 025066 104406      TRAP    C$CLP1
9869
9870                    ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
9871                    ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
9872
9873 025070 005037 002334 5$: CLR     R4LOAD            ;SETUP TO CLEAR ALL BITS IN VDAL REG
9874 025074 004737 007712  JSR     PC,CLRPSM        ;GO SET AND CLEAR VDAL2 H
9875
9876                    ;SET VDAL7 H TO A ONE IN THE VDAL REGISTER TO SET THE SIGNAL FETCT H
9877                    ;TO THE HIGH STATE.
9878
9879 025100 052737 000200 002334  BIS     #VDAL7,R4LOAD    ;SETUP BIT TO BE LOADED
  
```



```

9936                                     : 16 BIT ADDRESS - EPFN H - 0
9937
9938 025144 042737 000200 002334      BIC   #VDAL7,R4LOAD      :SETUP TO CLEAR FETCT H
9939 025152 013737 002334 002336      MOV   R4LOAD,R4GOOD     :COPY DATA LOADED TO EXPECTED
9940 025160 052737 001040 002336      BIS   #VDAL9!VDAL5,R4GOOD :EXPECT PSMW H AND BTS1 H TO BE SET
9941 025166 004737 006646              JSR   PC,LDRD4R         :GO LOAD, READ AND CHECK VDAL REG
9942 025172 001405                      BEQ   7$               :IF LOADED OK THEN CONTINUE
9943 025174                                ERRDF 3,VDALRG,R4EROR   :VDAL OR PAUSE STATE MACHINE ERROR
9944 025174 104455                      TRAP  C$ERDF
9945 025176 000003                      .WORD 3
9946 025200 002537                      .WORD VDALRG
9947 025202 005004                      .WORD R4EROR
9948 025204                                CKLOOP
9949 025204 104406                      TRAP  C$CLP1
9950
9951                                     :TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H. THE
9952                                     :SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
9953                                     :SIGNAL 'PB H', WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
9954                                     :SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE. THE SIGNAL XCAS H
9955                                     :WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-FLOP (0)
9956                                     :INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE 16 BIT ADDRESS
9957                                     :FLIP-FLOP TO A ZERO.
9958
9959                                     :
9960                                     :WHEN A PULSE IS ISSUED ON XCAS H AND XRAS L IS ASSERTED HIGH, A PULSE
9961                                     :WILL OCCUR ON THE SIGNAL ASPI L. WHEN A PULSE IS ISSUED ON ASPI L,
9962                                     :THE BTJET FLIP-FLOP WILL BE CLEARED, THUS SETTING THE SIGNAL BTJET L
9963                                     :TO THE HIGH STATE. WHEN BTJET L AND INTER L ARE ASSERTED HIGH, THE
9964                                     :SIGNAL BTS1 H WILL BE ASSERTED LOW.
9965 025206 004737 007376      7$:   JSR   PC,XCAS          :SET XCAS H TO THE HIGH STATE
9966
9967                                     :
9968                                     :READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
9969                                     :IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET TO 1.
9970                                     :ALSO CHECK VDALS H TO BE A ZERO AS A RESULT OF BTS1 H BEING ASSERTED
9971                                     :LOW AND ADAL10 H BEING SET TO A ONE.
9972                                     :
9973                                     :   PAUSE STATE WORKING - PSMW H - 1
9974                                     :   PAUSE STATE SYNC - EPSF H - 1
9975                                     :   16 BIT ADDRESS - EPFN H - 0
9976
9975 025212 052737 002000 002336      BIS   #VDAL10,R4GOOD    :SETUP TO EXPECT PAUSE STATE SYNC - EPSF
9976 025220 042737 000040 002336      BIC   #VDALS,R4GOOD     :EXPECT BTS1 H TO BE A ZERO FROM ASPI L
9977 025226 004737 006654              JSR   PC,READR4         :GO READ AND CHECK PAUSE STATE MACHINE
9978 025232 001405                      BEQ   8$               :IF LOADED OK THEN CONTINUE
9979 025234                                ERRDF 3,VDALRG,R4EROR   :EPSF H NOT SET/BTS1 H NOT LOW VIA ASPI L
9980 025234 104455                      TRAP  C$ERDF
9981 025236 000003                      .WORD 3
9982 025240 002537                      .WORD VDALRG
9983 025242 005004                      .WORD R4EROR
9984 025244                                CKLOOP
9985 025244 104406                      TRAP  C$CLP1
9986
9987                                     :
9988                                     :TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
9989                                     :THIS IS DONE TO SIMULATE A MACHINE CYCLE. WHEN THE SIGNAL XPI H IS
9990                                     :PULSED, THE EDFET H FLIP-FLOP WILL BE SET TO A ZERO.
9991 025246 004737 007502      8$:   JSR   PC,XPI          :GO PULSE XPI H VIA HDAL15 H

```

```

9992
9993
9994
9995
9996
9997
9998
9999
10000
10001
10002 025252 004737 007272
10003
10004
10005
10006
10007
10008
10009
10010 025256 004737 006654
10011 025262 001405
10012 025264
10013 025264 104455
10014 025266 000003
10015 025270 002537
10016 025272 005004
10017 025274
10018 025274 104406
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10028 025276 004737 007410 98:
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10036 025302 042737 002000 002336
10037 025310 052737 004000 002336
10038 025316 004737 006654
10039 025322 001405
10040 025324
10041 025324 104455
10042 025326 000003
10043 025330 002537
10044 025332 005004
10045 025334
10046 025334 104406
10047

;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
;EDFET H TO THE LOW STATE. WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
;PB H WILL BE ASSERTED LOW. WHEN XRAS H IS PULSED, THE SIGNALS RASP H
;AND RASP L WILL BE PULSED.
;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

JSR PC,XRAS ;GO PULSE XRAS H BY HDAL12

;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
: PAUSE STATE WORKING - PSMW H - 1
: PAUSE STATE SYNC - EPSF H - 1
: 16 BIT ADDRESS - EPFN H - 0

JSR PC,READR4 ;CHECK VDAL AND PAUSE STATE MACHINE
BEQ 98 ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;PAUSE STATE WORKING F/F PROBABLY NOT SET
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1

;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
;SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
;SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
;THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO. THE SIGNAL
;XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
;FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE
;16 BIT ADDRESS FLIP-FLOP TO A ONE.

JSR PC,XCASH ;SET THE SIGNAL XCAS H TO HIGH STATE

;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
: PAUSE STATE WORKING - PSMW H - 1
: PAUSE STATE SYNC - EPSF H - 0
: 16 BIT ADDRESS - EPFN H - 1

BIC #VDAL10,R4GOOD ;CLEAR BITS FOR EPSF H
BIS #VDAL11,R4GOOD ;SET BIT FOR EPFN H
JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
BEQ 108 ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;EPFN H PROBABLY NOT SET IN VDAL REG
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1

```

```

10048 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES. THE OLD FORCE
10049 ;JUMP ADDRESS REGISTER SHOULD BE ENABLED ON THE EODAL BUS AT THIS TIME.
10050 ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ
10051 ;BACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
10052
10053 025336 004737 007122 10$: JSR PC,SEODAL ;SELECT EODAL BUS VIA GDAL BITS 2:0
10054
10055 ;ON THE FIRST PULSE OF XRAS H WHEN THE SIGNAL EDFET H WAS SET HIGH,
10056 ;THE FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED WITH THE DATA
10057 ;IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE CLOCKING SIGNAL DFET H
10058 ;(ADDRESS BUS TO FORCE JUMP ADDRESS REGISTER). AT THIS POINT IN TIME,
10059 ;THE FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS VIA
10060 ;THE SIGNALS OEARH L AND OEARL L. THESE SIGNALS ARE ASSERTED LOW AS A
10061 ;RESULT OF THE FLIP-FLOP 'GET NEW ADDRESS' BEING CLEARED AND THE
10062 ;SIGNALS EARH H AND EARL H BEING ASSERTED HIGH. THE 'GET NEW ADDRESS'
10063 ;FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THE TEST WHEN VDAL REGISTER
10064 ;BIT 2 WAS SET AND CLEARED. THE SIGNAL EARH H AND EARL H ARE ASSERTED
10065 ;HIGH AS A RESULT OF THE 16 BIT ADDRESS FLIP-FLOP BEING SET TO A ONE,
10066 ;THE SIGNAL ACAS H BEING ASSERTED HIGH, AND MODE REGISTER BIT 11 SETUP
10067 ;FOR 16 BIT ADDRESS MODE. THE FOLLOWING SECTION WILL READ THE EODAL
10068 ;BUS VIA THE SIGNAL RPT7 L AND CHECK THAT THE DIAGNOSTIC ADDRESS
10069 ;REGISTER WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER AND THAT
10070 ;THE OLD FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS.
10071
10072 025342 011137 002342 MOV (R1),R6LOAD ;GET DATA LOADED INTO DIAG ADDRESS REG
10073 025346 004737 006700 JSR PC,READR6 ;READ FORCE JUMP ADDRESS ON EODAL BUS
10074 025352 001405 BEQ 11$ ;IF FORCE JUMP ADDRESS REG OK THEN CONT
10075 025354 ERRDF 4,FEODAL,R06ERR ;FORCE JUMP ADDRESS REG TO EODAL BUS ERR
10076 025354 104455 TRAP C$ERRDF
10077 025356 000004 .WORD 4
10078 025360 003147 .WORD FEODAL
10079 025362 005020 .WORD R06ERR
10080 025364 CKLOOP
10081 025364 104406 TRAP C$CLP1
10082
10083 ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10084
10085 025366 004737 006754 11$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10086
10087 ;LEAVING THE SIGNAL XCAS H ASSERTED HIGH, ASSERT THE SIGNAL PPI H TO THE
10088 ;HIGH STATE BY SETTING HDAL15 H TO A ONE. SETTING THE SIGNAL PPI H TO
10089 ;THE HIGH STATE WILL CAUSE THE SIGNALS COMB L AND COLB L TO BE ASSERTED
10090 ;LOW. SET HDAL9 H TO A ZERO. WHEN HDAL9 H IS A ZERO AND ADAL10 H IS A
10091 ;ONE, WHICH IT IS, THE EIDAL BUS WILL BE ENABLED TO THE ADDRESS BUS AND
10092 ;THE DIAGNOSTIC ADDRESS REGISTER WILL BE DISABLED FROM THE ADDRESS BUS.
10093
10094 025372 012737 020004 002342 MOV #HDAL13!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED (XCAS H)
10095 025400 004737 007514 JSR PC,XPIH ;SET XPI H AND PPI H TO HIGH STATE
10096
10097 ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10098
10099 025404 004737 007240 JSR PC,SEIDAL ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10100
10101 ;AT THIS POINT IN TIME, THE EODAL BUS, WHICH CONTAINS THE OLD FORCE
10102 ;JUMP ADDRESS REGISTER DATA, WILL BE ENABLED TO THE EIDAL BUS VIA THE
10103 ;SIGNAL COMB L AND COLB L. THE SIGNALS COMB L AND COLB L ARE ASSERTED

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10104 ;LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING SET, MODE
10105 ;REGISTER BIT 11 BEING A ZERO AND PPI H BEING ASSERTED HIGH. THE
10106 ;PROGRAM WILL READ AND CHECK THE EIDAL BUS TO CONTAIN THE OLD FORCE
10107 ;JUMP ADDRESS REGISTER DATA.
10108
10109 025410 011137 002342 MOV (R1),R6LOAD ;GET OLD FJA REGISTER DATA
10110 025414 004737 006700 JSR PC,READR6 ;READ EIDAL BUS FOR OLD FJA DATA
10111 025420 001405 BEQ 12$ ;IF DATA OK THEN CONTINUE
10112 025422 ERRDF 4,FJAEID,R026ER ;OLD FJA TO EIDAL BUS ERROR VIA EODAL
10113 025422 104455 TRAP C$ERDF
10114 025424 000004 .WORD 4
10115 025426 003446 .WORD FJAEID
10116 025430 005034 .WORD R026ER
10117 025432 CKLOOP
10118 025432 104406 TRAP C$CLP1
10119
10120 ;SELECT THE ADDRESS BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10121
10122 025434 004737 007072 12$: JSR PC,SLDADR ;SELECT ADDRESS BUS VIA GDAL BITS 2:0
10123
10124 ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD BE ENABLED TO THE ADDRESS
10125 ;BUS BY ADAL10 H BEING A ONE AND HDAL9 H BEING A ZERO. THE EIDAL BUS
10126 ;PRESENTLY CONTAINS THE OLD FORCE JUMP ADDRESS REGISTER DATA.
10127
10128 025440 011137 002342 MOV (R1),R6LOAD ;GET DATA LOADED INTO OLD FJA REGISTER
10129 025444 004737 006700 JSR PC,READR6 ;READ AND CHECK ADDRESS BUS FOR OLD FJA
10130 025450 001405 BEQ 13$ ;IF DATA OK THEN CONTINUE
10131 025452 ERRDF 4,FJAADR,R026ER ;FORCE JUMP ADDRESS TO ADDRESS BUS ERROR
10132 025452 104455 TRAP C$ERDF
10133 025454 000004 .WORD 4
10134 025456 003501 .WORD FJAADR
10135 025460 005034 .WORD R026ER
10136 025462 CKLOOP
10137 025462 104406 TRAP C$CLP1
10138
10139 ;THE OLD FORCE JUMP ADDRESS REGISTER IS PRESENTLY ENABLED TO THE EODAL
10140 ;BUS, THE CDAL BUS, THE EIDAL BUS AND THE ADDRESS BUS. THE CDAL BUS IS
10141 ;ALSO ENABLED TO THE TDAL BUS VIA THE SIGNALS DTHB L AND DTLB L. THE
10142 ;SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF PSEL0 L,
10143 ;PSEL1 L, PBCLR L AND CPI L BEING ASSERTED HIGH AND THE SIGNAL CCAS H
10144 ;BEING ASSERTED LOW. TO CHECK THE DATA PATH TO THE TDAL BUS, THE TEST
10145 ;WILL CLOCK THE TDAL BUS INTO THE TDAL DIAGNOSTIC LATCH BY SETTING AND
10146 ;AND CLEARING VDAL2 H. BY SETTING AND CLEARING VDAL2 H, THE PAUSE
10147 ;STATE MACHINE FLIP-FLOPS WILL BE CLEARED AND THE TDAL BUS WILL BE
10148 ;LATCHED INTO THE TDAL DIAGNOSTIC LATCH.
10149
10150 025464 005037 002334 13$: CLR R4LOAD ;SETUP TO EXPECT ALL BITS CLEARED
10151 025470 004737 007712 JSR PC,CLRPSM ;PULSE INVD L AND INVD H VIA VDAL2 H
10152 ;CLOCK TDAL BUS INTO TDAL DIAG LATCH
10153
10154 ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10155
10156 025474 004737 006754 JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10157
10158 ;SET THE SIGNALS XCAS H AND PCAS H TO THE LOW STATE BY CLEARING HDAL13 H
10159

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10160 025500 012737 120004 002342      MOV      #HDAL15!HDAL13!HDAL2,R6LOAD ;SETUP PREVIOUSLY LOADED BITS
10161 025506 004737 007442                JSR      PC,XCASL                      ;SET XCAS H AND PCAS H TO LOW STATE
10162                                     ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL15 H.
10163
10164
10165 025512 004737 007546                JSR      PC,XPIL
10166
10167                                     ;SET THE SIGNAL PBCLR H TO THE HIGH STATE BY SETTING HDAL7 H TO A ONE.
10168                                     ;WHEN THE SIGNAL PBCLR H IS ASSERTED HIGH AND ADAL12 H IS A ZERO, THE
10169                                     ;TDAL BUS WILL BE ENABLED TO THE CDAL BUS VIA THE SIGNALS DBHB L AND
10170                                     ;DBLB L.
10171
10172 025516 004737 007620                JSR      PC,XBCLRH                      ;SET PBCLR H TO HIGH STATE VIA HDAL7 H
10173
10174                                     ;TO ENABLE THE TDAL DIAGNOSTIC LATCH ONTO THE TDAL BUS THE TEST WILL
10175                                     ;SET VDALO H TO A ONE. THE TDAL DIAGNOSTIC LATCH WAS LOADED WITH THE
10176                                     ;OLD FORCE JUMP ADDRESS REGISTER DATA EARLIER IN THIS TEST WHEN THE
10177                                     ;SIGNAL VDAL2 H WAS SET AND CLEARED.
10178
10179 025522 052737 000001 002334      BIS      #VDALO,R4LOAD                  ;SETUP BIT TO ENABLE TDAL LATCH
10180 025530 004737 006640                JSR      PC,LDRDR4                      ;GO LOAD, READ AND CHECK VDAL REGISTER
10181 025534 001405                        BEQ      14$                             ;IF LOADED OK THEN CONTINUE
10182 025536                                     ERRDF   3,VDALRG,R4EROR                ;VDAL OR PAUSE STATE MACHINE ERROR
10183 025536 104455                        TRAP    C$ERDF
10184 025540 000003                        .WORD   3
10185 025542 002537                        .WORD   VDALRG
10186 025544 005004                        .WORD   R4EROR
10187 025546                                     CKLOOP
10188 025546 104406                        TRAP    C$CLP1
10189
10190                                     ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10191
10192 025550 004737 007240                14$:   JSR      PC,SEIDAL                  ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10193
10194                                     ;AT THIS POINT IN TIME THE TDAL DIAGNOSTIC LATCH, WHICH WAS LOADED
10195                                     ;EARLIER IN THIS TEST VIA VDAL2 H, IS ENABLED TO THE TDAL BUS BY
10196                                     ;VDALO H BEING A ONE. THE TDAL BUS IS ENABLED TO THE CDAL BUS VIA
10197                                     ;THE SIGNALS DBHB L AND DBLB L. THESE SIGNALS ARE ASSERTED LOW AS A
10198                                     ;RESULT OF ADAL12 H BEING A ZERO AND THE SIGNAL PBCLR H BEING ASSERTED
10199                                     ;HIGH. READ AND CHECK THE EIDAL BUS TO CONTAIN THE DATA WHICH WAS
10200                                     ;LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER EARLIER IN THIS TEST.
10201
10202 025554 011137 002342      MOV      (R1),R6LOAD                    ;GET THE OLD FJA REGISTER DATA
10203 025560 004737 006700                JSR      PC,READR6                      ;READ EIDAL BUS FOR OLD FJA DATA
10204 025564 001405                        BEQ      15$                             ;IF DATA OK THEN CONTINUE
10205 025566                                     ERRDF   4,FJATDL,R026ER                ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10206 025566 104455                        TRAP    C$ERDF
10207 025570 000004                        .WORD   4
10208 025572 003536                        .WORD   FJATDL
10209 025574 005034                        .WORD   R026ER
10210 025576                                     CKLOOP
10211 025576 104406                        TRAP    C$CLP1
10212
10213                                     ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10214
10215 025600 004737 006754                15$:   JSR      PC,SLHDAL                  ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

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10216
10217 ;SET THE SIGNAL PBCLR H TO THE LOW STATE BY CLEARING HDAL7 H.
10218
10219 025604 012737 000204 002342 MOV #HDAL7!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
10220 025612 004737 007652 JSR PC,XBCLRL ;SET PBCLR H TO THE LOW STATE VIA HDAL7
10221
10222 ;SET THE SIGNALS PSELO H, PSEL1 H, AND MSDI H TO THE HIGH STATE BY
10223 ;SETTING HDAL6, HDAL5, AND HDALO TO ONES IN THE HDAL REGISTER. WHEN
10224 ;PSELO H AND PSEL1 H ARE ASSERTED HIGH, THE TDAL BUS WILL BE ENABLED TO
10225 ;THE CDAL BUS AGAIN VIA THE SIGNALS DBHB L AND DBLB L. THE CDAL BUS
10226 ;WILL BE ENABLED TO THE EIDAL BUS UNCONDITIONALLY. THE SIGNALS MSDI H
10227 ;AND MSDO H WILL BE ASSERTED HIGH AS A RESULT OF XSELO L BEING ASSERTED
10228 ;LOW AND HDALO H BEING ASSERTED HIGH. THESE TWO SIGNALS WILL ENABLE THE
10229 ;EIDAL BUS TO THE DATA BUS AND TO THE EODAL BUS.
10230
10231 025616 052737 000141 002342 BIS #HDAL6!HDAL5!HDALO,R6LOAD ;SET PSELO H,PSEL1 H,MSDO H + MSDI H TO HIGH S
10232 025624 004737 006672 JSR PC,LDRDR6 ;GO LOAD READ AND CHECK HDAL REGISTER
10233 025630 001405 BEQ 16$ ;IF LOADED OK THEN CONTINUE
10234 025632 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10235 025632 104455 TRAP C$ERDF
10236 025634 000004 .WORD 4
10237 025636 002605 .WORD HDALRG
10238 025640 005020 .WORD R06ERR
10239 025642 CKLOOP
10240 025642 104406 TRAP C$CLP1
10241
10242 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL MSDI H IS ASSERTED
10243 ;HIGH WHEN HDALO H IS SET TO A ONE. THE LOGIC LEVEL OF THE SIGNAL
10244 ;MSDI H IS READBACK INTO THE VDAL REGISTER AS VDAL REGISTER BIT 6.
10245
10246 025644 052737 000100 002336 16$: BIS #VDAL6,R4GOOD ;SETUP TO EXPECT MSDI H AS A ONE
10247 025652 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL AND PAUSE STATE
10248 025656 001405 BEQ 17$ ;IF MSDI H A ONE THEN CONTINUE
10249 025660 ERRDF 3,VDALRG,R4EROR ;VDAL REG ERROR - MSDI H PROBABLY A 0
10250 025660 104455 TRAP C$ERDF
10251 025662 000003 .WORD 3
10252 025664 002537 .WORD VDALRG
10253 025666 005004 .WORD R4EROR
10254 025670 CKLOOP
10255 025670 104406 TRAP C$CLP1
10256
10257 ;SELECT EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10258
10259 025672 004737 007240 17$: JSR PC,SEIDAL ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10260
10261 ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10262 ;BY VDALO H BEING A ONE. THE TDAL BUS IS ENABLED TO THE CDAL BUS VIA
10263 ;THE SIGNALS DBHB L AND DBLB L. THESE SIGNALS ARE ASSERTED LOW AS A
10264 ;RESULT OF THE SIGNALS PSELO H AND PSEL1 H BEING ASSERTED HIGH. THE
10265 ;CDAL BUS IS ENABLED TO THE EIDAL BUS UNCONDITIONALLY. THE TDAL
10266 ;DIAGNOSTIC LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD FORCE
10267 ;JUMP ADDRESS REGISTER DATA.
10268
10269 025676 011137 002342 MOV (R1),R6LOAD ;GET OLD FJA REGISTER DATA LOADED
10270 025702 004737 006700 JSR PC,READR6 ;READ EIDAL BUS FOR OLD FJA REG DATA
10271 025706 001405 BEQ 18$ ;IF DATA OK THEN CONTINUE

```

TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSES

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10272 025710          ERRDF  4,FJATDL,R026ER          ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10273 025710 104455  TRAP   C$ERDF
10274 025712 000004  .WORD  4
10275 025714 003536  .WORD  FJATDL
10276 025716 005034  .WORD  R026ER
10277 025720          CKLOOP
10278 025720 104406  TRAP   C$CLP1
10279
10280          ;SELECT THE EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10281
10282 025722 004737 007122 18$: JSR    PC,SEODAL          ;SELECT EODAL BUS VIA GDAL BITS 2:0
10283
10284          ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10285          ;BY VDALO H BEING SET TO A ONE. THE TDAL BUS IS ENABLED TO THE CDAL
10286          ;BUS VIA THE SIGNALS DBHB L AND DBLB L. THE CDAL BUS IS ENABLED TO THE
10287          ;EIDAL BUS UNCONDITIONALLY. THE EIDAL BUS IS ENABLED TO THE DATA BUS
10288          ;BY THE SIGNAL MSDO H. THE SIGNAL MSDO H IS ASSERTED HIGH AS A RESULT
10289          ;OF XSELO L BEING ASSERTED LOW. THE DATA BUS IS ENABLED TO THE EODAL
10290          ;BUS BY THE SIGNAL MSDI H BEING ASSERTED HIGH. THIS SIGNAL IS ASSERTED
10291          ;HIGH AS A RESULT OF HDALO H BEING SET TO A ONE. THE TDAL DIAGNOSTIC
10292          ;LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD FORCE JUMP ADDRESS
10293          ;REGISTER DATA.
10294
10295 025726 011137 002342  MOV    (R1),R6LOAD          ;GET OLD FJA REGISTER DATA LOADED
10296 025732 004737 006700  JSR    PC,READR6          ;READ EODAL BUS FROM DATA + EIDAL BUSES
10297 025736 001405  BEQ    19$                ;IF DATA OK THEN CONTINUE
10298 025740          ERRDF  4,TDLEOD,R026ER          ;EIDAL BUS TO DATA BUS TO EODAL BUS ERROR
10299 025740 104455  TRAP   C$ERDF
10300 025742 000004  .WORD  4
10301 025744 003607  .WORD  TDLEOD
10302 025746 005034  .WORD  R026ER
10303 025750          CKLOOP
10304 025750 104406  TRAP   C$CLP1
10305
10306          ;SET ADAL13 H TO A ZERO. ADAL13 H ON A ZERO WILL ENABLE THE SIGNAL
10307          ;DBLB L TO BE ASSERTED WHEN PSEL1 H IS A ONE.
10308
10309 025752 042737 020000 002330 19$: BIC    #ADAL13,R2LOAD          ;SETUP BIT TO BE CLEARED
10310 025760 004737 006614  JSR    PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REG
10311 025764 001405  BEQ    20$                ;IF LOADED OK THEN CONTINUE
10312 025766          ERRDF  2,ADALRG,R2EROR          ;ADAL REGISTER NOT EQUAL EXPECTED
10313 025766 104455  TRAP   C$ERDF
10314 025770 000002  .WORD  2
10315 025772 002513  .WORD  ADALRG
10316 025774 004770  .WORD  R2EROR
10317 025776          CKLOOP
10318 025776 104406  TRAP   C$CLP1
10319
10320          ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0.
10321
10322 026000 004737 006754 20$: JSR    PC,SLHDAL          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10323
10324          ;SET THE SIGNAL PSELO H TO THE LOW STATE AND SET THE SIGNAL PSEL1 H
10325          ;TO THE HIGH STATE BY SETTING HDAL5 TO ZERO AND HDAL6 TO ONE IN THE
10326          ;HDAL REGISTER.
10327

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TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSES

```

10328 026004 012737 000145 002342      MOV      #HDAL6!HDAL5!HDAL2!DALO,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
10329 026012 042737 000040 002342      BIC      #HDAL5,R6LOAD ;SET THE SIGNAL PSELO H TO LOW STATE
10330 026020 004737 006672                JSR      PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
10331 026024 001405                BEQ      21$ ;IF LOADED OK THEN CONTINUE
10332 026026                ERRDF   4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10333 026026 104455                TRAP    C$ERDF
10334 026030 000004                .WORD   4
10335 026032 002605                .WORD   HDALRG
10336 026034 005020                .WORD   R06ERR
10337 026036                CKLOOP
10338 026036 104406                TRAP    C$CLP1
10339
10340                ;SELECT EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0.
10341
10342 026040 004737 007240      21$:    JSR      PC,SEIDAL ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10343
10344                ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10345                ;BY VDALO H BEING A ONE. THE LOW BYTE OF TDAL BUS IS ENABLED TO THE
10346                ;LOW BYTE OF THE CDAL BUS VIA THE SIGNAL DBLB L. THIS SIGNAL IS
10347                ;ASSERTED LOW AS A RESULT OF THE SIGNALS PSEL1 H AND ADAL13 L BEING
10348                ;ASSERTED HIGH. THE CDAL BUS IS ENABLED TO THE EIDAL BUS UNCONDITIONALLY.
10349                ;THE TIDAL DIAGNOSTIC LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD
10350                ;FORCE JUMP ADDRESS REGISTER DATA.
10351
10352 026044 005037 002342      CLR      R6LOAD ;CLEAR PREVIOUS BITS
10353 026050 111137 002342      MOVB    (R1),R6LOAD ;GET LOW BYTE OF OLD FJA REG DATA LOADED
10354 026054 012737 177400 002346      MOV      #177400,R6MASK ;MASK OUT HIGH BYTE
10355 026062 004737 006700                JSR      PC,READR6 ;READ EIDAL BUS FOR OLD FJA REG DATA
10356 026066 001404                BEQ      22$ ;IF DATA OK THEN CONTINUE
10357 026070                ERRDF   4,FJATDL,R026ER ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10358 026070 104455                TRAP    C$ERDF
10359 026072 000004                .WORD   4
10360 026074 035336                .WORD   FJATDL
10361 026076 050334                .WORD   R026ER
10362 026100                22$:    ENDSEG
10363 026100                10000$:
10364 026100 104405                TRAP    C$ESEG
10365
10366 026102 005721                TST     (R1)+ ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
10367 026104 005302                DEC     R2 ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
10368 026106 001410                BEQ     24$ ;IF YES THEN END OF TEST
10369 026110 000137 024722      JMP     1$ ;IF NOT THEN LOAD NEXT PATTERN
10370
10371 026114 125252      23$:    .WORD   125252
10372 026116 052525                .WORD   052525
10373 026120 177400                .WORD   177400
10374 026122 000377                .WORD   000377
10375 026124 177777                .WORD   177777
10376 026126 000000                .WORD   000000
10377
10378 026130                24$:    ENDTST
10379 026130                L10070:
10380 026130 104401                TRAP    C$ETST

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TEST 39: FDAL REGISTER TO EODAL BUS TO EIDAL BUS TEST

.SBTTL TEST 39: FDAL REGISTER TO EODAL BUS TO EIDAL BUS TEST

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:++
: THIS TEST WILL CHECK THAT THE FDAL REGISTER CAN BE ENABLED TO THE EODAL
: BUS VIA THE SIGNAL INTER L AND THAT THE EODAL BUS CAN BE ENABLED TO THE
: EIDAL BUS VIA THE SIGNAL COLB L. THE TEST WILL ALSO CHECK THAT THE EOAI
: REGISTER CAN BE CLEARED WHEN THE SIGNAL INTER L IS ASSERTED LOW. A BINARY
: COUNT DATA PATTERN WILL BE LOADED INTO THE FDAL REGISTER STARTING WITH A
: DATA PATTERN OF ONE AND INCREMENTING BY FOUR UNTIL THE DATA PATTERN 375 HAS
: BEEN LOADED AND CHECKED.
:--
  
```

10381									
10382									
10383									
10384									
10385									
10386									
10387									
10388									
10389									
10390									
10391									
10392									
10393	026132								
10394	026132								
10395	026132	004737	005510						
10396	026136	005001							
10397									
10398	026140								
10399	026140	104404							
10400									
10401	026142	005037	002346						
10402									
10403									
10404									
10405									
10406	026146	005037	002334						
10407	026152	004737	007712						
10408									
10409									
10410									
10411									
10412									
10413	026156	012737	020000	002330					
10414	026164	004737	006614						
10415	026170	001405							
10416	026172								
10417	026172	104455							
10418	026174	000002							
10419	026176	002513							
10420	026200	004770							
10421	026202								
10422	026202	104406							
10423									
10424									
10425									
10426	026204	004737	006754						
10427									
10428									
10429									
10430									
10431									
10432	026210	012737	000004	002342					
10433	026216	004737	006672						
10434	026222	001405							
10435	026224								
10436	026224	104455							

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BGNTST
T39:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
      CLR R1 ;START BINARY COUNT PATTERN AT ZERO.

1$: BGNSEG
   TRAP C$BSEG

      CLR R6MASK ;SETUP TO CHECK ALL 16 BITS ON REG 6 READ
      ;SET VDAL2 H TO A ONE AND THEN A ZERO TO CLEAR THE PAUSE STATE MACHINE
      ;FLIP-FLOP'S VIA THE SIGNALS INVD L AND INVD H.

      CLR R4LOAD ;SETUP TO 0 ALL OTHER BITS
      JSR PC,CLRPSM ;PULSE INVD L AND INVD H VIA VDAL2 H

      ;SET ADAL13 H TO A ONE IN THE ADAL REGISTER. ADAL13 H ON A ONE WILL
      ;ENABLE THE LOW BYTE OF THE EODAL BUS TO THE CDAL BUS WHEN PSEL1 H IS
      ;ASSERTED HIGH LATER ON IN THIS TEST.

      MOV #ADAL13,R2LOAD ;SETUP BIT TO BE SET TO A ONE
      JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
      BEQ 2$ ;IF LOADED OK THEN CONTINUE
      ERRDF 2,ADALRG,R2ERRR ;ADAL REGISTER NOT EQUAL EXPECTED
      TRAP C$ERDF
      .WORD 2
      .WORD ADALRG
      .WORD R2ERRR
      CKLOOP
      TRAP C$CLP1

      ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

2$: JSR PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0

      ;SET HDAL2 H TO A ONE AND ALL OTHER HDAL BITS TO A ZERO. HDAL2 H ON
      ;A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL
      ;SIGNALS.

      MOV #HDAL2,R6LOAD ;SETUP BIT TO BE LOADED
      JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ 3$ ;IF LOADED OK THEN CONTINUE
      ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
      TRAP C$ERDF
  
```

```

10437 026226 000004          .WORD 4
10438 026230 002605          .WORD HDALRG
10439 026232 005020          .WORD R06ERR
10440 026234                CKLOOP
10441 026234 104406          TRAP C$CLP1
10442
10443                          ;SELECT FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10444
10445 026236 004737 007154    3$: JSR PC,SLFDAL          ;SELECT FDAL AND EOAI REGISTER VIA GDAL
10446
10447                          ;LOAD READ AND CHECK FDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
10448                          ;FROM 1 TO 377 BY AN INCREMENT OF FOUR. THE EOAI REGISTER WILL BE
10449                          ;LOADED AND CHECKED WITH A DATA PATTERN OF ALL ONES.
10450
10451 026242 010137 002342      MOV R1,R6LOAD          ;GET THE FDAL BINARY COUNT PATTERN
10452 026246 052737 177401 002342  BIS #177401,R6LOAD      ;SET ALL EOAI REG BITS TO ONES + FDALO H
10453 026254 004737 006672      JSR PC,LDRDR6          ;LOAD, READ AND CHECK FDAL + EOAI REG'S
10454 026260 001405          BEQ 4$                 ;IF LOADED OK THEN CONTINUE
10455 026262                ERRDF 4,EOAIFD,R06ERR    ;EOAI OR FDAL REGISTER ERROR
10456 026262 104455          TRAP C$ERDF
10457 026264 000004          .WORD 4
10458 026266 002676          .WORD EOAIFD
10459 026270 005020          .WORD R06ERR
10460 026272                CKLOOP
10461 026272 104406          TRAP C$CLP1
10462
10463                          ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10464
10465 026274 004737 006754    4$: JSR PC,SLHDAL          ;SELECT THE HDAL REG VIA GDAL BITS 2:0
10466
10467                          ;SET HDAL6 H TO A ONE TO ASSERT THE SIGNAL XSEL1 L TO THE LOW STATE.
10468                          ;HDAL5 H ON A ZERO WILL CAUSE THE SIGNAL XSELO L TO BE ASSERTED HIGH.
10469                          ;WHEN XSELO L IS ASSERTED HIGH AND XSEL1 L IS ASSERTED LOW, THE SIGNALS
10470                          ;INTER H AND INTER L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY. WHEN
10471                          ;INTER L IS ASSERTED LOW, THE EOAI REGISTER WILL BE CLEARED AND THE FDAL
10472                          ;REGISTER WILL BE ENABLED TO THE LOW BYTE OF THE EODAL BUS.
10473
10474 026300 012737 000104 002342  MOV #HDAL6!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
10475 026306 004737 006672      JSR PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
10476 026312 001405          BEQ 5$                 ;IF LOADED OK THEN CONTINUE
10477 026314                ERRDF 4,HDALRG,R06ERR    HDAL REGISTER NOT EQUAL EXPECTED
10478 026314 104455          TRAP C$ERDF
10479 026316 000004          .WORD 4
10480 026320 002605          .WORD HDALRG
10481 026322 005020          .WORD R06ERR
10482 026324                CKLOOP
10483 026324 104406          TRAP C$CLP1
10484
10485                          ;SELECT THE EOAI AND FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
10486
10487 026326 004737 007154    5$: JSR PC,SLFDAL          ;SELECT EOAI AND FDAL REG VIA GDAL 2:0
10488
10489                          ;WHEN XSELO L IS ASSERTED HIGH AND XSEL1 L IS ASSERTED LOW, THE SIGNALS
10490                          ;INTER H AND INTER L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY. INTER L
10491                          ;BEING ASSERTED LOW WILL CLEAR THE EOAI REGISTER WHICH WAS LOADED WITH
10492                          ;ALL ONES PREVIOUSLY.

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TEST 39: FDAL REGISTER TO EODAL BUS TO EIDAL BUS TEST

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10493
10494 026332 010137 002342      MOV      R1,R6LOAD      ;GET THE FDAL REGISTER DATA
10495 026336 005237 002342      INC      R6LOAD        ;SETUP TO EXPECT FDALO H TO BE SET ALSO
10496 026342 004737 006700      JSR      PC,READR6     ;CHECK IF EOAI REG WAS 0'ED VIA INTER L
10497 026346 001405                BEQ      6$            ;IF DATA OK THEN CONTINUE
10498 026350                ERRDF    4,EOAIFD,R06ERR ;INTER L FAILED TO ZERO EOAI REGISTER
10499 026350 104455                TRAP    C$ERDF
10500 026352 000004                .WORD   4
10501 026354 002676                .WORD   EOAIFD
10502 026356 005020                .WORD   R06ERR
10503 026360                CKLOOP
10504 026360 104406                TRAP    C$CLP1
10505
10506                ;SELECT EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10507
10508 026362 004737 007122      6$: JSR      PC,SEODAL     ;SELECT EODAL BUS VIA GDAL BITS 2:0
10509
10510                ;WHEN THE SIGNAL INTER L IS ASSERTED LOW, THE FDAL REGISTER WILL BE
10511                ;ENABLED TO THE LOW BYTE OF THE EODAL BUS. THIS NEXT SECTION WILL
10512                ;CHECK THE EODAL BUS TO CONTAIN FDAL REGISTER DATA.
10513
10514 026366 010137 002342      MOV      R1,R6LOAD     ;GET FDAL REGISTER DATA LOADED
10515 026372 012737 177400 002346  MOV      #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE ON READ
10516 026400 004737 006700      JSR      PC,READR6     ;READ AND CHECK EODAL BUS FOR FDAL DATA
10517 026404 001405                BEQ      7$            ;IF DATA OK THEN CONTINUE
10518 026406                ERRDF    4,FDAL EO,R06ERR ;FDAL REG TO EODAL BUS ERROR
10519 026406 104455                TRAP    C$ERDF
10520 026410 000004                .WORD   4
10521 026412 003666                .WORD   FDAL EO
10522 026414 005020                .WORD   R06ERR
10523 026416                CKLOOP
10524 026416 104406                TRAP    C$CLP1
10525
10526                ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10527
10528 026420 004737 007240      7$: JSR      PC,SEIDAL     ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10529
10530                ;AT THIS TIME, THE FDAL REGISTER IS ENABLED TO THE LOW BYTE OF THE
10531                ;EODAL BUS VIA THE SIGNAL INTER L. THE LOW BYTE OF THE EODAL BUS IS
10532                ;ENABLED TO THE CDAL BUS AND TO THE EIDAL BUS VIA THE SIGNAL COLB L.
10533                ;THE SIGNAL COLB L IS ASSERTED LOW AS A RESULT OF ADAL13 H BEING A
10534                ;ONE, PSEL1 H BEING ASSERTED HIGH AND PSEL0 L BEING ASSERTED HIGH.
10535
10536 026424 010137 002342      MOV      R1,R6LOAD     ;GET THE FDAL REGISTER DATA LOADED
10537 026430 012737 177400 002346  MOV      #177400,R6MASK ;SETUP TO IGNORE THE HIGH BYTE
10538 026436 004737 006700      JSR      PC,READR6     ;GO READ EIDAL BUS FOR FDAL REG DATA
10539 026442 001405                BEQ      8$            ;IF DATA OK THEN CONTINUE
10540 026444                ERRDF    4,FDAL EI,R026ER ;FDAL REG TO EODAL TO EIDAL BUS ERROR
10541 026444 104455                TRAP    C$ERDF
10542 026446 000004                .WORD   4
10543 026450 003722                .WORD   FDAL EI
10544 026452 005034                .WORD   R026ER
10545 026454                CKLOOP
10546 026454 104406                TRAP    C$CLP1
10547
10548                ;SET THE SIGNAL ADAL13 H TO A ZERO. DOING THIS WILL CAUSE THE SIGNAL

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TEST 39: FDAL REGISTER TO EODAL BUS TO EIDAL BUS TEST

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10549                                     ;COLB L TO BE ASSERTED HIGH, THL'S DISABLING THE EODAL BUS TO THE CDAL
10550                                     ;BUS AND TO THE EIDAL BUS.
10551
10552 026456 005037 002330                8$: CLR      R2LOAD                ;SETUP TO CLEAR ADAL13 H
10553 026462 004737 006614                JSR      PC,LDRDR2            ;GO LOAD, READ AND CHECK ADAL REGISTER
10554 026466 001405                        BEQ      9$                    ;IF LOADED OK THEN CONTINUE
10555 026470                                ERRDF   2,ADALRG,R2EROR        ;ADAL REGISTER NOT EQUAL EXPECTED
10556 026470 104455                        TRAP    C$ERDF
10557 026472 000002                        .WORD   2
10558 026474 002513                        .WORD   ADALRG
10559 026476 004770                        .WORD   R2EROR
10560 026500                                CKLOOP
10561 026500 104406                        TRAP    C$CLP1
10562
10563                                     ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10564
10565 026502 004737 006754                9$: JSR      PC,SLHDAL          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10566
10567                                     ;RESET ALL HDAL REGISTER BITS TO ZERO EXCEPT HDAL REGISTER BIT 2.
10568
10569 026506 012737 000004 002342          MOV      #HDAL2,R6LOAD        ;SETUP TO CLEAR ALL BITS EXCEPT BIT 2
10570 026514 004737 006672                JSR      PC,LDRDR6            ;GO LOAD, READ AND CHECK HDAL REGISTER
10571 026520 001404                        BEQ      10$                   ;IF LOADED OK THEN CONTINUE
10572 026522                                ERRDF   4,HDALRG,R06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
10573 026522 104455                        TRAP    C$ERDF
10574 026524 000004                        .WORD   4
10575 026526 002605                        .WORD   HDALRG
10576 026530 005020                        .WORD   R06ERR
10577 026532                                ENDSEG
10578 026532                                10$:
10579 026532 104405                                10000$: TRAP    C$ESEG
10580
10581 026534 062701 000004                ADD      #FDAL2,R1            ;UPDATE BINARY COUNT PATTERN BY 4
10582 026540 105701                        TSTB    R1                    ;CHECK IF PATTERN DONE
10583 026542 001402                        BEQ      13$                   ;IF YES THEN EXIT THE TEST
10584 026544 000137 026140                JMP      1$                    ;IF NOT THEN LOAD NEXT PATTERN
10585
10586 026550                                13$: ENDTST
10587 026550                                L10071:
10588 026550 104401                        TRAP    C$ETST
10589

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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

.SBTTL TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

;++
: THIS TEST WILL CHECK THAT THE SIGNALS READ H AND MSDI H CAN BE ASSERTED HIGH
: AND LOW. THESE SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE LOGIC LEVELS
: ON THE INPUT SIGNALS TO THE GATES WHICH GENERATE THE SIGNALS. THE SIGNALS
: READ H AND MSDI H ARE READ IN THE VDAL REGISTER AS BITS 3 AND 6 RESPECTIVELY.
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026552 004737 005510
026556 104404
026560 004737 007006
026564 005037 002342
026570 004737 006672
026574 001405
026576 104455
026600 000004
026602 002631
026604 005020
026606 104406
026610 004737 007154
026614 012737 000001 002342
026622 004737 006672
026626 001405
026630 104455
026632 000004
026634 002676
026636 005020
026640 104406

BGNTST
T40:: JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C\$BSEG
;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
JSR PC,SLMODR ;SELECT MODE REG VIA GDAL BITS 2:0
;CLEAR ALL BITS IN THE MODE REGISTER. MODE REGISTER BIT 11 BEING A
;ZERO WILL CAUSE THE SIGNAL MR11 H AND MR11 L TO BE ASSERTED LOW AND
;HIGH RESPECTIVELY.
CLR R6LOAD ;SETUP TO CLEAR ALL MODE REG BITS
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REG
BEQ 1\$;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C\$CLP1
;SELECT THE FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
1\$: JSR PC,SLFDAL ;SELECT FDAL VIA GDAL BITS 2:0
;SET FDALO H TO A ONE AND ALL OTHER FDAL AND EOAI REGISTER BITS TO
;A ZERO. FDALO H ON A ONE WILL ALLOW THE EOAI REGISTER TO BE READ
;ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE CTL REGISTER.
;FDAL1 H ON A ZERO WILL ALLOW THE DMG FLIP-FLOP TO DEASSERT THE SIGNAL
;PSLO H WHEN THE SIGNAL DMG L IS ASSERTED LOW.
MOV #FDALO,R6LOAD ;SETUP BIT TO BE LOADED
JSR PC,LDRDR6 ;LOAD, READ AND CHECK EOAI AND FDAL REG
BEQ 2\$;IF OK THEN CONTINUE
ERRDF 4,EOAIFD,R06ERR ;EOAI OR FDAL REGISTER ERROR
TRAP C\$ERDF
.WORD 4
.WORD EOAIFD
.WORD R06ERR
CKLOOP
TRAP C\$CLP1
;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

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10646
10647 026642 004737 006754      2$:   JSR      PC,SLHDAL          ;SELECT HDAL REG VIA GDAL BITS 2:0
10648
10649                               ;SET HDAL REG BIT 2 ON A 1 AND ALL OTHER BITS TO A 0. HDAL2 H ON A ONE
10650                               ;WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
10651
10652 026646 012737 000004 002342   MOV      #HDAL2,R6LOAD        ;SETUP BIT TO BE LOADED
10653 026654 004737 006672          JSR      PC,LDRDR6           ;GO LOAD, READ AND CHECK HDAL REGISTER
10654 026660 001405          BEQ      3$                  ;IF LOADED OK THEN CONTINUE
10655 026662          ERRDF 4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
10656 026662 104455          TRAP    C$ERRDF
10657 026664 000004          .WORD   4
10658 026666 002605          .WORD   HDALRG
10659 026670 005020          .WORD   R06ERR
10660 026672          CKLOOP
10661 026672 104406          TRAP    C$CLP1
10662
10663                               ;SET ADAL REGISTER BITS 10 AND 0 TO ONES AND ALL OTHER ADAL BITS TO
10664                               ;ZEROS. THE SIGNAL PSLO H WILL BE ASSERTED HIGH WHEN ADAL10 H IS A
10665                               ;ONE AND THE PAUSE STATE WORKING AND DMG FLIP-FLOPS ARE CLEARED. THE
10666                               ;SIGNAL PSLO H WILL ENABLE THE SIGNALS EDEOC H AND REAT H TO THE
10667                               ;SYSTEM BUS AND TO THE VDAL REG. ADALO H ON A 1 WILL HOLD THE BREAK LOGIC CLEARE
10668
10669 026674 012737 002001 002330 3$:   MOV      #ADAL10!ADALO,R2LOAD ;SETUP BITS TO BE LOADED
10670 026702 004737 006614          JSR      PC,LDRDR2           ;LOAD, READ AND CHECK ADAL REGISTER
10671 026706 001405          BEQ      4$                  ;IF LOADED OK THEN CONTINUE
10672 026710          ERRDF 2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
10673 026710 104455          TRAP    C$ERRDF
10674 026712 000002          .WORD   2
10675 026714 002513          .WORD   ADALRG
10676 026716 004770          .WORD   R2EROR
10677 026720          CKLOOP
10678 026720 104406          TRAP    C$CLP1
10679
10680                               ;SET VDAL2 H TO A ONE AND THEN ZERO. THIS IS DONE TO INITIALIZE THE
10681                               ;PAUSE STATE MACHINE FLIP-FLOPS AND ALL OTHER FLIP-FLOPS TO A KNOWN
10682                               ;STATE. SETTING AND CLEARING VDAL2 H WILL CAUSE THE SIGNALS INVD L
10683                               ;AND INVD H TO BE PULSED.
10684
10685 026722 005037 002334          4$:   CLR      R4LOAD              ;SETUP TO CLEAR ALL OTHER R/W BITS
10686 026726 004737 007712          JSR      PC,CLRPSM          ;GO PULSE INVD L VIA VDAL2 H
10687
10688                               ;THE NEXT SECTION WILL SET THE HDAL REGISTER BITS TO THE STATE INDICATED
10689                               ; HDAL3 H - 1 ASSERTS XR/WLB H TO THE HIGH STATE
10690                               ; HDAL4 H - 1 ASSERTS XR/WMB H TO THE HIGH STATE
10691                               ; HDAL12 H - 1 ASSERTS XRAS H TO THE HIGH STATE
10692                               ; HDAL13 H - 1 ASSERTS XCAS H TO THE HIGH STATE
10693                               ;WHEN THE ABOVE SIGNALS ARE SET TO A ONE AND MODE REGISTER BIT 11 IS
10694                               ;CLEARED, THE SIGNAL REAT H WILL BE ASSERTED HIGH. THE SIGNAL REAT H
10695                               ;WILL BE ENABLED TO THE VDAL REGISTER WHEN THE SIGNAL PSLO H IS ASSERTED
10696                               ;HIGH. THE SIGNAL PSLO H IS ASSERTED HIGH AS A RESULT OF THE DMG FLIP-
10697                               ;FLOP BEING CLEARED, ADAL10 H ON A ONE, AND THE PAUSE STATE WORKING FLIP-
10698                               ;FLOP BEING CLEARED. THE SIGNAL REAT H WILL BE READ IN VDAL REGISTER
10699                               ;BIT 3 AS THE SIGNAL READ H. VDAL REGISTER BIT 6, WHICH INDICATES
10700                               ;THE LOGIC LEVEL OF THE SIGNAL MSDI H, WILL ALSO BE SET TO A ONE. MSDI H
10701                               ;IS ASSERTED HIGH AS A RESULT OF SIGNALS XSELO L, ADAL10 H, PSMW L,
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10702                                     ;REAT H, AND ETR L ALL BEING ASSERTED HIGH.
10703
10704 026732 012737 030034 002342      MOV      #HDAL13!HDAL12!HDAL4!HDAL3!HDAL2,R6LOAD ;BITS TO BE LOADED
10705 026740 004737 006672              JSR      PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
10706 026744 001405                      BEQ      5$ ;IF LOADED OK THEN CONTINUE
10707 026746                               ERRDF   4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10708 026746 104455                      TRAP    C$ERDF
10709 026750 000004                      .WORD   4
10710 026752 002605                      .WORD   HDALRG
10711 026754 005020                      .WORD   R06ERR
10712 026756                               CKLOOP
10713 026756 104406                      TRAP    C$CLP1
10714
10715                                     ;CHECK VDAL BITS 6 + 3 TO BE A 1 AS A RESULT OF MSDI H + READ H BEING SET HIGH.
10716
10717 026760 052737 000110 002336 5$:    BIS      #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
10718 026766 004737 006654              JSR      PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10719 026772 001405                      BEQ      6$ ;IF OK THEN CONTINUE
10720 026774                               ERRDF   3,VDALRG,R4EROR ;MSDI H AND/OR READ H PROBABLY NOT SET
10721 026774 104455                      TRAP    C$ERDF
10722 026776 000003                      .WORD   3
10723 027000 002537                      .WORD   VDALRG
10724 027002 005004                      .WORD   R4EROR
10725 027004                               CKLOOP
10726 027004 104406                      TRAP    C$CLP1
10727
10728                                     ;SET ADAL REGISTER BIT 10 TO A ZERO. WHEN ADAL10 H IS A ZERO, THE
10729                                     ;SIGNAL REAT H WILL BE DISABLED FROM THE VDAL REGISTER AS A RESULT OF
10730                                     ;THE SIGNAL PSLO H BEING ASSERTED LOW. THE SIGNAL MSDI H WILL BE
10731                                     ;ASSERTED LOW WHEN ADAL10 H IS SET TO A ZERO.
10732
10733 027006 042737 002000 002330 6$:    BIC      #ADAL10,R2LOAD ;SETUP TO CLEAR ADAL10 H
10734 027014 004737 006614              JSR      PC,LDRDR2 ;GO LOAD, READ AND CHECK ADLA REGISTER
10735 027020 001405                      BEQ      7$ ;IF LOADED OK THEN CONTINUE
10736 027022                               ERRDF   2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
10737 027022 104455                      TRAP    C$ERDF
10738 027024 000002                      .WORD-  2
10739 027026 002513                      .WORD   ADALRG
10740 027030 004770                      .WORD   R2EROR
10741 027032                               CKLOOP
10742 027032 104406                      TRAP    C$CLP1
10743
10744                                     ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H AND MSDI H
10745                                     ;ARE ASSERTED LOW. WHEN PSLO H IS ASSERTED LOW, THE SIGNAL REAT H,
10746                                     ;WHICH IS PRESENTLY HIGH, WILL BE DISABLED FROM THE VDAL REGISTER.
10747
10748 027034 005037 002336 7$:          CLR      R4GOOD ;SETUP TO EXPECT READ H AND MSDI H A 0
10749 027040 004737 006654              JSR      PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10750 027044 001405                      BEQ      8$ ;IF OK THEN CONTINUE
10751 027046                               ERRDF   3,VDALRG,R4EROR ;MSDI H AND/OR READ H PROBABLY NOT 0
10752 027046 104455                      TRAP    C$ERDF
10753 027050 000003                      .WORD   3
10754 027052 002537                      .WORD   VDALRG
10755 027054 005004                      .WORD   R4EROR
10756 027056                               CKLOOP
10757 027056 104406                      TRAP    C$CLP1

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10758
10759 ;SET ADAL10 H TO A 1 TO CAUSE THE SIGNALS PSLO H, REAJ H, + MSDI H TO BE SET HIGH
10760
10761 027060 052737 002000 002330 8$: BIS #ADAL10,R2LOAD ;SET BIT TO SET ADAL10 H TO A ONE
10762 027066 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
10763 027072 001405 BEQ 9$ ;IF LOADED OK THEN CONTINUE
10764 027074 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
10765 027074 104455 TRAP C$ERDF
10766 027076 000002 .WORD 2
10767 027100 002513 .WORD ADALRG
10768 027102 004770 .WORD R2EROR
10769 027104 CKLOOP
10770 027104 104406 TRAP C$CLP1
10771
10772 ;RECHECK THE VDAL REGISTER TO CHECK THAT THE SIGNALS MSDI H AND READ H
10773 ;ARE ASSERTED HIGH AGAIN
10774
10775 027106 052737 000110 002336 9$: BIS #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
10776 027114 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10777 027120 001405 BEQ 10$ ;IF OK THEN CONTINUE
10778 027122 ERRDF 3,VDALRG,R4EROR ;MSDI H AND/OR READ H PROBABLY NOT SET
10779 027122 104455 TRAP C$ERDF
10780 027124 000003 .WORD 3
10781 027126 002537 .WORD VDALRG
10782 027130 005004 .WORD R4EROR
10783 027132 CKLOOP
10784 027132 104406 TRAP C$CLP1
10785
10786 ;SET THE SIGNAL XR/WLB H TO THE LOW STATE BY CLEARING HDAL3 H IN THE
10787 ;HDAL REGISTER. WHEN XR/WLB H IS ASSERTED LOW AND THE SIGNALS XR/WLB H,
10788 ;MR11 L, XRAS H, AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL
10789 ;BE ASSERTED LOW. WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H
10790 ;AND MSDI H WILL BE ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER
10791
10792 027134 042737 000010 002342 10$: BIC #HDAL3,R6LOAD ;SETUP TO SET XR/WLB H TO LOW STATE
10793 027142 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
10794 027146 001405 BEQ 11$ ;IF LOADED OK THEN CONTINUE
10795 027150 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10796 027150 104455 TRAP C$ERDF
10797 027152 000004 .WORD 4
10798 027154 002605 .WORD HDALRG
10799 027156 005020 .WORD R06ERR
10800 027160 CKLOOP
10801 027160 104406 TRAP C$CLP1
10802
10803 ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
10804 ;LOW AS A RESULT OF XR/WLB H BEING ASSERTED LOW.
10805
10806 027162 005037 002336 11$: CLR R4GOOD ;EXPECT MSDI H AND READ H TO BE 0'S
10807 027166 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10808 027172 001405 BEQ 12$ ;IF OK THEN CONTINUE
10809 027174 ERRDF 3,VDALRG,R4EROR ;XR/WLB H PROBABLY NOT ASSERTED LOW
10810 027174 104455 TRAP C$ERDF
10811 027176 000003 .WORD 3
10812 027200 002537 .WORD VDALRG
10813 027202 005004 .WORD R4EROR

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10814 027204
10815 027204 104406
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10824 027206 042737 000020 002342 12$:
10825 027214 052737 000010 002342
10826 027222 004737 006672
10827 027226 001405
10828 027230
10829 027230 104455
10830 027232 000004
10831 027234 002605
10832 027236 005020
10833 027240
10834 027240 104406
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10839 027242 004737 006654 13$:
10840 027246 001405
10841 027250
10842 027250 104455
10843 027252 000003
10844 027254 002537
10845 027256 005004
10846 027260
10847 027260 104406
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10856 027262 052737 000020 002342 14$:
10857 027270 004737 007336
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10862 027274 004737 006654
10863 027300 001405
10864 027302
10865 027302 104455
10866 027304 000003
10867 027306 002537
10868 027310 005004
10869 027312

CKLOOP
TRAP C$CLP1

;SET THE SIGNAL XR/WLB H BACK TO THE HIGH STATE BY SETTING HDAL3 H TO
;A ONE AND SET THE SIGNAL XR/WHB H TO THE LOW STATE BY CLEARING HDAL4 H.
;WHEN XR/WHB H IS ASSERTED LOW AND THE SIGNALS XR/WLB H, MR11 L, XRAS H
;AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
;ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER.

BIC #HDAL4,R6LOAD ;SETUP TO SET XR/WHB H TO LOW STATE
BIS #HDAL3,R6LOAD ;SETUP BIT TO SET XR/WLB H TO HIGH STATE
JSR PC,LDRDR6 ;LOAD, READ AND CHECK THE HDAL REGISTER
BEQ 13$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLOOP
TRAP C$CLP1

;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
;LOW AS A RESULT OF XR/WHB H BEING ASSERTED LOW.

JSR PC,READR4 ;GO READ VDAL AND PAUSE STATE MACHINE
BEQ 14$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;XR/WHB H PROBABLY NOT ASSERTED LOW
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1

;SET THE SIGNAL XR/WHB H BACK TO THE HIGH STATE BY SETTING HDAL4 H TO
;A ONE, AND SET THE SIGNAL XRAS H TO THE LOW STATE BY CLEARING HDAL12 H.
;WHEN XRAS H IS ASSERTED LOW, AND THE SIGNALS XR/WLB H, XR/WHB H, MR11 L,
;AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
;ASSERTED LOW AND READ AS ZEROES IN THE VDLA REGISTER.

BIS #HDAL4,R6LOAD ;SET XR/WHB H TO HIGH STATE
JSR PC,XRASL ;SET XRAS H TO LOW STATE VIA HDAL12 H

;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW
;AS A RESULT OF XRAS H BEING ASSERTED LOW.

JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
BEQ 15$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;THE "AND" OF XRAS H AND XCAS H NOT LOW
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP

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10870 027312 104406 TRAP C$CLP1
10871
10872 ;SET THE SIGNAL XRAS H BACK TO THE HIGH STATE BY SETTING HDAL12 H TO
10873 ;A ONE AND SET THE SIGNAL XCAS H TO THE LOW STATE BY CLEARING HDAL13 H.
10874 ;WHEN XCAS H IS ASSERTED LOW AND THE SIGNALS XR/WLB H, XR/WHB H, MR11 L,
10875 ;AND XRAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
10876 ;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
10877 ;ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER.
10878
10879 027314 052737 010000 002342 15$: BIS #HDAL12,R6LOAD ;SET BIT TO SET XRAS H TO HIGH STATE
10880 027322 004737 007442 JSR PC,XCASL ;SET XCAS H TO LOW STATE VIA HDAL13 H
10881
10882 ;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW
10883 ;AS A RESULT OF XCAS L BEING ASSERTED LOW.
10884
10885 027326 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10886 027332 001405 BEQ 16$ ;IF OK THEN CONTINUE
10887 027334 ERRDF 3,VDALRG,R4EROR ;THE "AND" OF XRAS H AND XCAS H NOT LOW
10888 027334 104455 TRAP C$ERDF
10889 027336 000003 .WORD 3
10890 027340 002537 .WORD VDALRG
10891 027342 005004 .WORD R4EROR
10892 027344 CKLOOP
10893 027344 104406 TRAP C$CLP1
10894
10895 ;SET THE SIGNAL XCAS H BACK TO THE HIGH STATE BY SETTING HDAL13 H TO
10896 ;A ONE. WHEN XCAS H IS SET HIGH, THE SIGNAL REAT H WILL BE ASSERTED
10897 ;HIGH AS A RESULT OF XR/WLB H, XR/WHB H, MR11 L, XRAS H AND XCAS H
10898 ;BEING ASSERTED HIGH. WHEN REAT H IS ASSERTED HIGH, THE SIGNALS READ H
10899 ;AND MSDI H WILL BE ASSERTED HIGH AND READ AS ONES IN THE VDAL REGISTER.
10900
10901 027346 004737 007410 16$: JSR PC,XCASH ;SET XCAS H TO HIGH STATE VIA HDAL13 H
10902
10903 ;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED HIGH
10904 ;AS A RESULT OF REAT H BEING ASSERTED HIGH.
10905
10906 027352 052737 000110 002336 BIS #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
10907 027360 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
10908 027364 001405 BEQ 17$ ;IF OK THEN CONTINUE
10909 027366 ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
10910 027366 104455 TRAP C$ERDF
10911 027370 000003 .WORD 3
10912 027372 002537 .WORD VDALRG
10913 027374 005004 .WORD R4EROR
10914 027376 CKLOOP
10915 027376 104406 TRAP C$CLP1
10916
10917 ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10918
10919 027400 004737 007006 17$: JSR PC,SLMODR ;SELECT MODE REGISTE VIA GDAL BITS 2:0
10920
10921 ;SET MODE REGISTER BIT 11 TO A ONE TO SET THE SIGNAL MR11 H TO THE
10922 ;HIGH STATE AND THE SIGNAL MR11 L TO THE LOW STATE.
10923
10924 027404 012737 004000 002342 MOV #MR11,R6LOAD ;SETUP BIT TO BE LOADED
10925 027412 004737 006672 JSR PC,LDRDR6 ;LOAD, READ AND CHECK MODE REGISTER
  
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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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10926 027416 001405          BEQ      18$                ;IF LOADED OK THEN CONTINUE
10927 027420                ERRDF   4,MODREG,R06ERR    ;MODE REGISTER NOT EQUAL EXPECTED
10928 027420 104455          TRAP   C$ERDF
10929 027422 000004          .WORD  4
10930 027424 002631          .WORD  MODREG
10931 027426 005020          .WORD  R06ERR
10932 027430                CKLOOP
10933 027430 104406          TRAP   C$CLP1
10934
10935                ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10936
10937 027432 004737 006754      18$:   JSR    PC,SLHDAL          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10938 027436 012737 030034 002342  MOV    #HDAL13!HDAL12!HDAL4!HDAL3!HDAL2,R6LOAD ;BITS PREVIOUSLY LOADED
10939
10940                ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW,
10941                ;WHEN MR11 L IS ASSERTED LOW AND THE SIGNALS XR/WLB H, XR/WHB H, XRAS H
10942                ;AND XCAS H ARE ASSERTED HIGH.
10943
10944 027444 005037 002336      CLR    R4GOOD            ;EXPECT READ H AND MSDI H TO BE 0
10945 027450 004737 006654      JSR    PC,READR4        ;READ VDAL AND PAUSE STATE MACHINE
10946 027454 001405          BEQ    19$                ;IF OK THEN CONTINUE
10947 027456                ERRDF   3,VDALRG,R4EROR    ;READ H AND/OR MSDI H ARE SET HIGH
10948 027456 104455          TRAP   C$ERDF
10949 027460 000003          .WORD  3
10950 027462 002537          .WORD  VDALRG
10951 027464 005004          .WORD  R4EROR
10952 027466                CKLOOP
10953 027466 104406          TRAP   C$CLP1
10954
10955                ;SET THE SIGNAL XR/WHB L TO THE HIGH STATE BY CLEARING HDAL4 H. WHEN
10956                ;XR/WHB L, MR11 H, XRAS H AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H
10957                ;WILL BE ASSERTED HIGH. WHEN REAT H IS ASSERTED HIGH, THE SIGNALS
10958                ;READ H + MSDI H WILL BE ASSERTED HIGH AND READ AS ONES IN THE VDAL REG.
10959
10960 027470 042737 000020 002342 19$:   BIC    #HDAL4,R6LOAD      ;SET XR/WHB L TO THE HIGH STATE
10961 027476 004737 006672      JSR    PC,LDRDR6        ;LOAD, READ AND CHECK HDAL REGISTER
10962 027502 001405          BEQ    20$                ;IF OK THEN CONTINUE
10963 027504                ERRDF   4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
10964 027504 104455          TRAP   C$ERDF
10965 027506 000004          .WORD  4
10966 027510 002605          .WORD  HDALRG
10967 027512 005020          .WORD  R06ERR
10968 027514                CKLOOP
10969 027514 104406          TRAP   C$CLP1
10970
10971                ;READ THE VDAL REGISTER AND CHECK THAT READ H AND MSDI H ARE SET TO ONES
10972                ;AS A RESULT OF MR11 H, XR/WHB L, XRAS H AND XCAS H BEING ASSERTED HIGH.
10973
10974 027516 052737 000110 002336 20$:   BIS    #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
10975 027524 004737 006654      JSR    PC,READR4        ;READ VDAL AND PAUSE STATE MACHINE F/F'S
10976 027530 001405          BEQ    21$                ;IF OK THEN CONTINUE
10977 027532                ERRDF   3,VDALRG,R4EROR    ;REAT H PROBABLY NOT ASSERTED HIGH
10978 027532 104455          TRAP   C$ERDF
10979 027534 000003          .WORD  3
10980 027536 002537          .WORD  VDALRG
10981 027540 005004          .WORD  R4EROR

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10982 027542          CKLOOP
10983 027542 104406  TRAP   C$CLP1
10984
10985                ;SET THE SIGNAL XRAS H TO THE LOW STATE TO CHECK THAT THE "AND"
10986                ;CONDITION OF XRAS H AND XCAS H WILL CAUSE THE SIGNAL REAT H TO BE
10987                ;ASSERTED LOW.
10988
10989 027544 004737 007336 21$: JSR   PC,XRASL          ;SET XRAS H TO LOW STATE
10990
10991                ;READ THE VDAL REGISTER TO CHECK THAT XRAS H BEING SET LOW CAUSED THE
10992                ;SIGNALS READ H AND MSDI H TO BE ASSERTED LOW AS A RESULT OF REAT H BEING
10993                ;SET TO THE LOW STATE.
10994
10995 027550 005037 002336  CLR   R4GOOD          ;EXPECT READ H AND MSDI H TO BE ZEROES
10996 027554 004737 006654  JSR   PC,READR4       ;READ VDAL AND PAUSE STATE MACHINE
10997 027560 001405        BEQ   22$              ;IF OK THEN CONTINUE
10998 027562        ERRDF  3,VDALRG,R4EROR  ;REAT H, READ H, MSDI H OR PSLO H ERROR
10999 027562 104455        TRAP  C$ERDF
11000 027564 000003        .WORD 3
11001 027566 002537        .WORD VDALRG
11002 027570 005004        .WORD R4EROR
11003 027572          CKLOOP
11004 027572 104406  TRAP   C$CLP1
11005
11006                ;SET THE SIGNAL XRAS H BACK TO THE HIGH STATE BY SETTING HDAL12 H TO A 1
11007
11008 027574 004737 007304 22$: JSR   PC,XRASH          ;ASSERT XRAS H TO HIGH STATE VIA HDAL12 H
11009
11010                ;READ THE VDAL REGISTER AGAIN TO CHECK THAT READ H AND MSDI H ARE SET
11011                ;TO ONES AS A RESULT OF REAT H BEING ASSERTED HIGH.
11012
11013 027600 052737 000110 002336  BIS   #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
11014 027606 004737 006654  JSR   PC,READR4       ;READ VDAL AND PAUSE STATE MACHINE
11015 027612 001405        BEQ   23$              ;IF OK THEN CONTINUE
11016 027614        ERRDF  3,VDALRG,R4EROR  ;READ H AND/OR MSDI H NOT SET TO 1'S
11017 027614 104455        TRAP  C$ERDF
11018 027616 000003        .WORD 3
11019 027620 002537        .WORD VDALRG
11020 027622 005004        .WORD R4EROR
11021 027624          CKLOOP
11022 027624 104406  TRAP   C$CLP1
11023
11024                ;SET THE SIGNAL XSELO L TO THE LOW STATE BY SETTING HDAL5 H TO A ONE.
11025                ;WHEN XSELO L IS ASSERTED LOW, THE SIGNAL MSDI H WILL BE ASSERTED LOW.
11026
11027 027626 052737 000040 002342 23$: BIS   #HDAL5,R6LOAD       ;SET BIT TO SET XSELO L TO LOW STATE
11028 027634 004737 006672  JSR   PC,LDRDR6       ;GO LOAD, READ AND CHECK HDAL REGISTER
11029 027640 001405        BEQ   24$              ;IF LOADED OK THEN CONTINUE
11030 027642        ERRDF  4,HDALRG,R06ERR  ;HDAL REGISTER NOT EQUAL EXPECTED
11031 027642 104455        RAP   C$ERDF
11032 027644 000004        .WORD 4
11033 027646 002605        .WORD HDALRG
11034 027650 005020        .WORD R06ERR
11035 027652          CKLOOP
11036 027652 104406  TRAP   C$CLP1
11037

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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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11038                                     ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL MSDI H IS ASSERTED
11039                                     ;LOW WHEN THE SIGNAL XSELO L IS ASSERTED LOW.
11040
11041 027654 042737 000100 002336 24$: BIC #VDAL R4GOOD ;EXPECT MSDI H TO BE A ZERO
11042 027662 004737 006654 JSR PC,REALR4 ;READ VDAL AND PAUSE STATE MACHINE
11043 027666 001405 BEQ 25$ ;IF OK THEN CONTINUE
11044 027670 ERRDF 3,VDALRG,R4EROR ;MSDI H NOT A 0 BY XSELO L BEING SET LOW
11045 027670 104455 TRAP C$ERDF
11046 027672 000003 .WORD 3
11047 027674 002537 .WORD VDALRG
11048 027676 005004 .WORD R4EROR
11049 027700 CKLOOP
11050 027700 104406 TRAP C$CLP1
11051
11052                                     ;SET THE SIGNAL DMG L BY SETTING XSELO L AND XSEL1 L TO THE LOW STATE.
11053                                     ;WHEN DMG L IS SET LOW, THE DMG FLIP-FLOP WILL BE SET, THUS CAUSING
11054                                     ;THE SIGNAL PSLO H TO BE ASSERTED LOW. WHEN THE SIGNAL PSLO H IS ASSERTED
11055                                     ;LOW, THE SIGNAL REAT H WILL BE DISABLED TO THE SIGNAL READ H, THUS
11056                                     ;CAUSING THE SIGNAL READ H TO BE ASSERTED LOW. THE SIGNAL READ H WILL
11057                                     ;BE READ AS A ZERO IN THE VDAL REGISTER.
11058
11059 027702 052737 000100 002342 25$: BIS #HDAL6,R6LOAD ;SET BIT TO SET XSEL1 L TO LOW STATE
11060 027710 004737 006672 JSR PC,LDRDR6 ;LOAD, READ AND CHECK HDAL REGISTER
11061 027714 001405 BEQ 26$ ;IF OK THEN CONTINUE
11062 027716 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
11063 027716 104455 TRAP C$ERDF
11064 027720 000004 .WORD 4
11065 027722 002605 .WORD HDALRG
11066 027724 005020 .WORD R06ERR
11067 027726 CKLOOP
11068 027726 104406 TRAP C$CLP1
11069
11070                                     ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H WAS ASSERTED
11071                                     ;LOW WHEN THE DMG FLIP-FLOP WAS SET TO A ONE BY DMG L BEING ASSERTED LOW.
11072                                     ;THE SIGNAL READ H SHOULD BE A ZERO WHEN PSLO H IS ASSERTED LOW.
11073
11074 027730 042737 000010 002336 26$: BIC #VDAL3,R4GOOD ;EXPECT READ H TO BE A ZERO
11075 027736 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
11076 027742 001405 BEQ 27$ ;IF OK THEN CONTINUE
11077 027744 ERRDF 3,VDALRG,R4EROR ;PSLO H NOT LOW WHEN DMG F/F SET TO ONE
11078 027744 104455 TRAP C$ERDF
11079 027746 000003 .WORD 3
11080 027750 002537 .WORD VDALRG
11081 027752 005004 .WORD R4EROR
11082 027754 CKLOOP
11083 027754 104406 TRAP C$CLP1
11084
11085                                     ;SELECT FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
11086
11087 027756 004737 007154 27$: JSR PC,SLFDAL ;SELECT FDAL AND EOAI REG VIA GDAL 2:0
11088
11089                                     ;SET FDALO H AND FDAL1 H TO ONES AND ALL OTHER FDAL AND EOAI REGISTER
11090                                     ;BITS TO ZEROES. FDALO H ON A ONE WILL ENABLE THE EOAI REGISTER TO BE
11091                                     ;READ WITH THE FDAL REGISTER INSTEAD OF THE CTL REGISTER WHEN A READ
11092                                     ;COMMAND IS ISSUED TO CONTROL REGISTER 6.
11093

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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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11094 027762 012737 000003 002342      MOV      #FDAL1!FDALO,R6LOAD      ;SETUP BITS TO BE LOADED
11095 027770 004737 006672              JSR      PC,LDRDR6                ;LOAD, READ AND CHECK FDAL AND EOAI REG'S
11096 027774 001405                      BEQ      28$                       ;IF LOADED OK THEN CONTINUE
11097 027776                      ERRDF   4,EOAIFD,R06ERR           ;EOAI OR FDAL REGISTER ERROR
11098 027776 104455                      TRAP    C$ERDF
11099 030000 000004                      .WORD   4
11100 030002 002676                      .WORD   EOAIFD
11101 030004 005020                      .WORD   R06ERR
11102 030006                      CKLOOP
11103 030006 104406                      TRAP    C$CLP1
11104
11105
11106                      ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H IS ASSERTED HIGH
11107                      ;WHEN FDAL1 H IS A ONE AND THE DMG FLIP-FLOP IS SET TO A ONE. THE
11108                      ;SIGNAL REAT H, WHICH IS HIGH, SHOULD BE ENABLED TO VDAL REGISTER BIT 3
11109                      ;AND READ AS A ONE WHEN PSLO H IS ASSERTED HIGH.
11110 030010 052737 000010 002336 28$:      BIS      #VDAL3,R4GOOD            ;EXPECT READ H TO BE A ONE
11111 030016 004737 006654              JSR      PC,READR4                ;READ VDAL AND PAUSE STATE MACHINE
11112 030022 001405                      BEQ      29$                       ;IF OK THEN CONTINUE
11113 030024                      ERRDF   3,VDALRG,R4EROR         ;PSLO H PROBABLY NOT SET HIGH BY FDAL1 H
11114 030024 104455                      TRAP    C$ERDF
11115 030026 000003                      .WORD   3
11116 030030 002537                      .WORD   VDALRG
11117 030032 005004                      .WORD   R4EROR
11118 030034                      CKLOOP
11119 030034 104406                      TRAP    C$CLP1
11120
11121                      ;SET FDAL1 H BACK TO THE LOW STATE BY CLEARING FDAL1 H IN FDLA REGISTER
11122
11123 030036 042737 000002 002342 29$:      BIC      #FDAL1,R6LOAD            ;SETUP TO CLEAR FDAL1 H
11124 030044 004737 006672              JSR      PC,LDRDR6                ;GO LOAD, READ AND CHECK FDAL AND EOAI
11125 030050 001405                      BEQ      30$                       ;IF OK THEN CONTINUE
11126 030052                      ERRDF   4,EOAIFD,R06ERR           ;EOAI OR FDAL REGISTER ERROR
11127 030052 104455                      TRAP    C$ERDF
11128 030054 000004                      .WORD   4
11129 030056 002676                      .WORD   EOAIFD
11130 030060 005020                      .WORD   R06ERR
11131 030062                      CKLOOP
11132 030062 104406                      TRAP    C$CLP1
11133
11134                      ;WHEN FDAL1 H IS A ZERO AND THE DMG FLIP-FLOP IS SET TO A ONE, THE
11135                      ;SIGNAL PSLO H WILL BE ASSERTED LOW. WHEN PSLO H IS ASSERTED LOW, THE
11136                      ;SIGNAL READ H WILL BE READ AS A ZERO IN THE VDAL REGISTER. THE
11137                      ;SIGNAL READ H IS READ IN THE VDAL REGISTER AS BIT 3.
11138
11139 030064 005037 002336 30$:      CLR      R4GOOD                    ;EXPECT READ H TO BE A ZERO
11140 030070 004737 006654              JSR      PC,R=ADR4                ;READ VDAL AND PAUSE STATE MACHINE
11141 030074 001405                      BEQ      31$                       ;IF OK THEN CONTINUE
11142 030076                      ERRDF   3,VDALRG,R4EROR         ;PSLO H PROBABLY NOT SET LOW
11143 030076 104455                      TRAP    C$ERDF
11144 030100 000003                      .WORD   3
11145 030102 002537                      .WORD   VDALRG
11146 030104 005004                      .WORD   R4EROR
11147 030106                      CKLOOP
11148 030106 104406                      TRAP    C$CLP1
11149

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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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11150                                     ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11151
11152 030110 004737 006754          31$: JSR      PC,SLHDAL          ;SELECT HDAL REG VIA GDAL BITS 2:0
11153
11154                                     ;SET XSEL1 L AND XSELO L BACK TO THE HIGH STATE BY CLEARING HDAL6 AND
11155                                     ;HDAL5 H. THIS WILL SET THE SIGNAL DMG L TO THE HIGH STATE AND ASSERT
11156                                     ;THE SIGNAL MSDI H TO THE HIGH STATE. THE SIGNAL XRAS H WILL BE SET LOW
11157                                     ;AND THEN BACK TO THE HIGH STATE TO CLOCK THE DMG F/F TO THE CLEARED STATE.
11158
11159 030114 012737 030004 002342     MOV      #HDAL13!HDAL12!HDAL2,R6LOAD ;SETUP BITS TO BE CLEARED
11160 030122 004737 007336             JSR      PC,XRASL          ;SET XRAS H TO LOW STATE
11161 030126 004737 007304             JSR      PC,XRASH         ;SET XRAS H TO HIGH STATE
11162
11163                                     ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
11164                                     ;HIGH WHEN MR11 H, XR/WHB L, XRAS H, XCAS H, PSLO H, XSELO L, ADAL10 H,
11165                                     ;REAT H, AND ETR L ARE ASSERTED HIGH AND THE PAUSE STATE WORKING FLIP-
11166                                     ;FLOP IS CLEARED.
11167
11168 030132 052737 000110 002336     BIS      #VDAL6!VDAL3,R4GOOD        ;EXPECT READ H AND MSDI H TO BE SET
11169 030140 004737 006654             JSR      PC,READR4         ;READ VDAL AND PAUSE STATE MACHINE
11170 030144 001405                     BEQ      32$               ;IF OK THEN CONTINUE
11171 030146                             ERRDF   3,VDALRG,R4EROR      ;DMG FLIP-FLOP PROBABLY NOT CLEARED
11172 030146 104455                     TRAP    C$ERDF
11173 030150 000003                     .WORD   3
11174 030152 002537                     .WORD   VDALRG
11175 030154 005004                     .WORD   R4EROR
11176 030156                             CKLOOP
11177 030156 104406                     TRAP    C$CLP1
11178
11179                                     ;SET THE SIGNAL DMG L TO THE LOW STATE AGAIN BY SETTING XSELO L AND
11180                                     ;XSEL1 L TO THE LOW STATE. WHEN DMG L IS ASSERTED LOW, THE DMG FLIP-
11181                                     ;FLOP WILL BE SET TO A ONE, THUS CAUSING THE SIGNAL PSLO H TO BE
11182                                     ;ASSERTED LOW. WHEN PSLO H IS SET LOW, THE SIGNAL REAT H, WHICH IS HIGH,
11183                                     ;WILL BE DISBALED FROM THE SIGNAL READ H, THUS CAUSING READ H TO BE
11184                                     ;READ IN THE VDAL REGISTER AS A ZERO.
11185
11186 030160 052737 000140 002342 32$: BIS      #HDAL6!HDAL5,R6LOAD        ;SETUP BITS TO BE LOADED
11187 030166 004737 006672             JSR      PC,LDRDR6         ;LOAD, READ AND CHECK HDAL REGISTER
11188 030172 001405                     BEQ      33$               ;IF OK THEN CONTINUE
11189 030174                             ERRDF   4,HDALRG,R06ERR     ;HDAL REGISTER NOT EQUAL EXPECTED
11190 030174 104455                     TRAP    C$ERDF
11191 030176 000004                     .WORD   4
11192 030200 002605                     .WORD   HDALRG
11193 030202 005020                     .WORD   R06ERR
11194 030204                             CKLOOP
11195 030204 104406                     TRAP    C$CLP1
11196
11197                                     ;READ THE VDAL REGISTER TO CHECK THAT PSLO H IS ASSERTED LOW AS A
11198                                     ;RESULT OF THE DMG FLIP-FLOP BEING SET TO A ONE AND THAT MSDI H IS
11199                                     ;ASSERTED LOW AS A RESULT OF XSELO L BEING ASSERTED LOW.
11200
11201 030206 005037 002336          33$: CLR      R4GOOD              ;EXPECT READ H AND MSDI H TO BE A 0
11202 030212 004737 006654             JSR      PC,READR4         ;READ VDAL AND PAUSE STATE MACHINE
11203 030216 001405                     BEQ      34$               ;IF OK THEN CONTINUE
11204 030220                             ERRDF   3,VDALRG,R4EROR     ;VDAL OR PAUSE STATE MACHINE ERROR
11205 030220 104455                     TRAP    C$ERDF

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TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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11206 030222 000003          .WORD 3
11207 030224 002537          .WORD VDALRG
11208 030226 005004          .WORD R4EROR
11209 030230          CKLOOP
11210 030230 104406          TRAP C$CLP1
11211
11212          ;SET DMG L TO THE HIGH STATE AGAIN BY SETTING XSELO L AND XSEL1 L TO
11213          ;THE HIGH STATE. WHEN XSELO L IS RETURNED TO THE HIGH STATE, MSDI H
11214          ;WILL BE ASSERTED HIGH.
11215
11216 030232 042737 000140 002342 34$: BIC #HDAL6!HDAL5,R6LOAD ;SETUP TO SET XSELO L AND XSEL1 L HIGH
11217 030240 004737 006672          JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
11218 030244 001405          BEQ 35$ ;IF OK THEN CONTINUE
11219 030246          ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL TO EXPECTED
11220 030246 104455          TRAP C$ERDF
11221 030250 000004          .WORD 4
11222 030252 002605          .WORD HDALRG
11223 030254 005020          .WORD R06ERR
11224 030256          CKLOOP
11225 030256 104406          TRAP C$CLP1
11226
11227          ;SET VDAL2 H TO A ONE TO SET THE SIGNAL INVD L TO THE LOW STATE. WHEN
11228          ;VDAL2 H IS ASSERTED LOW, THE DMG FLIP-FLOP WILL BE CLEARED, THUS
11229          ;CAUSING THE SIGNAL PSLO H TO BE ASSERTED HIGH AGAIN. READ THE VDAL
11230          ;REGISTER TO CHECK THAT READ H AND MSDI H ARE ONES AS A RESULT OF
11231          ;REAT H BEING ASSERTED HIGH, PSLO H BEING ASSERTED HIGH AND XSELO L BEING
11232          ;ASSERTED HIGH.
11233
11234 030260 012737 000004 002334 35$: MOV #VDAL2,R4LOAD ;SETUP BIT TO SET INVD L LOW
11235 030266 013737 002334 002336 MOV R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
11236 030274 052737 000110 002336 BIS #VDAL6!VDAL3,R4GOOD ;SETUP TO EXPECT READ H AND MSDI H AS 1'S
11237 030302 004737 006646          JSR PC,LDRD4R ;LOAD, READ AND CHECK VDAL REGISTER
11238 030306 001405          BEQ 36$ ;IF LOADED OK THEN CONTINUE
11239 030310          ERRDF 3,VDALRG,R4EROR ;INVD L FAILED TO CLEAR DMG FLIP-FLOP
11240 030310 104455          TRAP C$ERDF
11241 030312 000003          .WORD 3
11242 030314 002537          .WORD VDALRG
11243 030316 005004          .WORD R4EROR
11244 030320          CKLOOP
11245 030320 104406          TRAP C$CLP1
11246
11247          ;SET THE SIGNAL INVD L BACK TO THE HIGH STATE BY CLEARING VDAL2 H.
11248          ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
11249          ;THE SIGNALS READ H AND MSDI H SHOULD STILL BE READ AS ONES IN VDAL REG.
11250
11251 030322 012737 000200 002334 36$: MOV #VDAL7,R4LOAD ;SETUP BIT TO LOAD - CLEAR VDAL2 H
11252 030330 013737 002334 002336 MOV R4LOAD,R4GOOD ;COPY DATA LOADED TO EXPECTED
11253 030336 052737 000110 002336 BIS #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
11254 030344 004737 006646          JSR PC,LDRD4R ;LOAD, READ AND CHECK VDAL REGISTER
11255 030350 001405          BEQ 37$ ;IF LOADED THEN CONTINUE
11256 030352          ERRDF 3,VDALRG,R4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
11257 030352 104455          TRAP C$ERDF
11258 030354 000003          .WORD 3
11259 030356 002537          .WORD VDALRG
11260 030360 005004          .WORD R4EROR
11261 030362          CKLOOP
  
```


TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'

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11262 030362 104406          TRAP    C$CLP1
11263
11264                      ;THE PROGRAM WILL NOW PULSE XRAS H FROM THE HIGH STATE TO THE LOW
11265                      ;STATE AND THEN BACK TO THE HIGH STATE.  WHEN XRAS H IS RETURNED
11266                      ;TO THE HIGH STATE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT
11267                      ;SET TO A ONE BY THE SIGNALS SOP H AND EDFET H BEING ASSERTED HIGH.
11268
11269 030364 004737 007336    37$:   JSR    PC,XRASL          ;SET XRAS H TO LOW STATE
11270 030370 004737 007304    JSR    PC,XRASH          ;SET XRAS H TO HIGH STATE
11271
11272                      ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNALS
11273                      ;PSLO H AND MSDI H WILL BE ASSERTED LOW.  WHEN PSLO H IS ASSERTED LOW
11274                      ;THE SIGNAL REAT H WILL BE DISABLED FROM THE VDAL REGISTER THUS
11275                      ;CAUSING THE SIGNAL READ H TO BE READ AS A ZERO.
11276
11277 030374 052737 001000 002336    BIS    #VDAL9,R4GOOD      ;EXPECT PSMW H TO BE SET TO A ONE
11278 030402 042737 000110 002336    BIC    #VDAL6!VDAL3,R4GOOD ;EXPECT READ H AND MSDI H TO BE A 0
11279 030410 004737 006654          JSR    PC,READR4         ;READ VDAL AND PAUSE STATE MACHINE
11280 030414 001405          BEQ    38$               ;IF OK THEN CONTINUE
11281 030416          ERRDF 3,VDALRG,R4EROR    ;PSMW L PROBABLY NOT ASSERTED LOW
11282 030416 104455          TRAP  C$ERDF
11283 030420 000003          .WORD 3
11284 030422 002537          .WORD VDALRG
11285 030424 005004          .WORD R4EROR
11286 030426          CKLOOP
11287 030426 104406          TRAP  C$CLP1
11288
11289                      ;CLEAR ALL BITS IN HDAL REGISTER EXCEPT HDAL2 H
11290
11291 030430 012737 000004 002342 38$:   MOV    #HDAL2,R6LOAD      ;SETUP TO CLEAR ALL BITS EXCEPT HDAL2 H
11292 030436 004737 006672          JSR    PC,LDRDR6         ;LOAD, READ AND CHECK VDAL REGISTER
11293 030442 001405          BEQ    39$               ;IF LOADED OK THEN CONTINUE
11294 030444          ERRDF 4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
11295 030444 104455          TRAP  C$ERDF
11296 030446 000004          .WORD 4
11297 030450 002605          .WORD HDALRG
11298 030452 005020          .WORD R06ERR
11299 030454          CKLOOP
11300 030454 104406          TRAP  C$CLP1
11301
11302                      ;PULSE INVD L TO CLEAR ALL PAUSE STATE MACHINE FLIP-FLOPS AND ANY OTHER
11303                      ;FLIP-FLOPS THAT MAY BE SET AT THIS TIME.
11304
11305 030456 005037 002334    39$:   CLR    R4LOAD            ;EXPECT VDAL REGISTER BITS TO BE ZERO
11306 030462 004737 007712          JSR    PC,CLRPSM        ;PULSE INVD L VIA VDAL2 H
11307
11308          ENDSEG
11309 030466    10000$:
11310 030466 104405          TRAP  C$ESEG
11311 030470          ENDTST
11312 030470    L10072:
11313 030470 104401          TRAP  C$ETST
  
```

TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

.SBTTL TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

```

:++
: THIS TEST WILL CHECK THAT THE SIGNALS FETCT H AND BTS1 H CAN BE ASSERTED HIGH
: AND LOW. THESE TWO SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE INPUT
: SIGNALS TO THE GATES WHICH GENERATE THESE SIGNALS. THE PAUSE STATE MACHINE
: LOGIC IS USE' TO TEST THE SIGNAL FETCT H. THE SIGNAL FETCT H IS ALSO CHECKED
: ON THE SIGNA ITS1 H. THE SIGNAL BTS1 H IS READ IN THE VDAL REGISTER ON BIT 5.
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 030500 004737 007006
 030504 005037 002342
 030510 004737 006672
 030514 001405
 030516 104455
 030520 000004
 030522 002631
 030524 005020
 030526 104406
 030530 004737 006754
 030534 012737 000004 002342
 030542 004737 006672
 030546 001405
 030550 104455
 030552 000004
 030554 002605
 030556 005020
 030560 104406

```

T41:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C$BSEG
;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
JSR PC,SLMODR ;SELECT MODE REGISTER VIA GDAL BITS 2:0
;CLEAR ALL BITS IN THE MODE REGISTER WHICH WILL SET ALL OUTPUTS LOW.
CLR R6LOAD ;SETUP TO CLEAR ALL BITS
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REGISTER
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL TO ZERO
TRAP C$ERDF
.WORD 4
.WORD MODREG
.WORD R06ERR
CKLOOP
TRAP C$CLP1
;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
1$: JSR PC,SLHDAL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
;SET HDAL2 H TO A ONE AND ALL OTHER HDAL BITS TO ZEROES. WHEN HDAL2 H
;IS SET TO A ONE, THE PROGRAM HAS CONTROL OVER THE T-11 TIMING AND
;CONTROL SIGNALS.
MOV #HDAL2,R6LOAD ;SETUP BIT TO BE LOADED
JSR PC,LDRDR6 ;LOAD, READ AND CHECK HDAL REGISTER
BEQ 2$ ;IF OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL TO EXPECTED
TRAP C$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLOOP
TRAP C$CLP1
;SET ADAL10 H TO A ONE AND ALL OTHER ADAL BITS TO A ZERO. ADAL10 H
;ON A ONE WILL ENABLE THE SIGNAL BTS1 H TO VDAL REGISTER BIT 5.
  
```

TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11370 030562 012737 002000 002330 2$: MOV #ADAL10,R2LOAD ;SETUP BIT TO BE LOADED
11371 030570 004737 006614 JSR PC,LDRDR2 ;LOAD, READ AND CHECK ADAL REGISTER
11372 030574 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
11373 030576 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
11374 030576 104455 TRAP C$ERDF
11375 030600 .WORD 2
11376 030602 .WORD ADALRG
11377 030604 .WORD R2EROR
11378 030606 CKLOOP
11379 030606 104406 TRAP C$CLP1
11380
11381 ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING THE SIGNAL VDAL2 H.
11382 ;THE SIGNAL INVD L, WHEN PULSED, WILL CLEAR THE PAUSE STATE MACHINE
11383 ;FLIP-FLOPS, AND OTHER FLIP-FLOPS ON THE MODULE INCLUDING THE BTFET
11384 ;FLIP-FLCP
11385
11386 030610 005037 002334 3$: CLR R4LOAD ;SETUP TO CLEAR ALL R/W BITS
11387 030614 004737 007712 JSR PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
11388
11389 ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
11390 ;LOW STATE AND XSELO L TO THE HIGH STATE. WHEN HDAL5 H IS SET TO A
11391 ;ZERO, THE SIGNAL XSELO L WILL BE ASSERTED HIGH. WHEN HDAL6 H IS SET
11392 ;TO A ONE, THE SIGNAL XSEL1 L WILL BE ASSERTED LOW.
11393
11394 030620 012737 000104 002342 MOV #HDAL6!HDAL2,R6LOAD ;SET XSEL1 L TO LOW STATE VIA HDAL6 H
11395 030626 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
11396 030632 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
11397 030634 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EPXECTED
11398 030634 104455 TRAP C$ERDF
11399 030636 .WORD 4
11400 030640 .WORD HDALRG
11401 030642 .WORD R06ERR
11402 030644 CKLOOP
11403 030644 104406 TRAP C$CLP1
11404
11405 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL BTS1 H IS ASSERTED
11406 ;HIGH WHEN THE SIGNAL INTER L IS ASSERTED LOW AND THE BTFET FLIP-FLOP
11407 ;IS CLEARED. THE BTFET FLIP-FLOP WAS CLEARED WHEN INVD L WAS PULSED.
11408
11409 030646 052737 000040 002336 4$: BIS #VDAL5,R4GOOD ;SETUP TO EXPECT BTS1 H TO EQUAL A ONE
11410 030654 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
11411 030660 001405 BEQ 5$ ;IF OK THEN CONTINUE
11412 030662 ERRDF 3,VDALRG,R4EROR ;BTS1 H NOT A 1 WHEN INTER L SET LOW
11413 030662 104455 TRAP C$ERDF
11414 030664 .WORD 3
11415 030666 .WORD VDALRG
11416 030670 .WORD R4EROR
11417 030672 CKLOOP
11418 030672 104406 TRAP C$CLP1
11419
11420 ;SET THE SIGNAL XSEL1 L TO THE HIGH STATE BY CLEARING HDAL6 H AND SET
11421 ;THE SIGNAL XSELO L TO THE LOW STATE BY SETTING HDAL5 H TO A ONE. WHEN
11422 ;XSELO L IS ASSERTED LOW AND XSEL1 L IS ASSERTED HIGH, THE SIGNAL INTER L
11423 ;WILL BE ASSERTED HIGH. THEREFORE, THE SIGNAL BTS1 H WILL BE ASSERTED
11424 ;LOW AS A RESULT OF THE BTFET FLIP-FLOP BEING CLEARED AND THE SIGNAL
11425 ;INTER L BEING ASSERTED HIGH.

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TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11426
11427 030674 012737 000044 002342 5$: MOV #HDAL5!HDAL2,R6LOAD ;SET XSELO L LOW + XSEL1 L HIGH
11428 030702 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
11429 030706 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
11430 030710 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
11431 030710 104455 TRAP C$ERRDF
11432 030712 000004 .WORD 4
11433 030714 002605 .WORD HDALRG
11434 030716 005020 .WORD R06ERR
11435 030720 CKLOOP
11436 030720 104406 TRAP C$CLP1
11437
11438 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL BTS1 H IS READ AS A
11439 ;ZERO WHEN INTER L IS ASSERTED HIGH AND THE BTFET FLIP-FLOP IS CLEARED.
11440
11441 030722 005037 002336 6$: CLR R4GOOD ;SETUP TO EXPECT BTS1 H AS A ZERO
11442 030726 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
11443 030732 001405 BEQ 7$ ;IF OK THEN CONTINUE
11444 030734 ERRDF 3,VDALRG,R4EROR ;BTS1 H NOT A 0 - INTER L NOT SET HIGH
11445 030734 104455 TRAP C$ERRDF
11446 030736 000003 .WORD 3
11447 030740 002537 .WORD VDALRG
11448 030742 005004 .WORD R4EROR
11449 030744 CKLOOP
11450 030744 104406 TRAP C$CLP1
11451
11452 ;AT THIS POINT IN TIME, THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS
11453 ;A RESULT OF MODE REGISTER BITS 10 AND 9 BEING A ZERO, XSELO L ASSERTED
11454 ;LOW AND XSEL1 L ASSERTED HIGH.
11455
11456 ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11457 ;THE SIGNAL HDAL12 H. THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE
11458 ;SIGNAL FETCT H, WHICH SHOULD BE HIGH, INTO THE EDFET FLIP-FLOP, THUS
11459 ;SETTING THE SIGNAL EDFET H TO THE HIGH STATE. THE SIGNAL XRAS H WILL
11460 ;CLOCK THE STATE OF ADAL4 H, WHICH IS LOW, INTO THE PAUSE MODE FLIP-FLOP,
11461 ;THUS SETTING THE SIGNAL PAUSE L TO THE HIGH STATE. THE SIGNAL SOP H
11462 ;WILL BE ASSERTED HIGH WHEN PAUSE L IS ASSERTED HIGH. WHEN SOP H AND
11463 ;EDFET H ARE ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE
11464 ;DIRECT SET TO A ONE, THUS SETTING THE SIGNAL PSMW H TO THE HIGH STATE.
11465 ;THE SIGNAL PSMW H WILL BE READ IN THE VDAL REGISTER AS VDAL BIT 9.
11466
11467 ;WHEN FETCT H IS ASSERTED HIGH AND A PULSE IS ISSUED ON XRAS H, THE
11468 ;BTFET FLIP-FLOP WILL BE CLOCKED TO A ONE, THUS CAUSING THE SIGNAL
11469 ;BTFET L TO BE ASSERTED LOW. WHEN BTFET L IS ASSERTED LOW AND INTER L
11470 ;IS ASSERTED HIGH, THE SIGNAL BTS1 H WILL BE ASSERTED HIGH. THE SIGNAL
11471 ;BTS1 H WILL BE READ IN THE VDAL REGISTER AS BIT 5 WHEN ADAL10 H IS
11472 ;SET TO A ONE. ADAL10 H IS A ONE AT THE PRESENT TIME.
11473
11474 030746 004737 007272 7$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
11475
11476 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS PSMW H AND BTS1 H
11477 ;ARE ASSERTED HIGH AND THAT THEY ARE READ AS ONES IN THE VDAL REGISTER.
11478
11479 030752 052737 001040 002336 BIS #VDAL9!VDAL5,R4GOOD ;EXPECT PSMW H AND BTS1 H TO BE ONES
11480 030760 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
11481 030764 001405 BEQ 8$ ;IF OK THEN CONTINUE

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TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11482 030766          ERRDF 3,VDALRG,R4EROR          ;FETCT H PROBABLY NOT SET HIGH
11483 030766 104455  TRAP  C$ERDF
11484 030770 000003  .WORD 3
11485 030772 002537  .WORD VDALRG
11486 030774 005004  .WORD R4EROR
11487 030776          CKLOOP
11488 030776 104406  TRAP  C$CLP1
11489
11490          ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H. THE SIGNAL
11491          ;INVD L WILL CLEAR THE PAUSE STATE WORKING FLIP-FLOP AND THE BTJET
11492          ;FLIP-FLOP. WHEN BTJET FLIP-FLOP IS CLEARED, THE SIGNAL BTS1 H SHOULD
11493          ;BE ASSERTED LOW AS A RESULT OF BTJET L BEING ASSERTED HIGH AND THE
11494          ;SIGNAL INTER L BEING ASSERTED HIGH.
11495
11496 031000 012737 000004 002334 8$:  MOV  #VDAL2,R4LOAD          ;SET INVD L TO LOW STATE VIA VDAL2 H
11497 031006 004737 006640          JSR  PC,LDRDR4          ;GO LOAD, READ AND CHECK VDAL REGISTER
11498 031012 001405          BEQ  9$                ;IF OK THEN CONTINUE
11499 031014          ERRDF 3,VDALRG,R4EROR          ;BTJET F/F PROBABLY NOT CLEARED BY INVD L
11500 031014 104455  TRAP  C$ERDF
11501 031016 000003  .WORD 3
11502 031020 002537  .WORD VDALRG
11503 031022 005004  .WORD R4EROR
11504 031024          CKLOOP
11505 031024 104406  TRAP  C$CLP1
11506 031026 005037 002334 9$:  CLR  R4LOAD          ;SET INVD L BACK TO HIGH STATE
11507 031032 004737 006640          JSR  PC,LDRDR4          ;GO LOAD, READ AND CHECK VDAL REGISTER
11508 031036 001405          BEQ  10$               ;IF OK THEN CONTINUE
11509 031040          ERRDF 3,VDALRG,R4EROR          ;VDAL REGISTER NOT EQUAL EXPECTED
11510 031040 104455  TRAP  C$ERDF
11511 031042 000003  .WORD 3
11512 031044 002537  .WORD VDALRG
11513 031046 005004  .WORD R4EROR
11514 031050          CKLOOP
11515 031050 104406  TRAP  C$CLP1
11516
11517          ;AT THIS POINT IN TIME, THE SIGNAL FETCT H IS ASSERTED HIGH AS A
11518          ;RESULT OF MODE REGISTER BITS 10 AND 9 BEING CLEARED, XSELO L ASSERTED
11519          ;LOW, AND XSEL1 L ASSERTED HIGH. TO SET THE SIGNAL FETCT H TO THE
11520          ;LOW STATE, THE PROGRAM WILL SET THE SIGNAL XSEL1 L TO THE LOW STATE
11521          ;BY SETTING HDAL6 H TO A ONE.
11522
11523 031052 012737 000144 002342 10$: MOV  #HDAL6!HDAL5!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
11524 031060 004737 006672          JSR  PC,LDRDR6          ;LOAD, READ AND CHECK HDAL REGISTER
11525 031064 001405          BEQ  11$               ;IF LOADED OK THEN CONTINUE
11526 031066          ERRDF 4,HDALRG,R06ERR          ;HDAL REGISTER NOT EQUAL TO EXPECTED
11527 031066 104455  TRAP  C$ERDF
11528 031070 000004  .WORD 4
11529 031072 002605  .WORD HDALRG
11530 031074 005020  .WORD R06ERR
11531 031076          CKLOOP
11532 031076 104406  TRAP  C$CLP1
11533
11534          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING THE SIGNAL HDAL12 H.
11535          ;WHEN THE SIGNAL FETCT H IS ASSERTED LOW AND A PULSE IS ISSUED ON THE
11536          ;SIGNAL XRAS H, THE EDFET, BTJET AND PAUSE MODE FLIP-FLOPS WILL BE
11537          ;CLOCKED TO ZEROES. THE PAUSE STATE WORKING FLIP-FLOP WILL BE
  
```

TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11538                                     :CLOCKED TO A ZERO AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP
11539                                     :ALREADY BEING CLEARED, EPFN L ASSERTED HIGH, EPBN L ASSERTED HIGH AND
11540                                     :A PULSE BEING ISSUED ON THE SIGNAL RASP L. WHEN XRAS H IS PULSED THE
11541                                     :SIGNAL RASP L WILL BE PULSED.
11542
11543 031100 004737 007272                11$: JSR      PC,XRAS                      :GO PULSE XRAS H VIA HDAL12 H
11544
11545                                     :READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
11546                                     :IS NOT SET WHEN THE SIGNAL FETCT H IS ASSERTED LOW BY THE SIGNAL XSEL1 L
11547                                     :BEING ASSERTED LOW. THE SIGNAL BTS1 H SHOULD ALSO BE ASSERTED LOW AS
11548                                     :A RESULT OF THE BTFET FLIP-FLOP BEING A ZERO AND THE SIGNAL INTER L
11549                                     :BEING ASSERTED HIGH.
11550
11551 031104 004737 006654                JSR      PC,READR4                      :READ VDAL AND PAUSE STATE MACHINE
11552 031110 001405                      BEQ      12$                            :IF OK THEN CONTINUE
11553 031112                                ERRDF    3,VDALRG,R4EROR                :FETCT H PROBABLY NOT LOW BY XSEL1 L
11554 031112 104455                      TRAP     C$ERDF
11555 031114 000003                      .WORD   3
11556 031116 002537                      .WORD   VDALRG
11557 031120 005004                      .WORD   R4EROR
11558 031122                                CKLOOP
11559 031122 104406                      TRAP     C$CLP1
11560
11561                                     :SET THE SIGNAL XSEL1 L BACK TO THE HIGH STATE BY CLEARING HDAL6 H.
11562                                     :WHEN XSEL1 L IS RETURNED TO THE HIGH STATE, THE SIGNAL FETCT H SHOULD
11563                                     :BE ASSERTED HIGH.
11564
11565 031124 012737 000044 002342 12$:  MOV     #HDAL5!HDAL2,R6LOAD             :SET XSEL1 L TO HIGH STATE
11566 031132 004737 006672                JSR      PC,LDRDR6                      :GO LOAD, READ AND CHECK HDAL REGISTER
11567 031136 001405                      BEQ      13$                            :IF OK THEN CONTINUE
11568 031140                                ERRDF    4,HDALRG,R06ERR                :HDAL REGISTER NOT EQUAL EXPECTED
11569 031140 104455                      TRAP     C$ERDF
11570 031142 000004                      .WORD   4
11571 031144 002605                      .WORD   HDALRG
11572 031146 005020                      .WORD   R06ERR
11573 031150                                CKLOOP
11574 031150 104406                      TRAP     C$CLP1
11575
11576                                     :SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11577
11578 031152 004737 007006                13$: JSR      PC,SLMODR                      :SELECT MODE REG VIA GDAL BITS 2:0
11579
11580                                     :SET MODE REGISTER BIT 10 TO A ONE AND MODE REGISTER BIT 9 TO A ZERO.
11581
11582 031156 012737 002000 002342          MOV     #MR10,R6LOAD                     :SETUP BIT TO SET MR10 H TO HIGH STATE
11583 031164 004737 006672                JSR      PC,LDRDR6                      :GO LOAD, READ AND CHECK MODE REGISTER
11584 031170 001405                      BEQ      14$                            :IF LOADED OK THEN CONTINUE
11585 031172                                ERRDF    4,MODREG,R06ERR                :MODE REGISTER NOT EQUAL EXPECTED
11586 031172 104455                      TRAP     C$ERDF
11587 031174 000004                      .WORD   4
11588 031176 002631                      .WORD   MODREG
11589 031200 005020                      .WORD   R06ERR
11590 031202                                CKLOOP
11591 031202 104406                      TRAP     C$CLP1
11592
11593                                     :RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

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TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11594
11595 031204 004737 006754      14$: JSR    PC,SLHDAL          ;SELECT HDAL REG VIA GDAL BITS 2:0
11596
11597                               ;THE SIGNAL FETCT H SHOULD BE ASSERTED LOW AS THIS POINT IN TIME AS A
11598                               ;RESULT OF MODE REGISTER BIT 10 BEING SET TO A ONE, MODE REGISTER BIT 9
11599                               ;SET TO A ZERO, XSELO L BEING ASSERTED LOW, AND XSEL1 L BEING ASSERTED
11600                               ;HIGH. WHEN FETCT H IS ASSERTED LOW AND A PULSE IS ISSUED ON XRAS H,
11601                               ;THE PAUSE STATE WORKING AND BTRET FLIP-FLOPS SHOULD BE CLOCKED TO A
11602                               ;ZERO.
11603
11604 031210 012737 000044 002342  MOV    #HDAL5!HDAL2,R6LOAD      ;BITS PREVIOUSLY LOADED
11605 031216 004737 007272          JSR    PC,XRAS                  ;GO PULSE XRAS H VIA HDAL12 H
11606
11607                               ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING AND BTRET
11608                               ;FLIP-FLOPS WERE CLOCKED TO ZEROES BY XRAS H WHEN THE SIGNAL FETCT H
11609                               ;WAS ASSERTED LOW BY MODE REGISTER BIT 10 BEING A ONE.
11610
11611 031222 004737 006654          JSR    PC,READR4                ;READ VDAL AND PAUSE STATE MACHINE
11612 031226 001405          BEQ    15$                      ;IF OK THEN CONTINUE
11613 031230          ERRDF 3,VDALRG,R4ERROR      ;FETCT H PROBABLY NOT LOW BY MR10 H A 1
11614 031230 104455          TRAP  C$ERRDF
11615 031232 000003          .WORD 3
11616 031234 002537          .WORD VDALRG
11617 031236 005004          .WORD R4ERROR
11618 031240          CKLOOP
11619 031240 104406          TRAP  C$CLP1
11620
11621                               ;RESELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11622
11623 031242 004737 007006      15$: JSR    PC,SLMODR          ;SELECT MODE REGISTER VIA GDAL BITS 2:0
11624
11625                               ;SET MODE REGISTER BITS 10 AND 9 TO ONES.
11626
11627 031246 012737 003000 002342  MOV    #MR10!MR9,R6LOAD        ;SETUP BITS TO SET MR10 + MR9 TO HIGH STATE
11628 031254 004737 006672          JSR    PC,LDRDR6              ;GO LOAD, READ AND CHECK MODE REGISTER
11629 031260 001405          BEQ    16$                      ;IF LOADED OK THEN CONTINUE
11630 031262          ERRDF 4,MODREG,R06ERR      ;MODE REGISTER NOT EQUAL EXPECTED
11631 031262 104455          TRAP  C$ERRDF
11632 031264 000004          .WORD 4
11633 031266 002631          .WORD MODREG
11634 031270 005020          .WORD R06ERR
11635 031272          CKLOOP
11636 031272 104406          TRAP  C$CLP1
11637
11638                               ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11639
11640 031274 004737 006754      16$: JSR    PC,SLHDAL          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
11641
11642                               ;AT THIS POINT IN TIME, THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS A
11643                               ;RESULT OF MODE REGISTER BIT 9 BEING A ONE, XSELO L BEING ASSERTED LOW,
11644                               ;AND XSEL1 L BEING ASSERTED HIGH.
11645                               ;
11646                               ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11647                               ;THE SIGNAL HDAL12 H. WHEN FETCT H IS HIGH AND A PULSE IS ISSUED ON
11648                               ;THE SIGNAL XRAS H, THE PAUSE STATE WORKING AND BTRET FLIP-FLOPS SHOULD
11649                               ;BE SET TO ONES.

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11650
11651 031300 012737 000044 002342      MOV    #HDAL5!HDAL2,R6LOAD      ;SETUP BITS PREVIOUSLY LOADED
11652 031306 004737 007272              JSR    PC,XRAS                  ;GO PULSE XRAS H VIA HDAL12 H
11653
11654                                     ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
11655                                     ;AND THE BTRET FLIP-FLOP ARE SET TO ONES AS A RESULT OF FETCT H BEING
11656                                     ;ASSERTED HIGH AND A PULSE BEING ISSUED ON XRAS H.
11657
11658 031312 012737 001040 002336      MOV    #VDAL9!VDAL5,R4GOOD      ;EXPECT PSMW H AND BTS1 H TO BE ONES
11659 031320 004737 006654              JSR    PC,READR4                ;READ VDAL AND PAUSE STATE MACHINE
11660 031324 001405                      BEQ    17$                      ;IF OK THEN CONTINUE
11661 031326                               ERRDF  3,VDALRG,R4EROR          ;FETCT H PROBABLY NOT HIGH BY MR9 H A 1
11662 031326 104455                      TRAP   C$ERDF
11663 031330 000003                      .WORD  3
11664 031332 002537                      .WORD  VDALRG
11665 031334 005004                      .WORD  R4EROR
11666 031336                               CKLOOP
11667 031336 104406                      TRAP   C$CLP1
11668
11669                                     ;PULSE INVD L VIA VDAL2 H TO CLEAR THE PAUSE STATE WORKING AND BTRET
11670                                     ;FLIP-FLOPS.
11671
11672 031340 005037 002334      17$:  CLR    R4LOAD                  ;SETUP TO EXPECT ALL ZEROES ON READBACK
11673 031344 004737 007712              JSR    PC,CLRPSM                ;PULSE INVD L VIA VDAL2 H
11674
11675                                     ;RESELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11676
11677 031350 004737 007006      JSR    PC,SLMODR                ;SELECT MODE REG VIA GDAL BITS 2:0
11678
11679                                     ;CLEAR MODE REGISTER BIT9 AND LEAVE MODE REGISTER BIT 10 SET TO A ONE.
11680
11681 031354 012737 002000 002342      MOV    #MR10,R6LOAD             ;SETUP BIT TO BE LOADED
11682 031362 004737 006672              JSR    PC,LDRDR6                ;GO LOAD, READ AND CHECK MDOE REGISTER
11683 031366 001405                      BEQ    18$                      ;IF LOADED OK THEN CONTINUE
11684 031370                               ERRDF  4,MODREG,R06ERR          ;MODE REGISTER NOT EQUAL EXPECTED
11685 031370 104455                      TRAP   C$ERDF
11686 031372 000004                      .WORD  4
11687 031374 002631                      .WORD  MODREG
11688 031376 005020                      .WORD  R06ERR
11689 031400                               CKLCOP
11690 031400 104406                      TRAP   C$CLP1
11691
11692                                     ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11693
11694 031402 004737 006754      18$:  JSR    PC,SLHDAL                ;SELECT HDAL REG VIA GDAL BITS 2:0
11695
11696                                     ;SET XSELO L TO THE HIGH STATE BY CLEARING HDAL5 H.
11697
11698 031406 012737 000004 002342      MOV    #HDAL2,R6LOAD             ;SETUP TO SET XSELO L TO HIGH STATE
11699 031414 004737 006672              JSR    PC,LDRDR6                ;GO LOAD, READ AND CHECK HDAL REGISTER
11700 031420 001405                      BEQ    19$                      ;IF OK THEN CONTINUE
11701 031422                               ERRDF  4,HDALRG,R06ERR          ;HDAL REGISTER NOT EQUAL EXPECTED
11702 031422 104455                      TRAP   C$ERDF
11703 031424 000004                      .WORD  4
11704 031426 002605                      .WORD  HDALRG
11705 031430 005020                      .WORD  R06ERR

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TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'

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11706 031432          CKLOOP
11707 031432 104406  TRAP   C$CLP1
11708
11709
11710                ;AT THIS POINT IN TIME THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS A
11711                ;RESULT OF MODE REGISTER BIT 9 BEING A ZERO, MODE REGISTER BIT 10 BEING
11712                ;A ONE, XSELO L ASSERTED HIGH AND EIAIO L BEING ASSERTED LOW. EIAIO L
11713                ;IS ASSERTED LOW AS A RESULT OF CAIO H BEING PULLED UP AND NO BUFFERS
11714                ;DRIVING THE CAI BUS.
11715                ;
11716                ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11717                ;HDAL12 H. WHEN FETCT H IS ASSERTED HIGH AND A PULSE IS ISSUED ON THE
11718                ;SIGNAL XRAS H, THE PAUSE STATE WORKING FLIP-FLOP AND THE BTFET FLIP-
11719                ;FLOP WILL BE SET TO ONES.
11720 031434 004737 007272      19$: JSR    PC,XRAS          ;GO PULSE XRAS H VIA HDAL12 H
11721
11722                ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING AND BTFET
11723                ;FLIP-FLOPS WERE SET TO ONES AS A RESULT OF FETCT H BEING ASSERTED HIGH
11724                ;AND A PULSE BEING ISSUED ON XRAS H.
11725
11726 031440 012737 001040 002336  MOV    #VDAL9!VDALS,R4GOOD. ;EXPECT PSMW H AND BTS1 H TO BE SET
11727 031446 004737 006654          JSR    PC,READR4          ;READ VDAL AND PAUSE STATE MACHINE
11728 031452 001405          BEQ    20$              ;IF OK THEN CONTINUE
11729 031454          ERRDF  3,VDALRG,R4EROR ;FETCT H PROBABLY NOT SET HIGH
11730 031454 104455          TRAP   C$ERDF
11731 031456 000003          .WORD  3
11732 031460 002537          .WORD  VDALRG
11733 031462 005004          .WORD  R4EROR
11734 031464          CKLOOP
11735 031464 104406          TRAP   C$CLP1
11736
11737                ;PULSE INVDL VIA VDAL2 H TO CLEAR THE PAUSE STATE WORKING AND BTFET
11738                ;FLIP-FLOPS.
11739
11740 031466 005037 002334      20$: CLR    R4LOAD          ;SETUP TO EXPECT ALL ZEROES
11741 031472 004737 007712          JSR    PC,CLRPSM        ;GO PULSE INVD L VIA VDAL2 H
11742
11743                ENDSEG
11744 031476          10000$:
11745 031476 104405          TRAP   C$ESEG
11746 031500          ENDTST
11747 031500          L10073:
11748 031500 104401          TRAP   C$ETST
11749

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

.SBTTL TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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:++
: THIS TEST WILL CHECK THAT THE SIGNAL EDEOC H CAN BE SET TO THE HIGH STATE AND
: TO THE LOW STATE. THE SIGNAL EDEOC H IS READ IN THE VDAL REGISTER ON BIT 4
: WHEN ADAL REGISTER BIT 10 IS SET TO A ONE. THE PROGRAM WILL CHECK THE SIGNAL
: EDEOC H TO SET AND CLEAR BY CHANGING THE LOGIC LEVEL ON THE FOLLOWING SIGNALS:
: ADAL9 H, PSM L, INTER L, REFR L, XRAS H, XRAS L, XCAS H, XCAS L AND SOP L.
: THE TEST WILL USE THE SIGNAL EDEOC H TO CHECK THAT THE REFR FLIP-FLOP CAN BE
: SET AND CLEARED. THE REFR FLIP-FLOP WILL BE CHECKED TO BE CLEARED BY CHANGING
: THE LOGIC LEVELS ON THE SIGNALS ADAL7 H AND XCAS H. THE REFR FLIP-FLOP CAN
: NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INVDL BECAUSE OF THE LOGIC DESIGN.
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031502
 031502
 031502 004737 005510
 031506 104404
 031510 004737 006754
 031514 012737 000004 002342
 031522 004737 006672
 031526 001405
 031530
 031530 104455
 031532 000004
 031534 002605
 031536 005020
 031540
 031540 104406
 031542 012737 002000 002330 1\$:
 031550 004737 006614
 031554 001405
 031556
 031556 104455
 031560 000002
 031562 002513
 031564 004770
 031566
 031566 104406

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T42:: BGNTST
JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR
BGNSEG
TRAP C$BSEG

;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
JSR PC,SLHDL ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

;SET HDAL2 H TO A ONE IN THE HDAL REGISTER. WHEN HDAL2 H IS SET TO A
;ONE, THE PROGRAM HAS CONTROL OF THE T-11 TIMING AND CONTROL SIGNALS
MOV #HDAL2,R6LOAD ;SETUP BIT TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL TO EXPECTED
TRAP C$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLOOP
TRAP C$CLP1

;SET ADAL REGISTER BIT 10 TO A ONE AND ALL OTHER ADAL REGISTER BITS TO
;A ZERO. ADAL10 H ON A ONE WILL ENABLE THE SIGNAL EDEOC H TO VDAL
;REGISTER BIT 4. ADAL4 H ON A ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP
;TO BE CLOCKED TO THE PAUSE MODE WHEN XRAS H IS PULSED. ADAL9 H ON
;A ZERO WILL CAUSE THE ENCLK FLIP-FLOP TO BE CLOCKED TO A ZERO WHEN
;EITHER XRAS L OR XCAS L ARE PULSED
MOV #ADAL10,R2LOAD ;SETUP BIT TO BE LOADED
JSR PC,LDRDR2 ;LOAD, READ AND CHECK ADAL REGISTER
BEQ 2$ ;IF LOADED OK THEN CONTINUE
ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 2
.WORD ADALRG
.WORD R2EROR
CKLOOP
TRAP C$CLP1
  
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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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11806 ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 2.
11807 ;WHEN INVD L IS PULSED, THE PAUSE STATE MACHINE FLIP-FLOPS, THE REFR
11808 ;FLIP-FLOP, THE EDFET FLIP-FLOP, THE ENCLK AND ENEDC FLIP-FLOPS WILL BE
11809 ;CLEARED. THE PAUSE MODE FLIP-FLOP AND THE SINGLE STEP SYNC FLIP-FLOPS
11810 ;WILL BE PRESET TO A ONE VIA INVD L THUS SETTING THE SIGNAL PAUSE L
11811 ;TO THE LOW STATE AND PSM L TO THE HIGH STATE. THE SIGNAL FETCT H WILL
11812 ;BE ASSERTED HIGH BY SETTING VDAL7 H TO A ONE. WHEN XRAS H IS PULSED
11813 ;LATER ON IN THIS TEST, THE EDFET FLIP-FLOP WILL BE CLOCKED TO A ONE
11814 ;AS A RESULT OF FETCT H BEING ASSERTED HIGH. THE SIGNAL EDEOC H SHOULD
11815 ;BE READ AS A ZERO AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED
11816 ;AS LISTED.
11817 : INTER L - HIGH
11818 : REFR L - HIGH
11819 : XRAS H - LOW
11820 : XCAS L - HIGH
11821 : CYCLE L - HIGH
11822 : ADAL9 H - LOW
11823 : ENCLK H - LOW
11824 : ENEDC H - LOW
11825 : PSM L - HIGH
11826 : SOP L - HIGH
11827
11828 031570 012737 000200 002334 2$: MOV #VDAL7,R4LOAD ;SETUP BIT TO SET FETCT H HIGH
11829 031576 004737 007712 JSR PC,CLRPSM ;SET FETCT H HIGH AND PULSE INVD L
11830
11831 ;TOGGLE THE SIGNAL XCAS L TO CLOCK THE STATE OF ADAL9 H INTO THE ENCLK
11832 ;FLIP-FLOP, TO CLOCK THE STATE OF THE PSMW FLIP-FLOP INTO THE PSM FLIP-
11833 ;FLOP AND TO CAUSE THE CYCLE ONE SHOT TO BE FIRED WHICH WILL CAUSE THE
11834 ;STATE OF ENCLK FLIP-FLOP TO BE CLOCKED INTO THE ENEDC FLIP-FLOP. ALL
11835 ;THESE FLIP-FLOPS SHOULD BE CLOCKED TO A ZERO.
11836
11837 031602 004737 007376 JSR PC,XCAS ;PULSE XCAS H AND XCAS L VIA HDAL13 H
11838
11839 ;READ THE VDAL REGISTER TO CHECK THAT NO CHANGES OCCURED SINCE THE
11840 ;LAST CHECK OF THE VDAL REGISTER ABOVE.
11841
11842 031606 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL REGISTER
11843 031612 001405 BEQ 3$ ;IF NO CHANGE THEN CONTINUE
11844 031614 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
11845 031614 104455 TRAP C$ERDF
11846 031616 000003 .WORD 3
11847 031620 002537 .WORD VDALRG
11848 031622 005004 .WORD R4EROR
11849 031624 CKLOOP
11850 031624 104406 TRAP C$CLP1
11851
11852 ;SET ADAL REGISTER BIT 9 TO A ONE. WHEN ADAL9 H IS SET TO A ONE AND
11853 ;A PULSE IS ISSUED ON XRAS L OR XCAS L, THE ENCLK FLIP-FLOP WILL BE
11854 ;SET TO A ONE.
11855
11856 031626 052737 001000 002330 3$: BIS #ADAL9,R2LOAD ;SETUP BIT TO BE LOADED
11857 031634 004737 006614 JSR PC,LDRDR2 ;LOAD, READ AND CHECK ADLA REGISTER
11858 031640 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
11859 031642 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
11860 031642 104455 TRAP C$ERDF
11861 031644 000002 .WORD 2

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11862 031646 002513          .WORD  ADALRG
11863 031650 004770          .WORD  R2EROR
11864 031652                CKLOOP
11865 031652 104406          TRAP   C$CLP1
11866
11867                          ;TOGGLE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
11868                          ;A PULSE ON XCAS H WILL CLOCK THE OUTPUT OF THE PSMW FLIP-FLOP INTO THE
11869                          ;PSM FLIP-FLOP THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE. A PULSE
11870                          ;ON XCAS L WILL CLOCK THE LEVEL OF ADAL9 H INTO THE ENCLK FLIP-FLOP THUS
11871                          ;CLOCKING THAT FLIP-FLOP TO A ONE. A PULSE ON XCAS L WILL CAUSE A PULSE
11872                          ;ON THE SIGNAL CYCLE L WHICH WILL CAUSE THE CYCLE ONE SHOT TO BE FIRED.
11873                          ;WHEN THE CYCLE ONE SHOT IS FIRED, THE STATE OF THE ENCLK FLIP-FLOP WILL
11874                          ;BE CLOCKED INTO THE ENEDC FLIP-FLOP THUS SETTING THE SIGNAL ENEDC H
11875                          ;TO THE HIGH STATE.
11876
11877 031654 004737 007376      4$:  JSR    PC,XCAS                ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
11878
11879                          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A
11880                          ;ONE AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED AS LISTED.
11881                          :      INTER L  - HIGH
11882                          :      REFR L   - HIGH
11883                          :      XRAS H   - LOW
11884                          :      XCAS L   - HIGH
11885                          :      CYCLE L  - HIGH
11886                          :      ADAL9 H  - HIGH
11887                          :      ENCLK H  - HIGH
11888                          :      ENEDC H  - HIGH
11889                          :      PSM L    - HIGH
11890                          :      SOP L    - HIGH
11891
11892 031660 052737 000020 002336  BIS    #VDAL4,R4GOOD          ;EXPECT EDEOC H TO BE A ONE
11893 031666 004737 006654          JSR    PC,READR4            ;READ AND CHECK VDAL REGISTER
11894 031672 001405          BEQ    $$                  ;IF OK THEN CONTINUE
11895 031674                ERRDF  3,VDALRG,R4EROR          ;EDEOC H PROBABLY NOT SET
11896 031674 104455          TRAP  C$ERDF
11897 031676 000003          .WORD  3
11898 031700 002537          .WORD  VDALRG
11899 031702 005004          .WORD  R4EROR
11900 031704                CKLOOP
11901 031704 104406          TRAP  C$CLP1
11902
11903                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. A PULSE
11904                          ;ON XRAS H WILL CLOCK THE PAUSE MODE FLIP-FLOP TO A ZERO THUS SETTING
11905                          ;THE SIGNALS PAUSE L AND SOP H TO THE HIGH STATES. A PULSE ON XRAS H
11906                          ;WILL ALSO CLOCK THE EDFET AND BTFET FLIP-FLOPS TO ONES AS A RESULT OF
11907                          ;FETCT H BEING ASSERTED HIGH. WHEN THE VDAL REGISTER IS READ THE
11908                          ;SIGNALS PSMW H AND BTS1 H SHOULD BE READ AS ONES AS A RESULT OF THE
11909                          ;PAUSE STATE WORKING AND BTFET FLIP-FLOPS BEING SET TO ONES.
11910
11911 031706 004737 007272      5$:  JSR    PC,XRAS                ;GO PULSE XRAS H VIA HDAL12 H
11912
11913                          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H WENT TO A
11914                          ;ZERO AS A RESULT OF SOP L BEING ASSERTED LOW. THE FOLLOWING SIGNALS
11915                          ;SHOULD BE ASSERTED AS LISTED. WHEN THE VDAL REGISTER IS READ, THE
11916                          ;SIGNALS PSMW H AND BTS1 H SHOULD BE READ AS ONES AS A RESULT OF THE
11917                          ;PAUSE STATE WORKING AND BTFET FLIP-FLOPS BEING SET TO ONES.

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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11918 : INTER L - HIGH
11919 : REFR L - HIGH
11920 : XRAS H - LOW
11921 : XCAS L - HIGH
11922 : CYCLE L - HIGH
11923 : ADAL9 H - HIGH
11924 : ENCLK H - HIGH
11925 : ENEDC H - HIGH
11926 : PSM L - HIGH
11927 : SOP L - LOW
11928 :
11929 031712 052737 001040 002336 BIS #VDAL9!VDAL5,R4GOOD ;EXPECT PSMW H TO BE A ONE
11930 031720 042737 000020 002336 BIC #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ZERO
11931 031726 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL REGISTER
11932 031732 001405 BEQ 6$ ;IF OK THEN CONTINUE
11933 031734 ERRDF 3,VDALRG,R4EROR ;SOP L PROBABLY FAILED TO 0 EDEOC H
11934 031734 104455 TRAP C$ERDF
11935 031736 000003 .WORD 3
11936 031740 002537 .WORD VDALRG
11937 031742 005004 .WORD R4EROR
11938 031744 CKLOOP
11939 031744 104406 TRAP C$CLP1
11940
11941 :SET ADAL REGISTER BIT 4 TO A ONE. WHEN XRAS H IS PULSED, THE PAUSE
11942 :MODE FLIP-FLOP WILL BE CLOCKED TO RUN MODE THUS SETTING THE SIGNALS
11943 :PAUSE L AND SOP H TO THE LOW STATE. THE SIGNAL SOP L WILL BE ASSERTED
11944 :TO THE HIGH STATE.
11945
11946 031746 052737 000020 002330 6$: BIS #ADAL4,R2LOAD ;SETUP BIT TO BE LOADED
11947 031754 004737 006614 JSR PC,LDRDR2 ;LOAD, READ AND CHECK ADAL REGISTER
11948 031760 001405 BEQ 7$ ;IF LOADED OK THEN CONTINUE
11949 031762 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
11950 031762 104455 TRAP C$ERDF
11951 031764 000002 .WORD 2
11952 031766 002513 .WORD ADALRG
11953 031770 004770 .WORD R2EROR
11954 031772 CKLOOP
11955 031772 104406 TRAP C$CLP1
11956
11957 :SET THE SIGNAL FETCT H TO THE LOW STATE AND CHECK THAT NO CHANGES HAVE
11958 :OCCURED IN THE VDAL REGISTER. NO CHANGES SHOULD OCCUR UNTIL XRAS H IS
11959 :PULSED AGAIN.
11960
11961 031774 042737 000200 002334 7$: BIC #VDAL7,R4LOAD ;SETUP BIT TO CLEAR FETCT H
11962 032002 042737 000200 002336 BIC #VDAL7,R4GOOD ;EXPECT FETCT H TO BE A 0 ON A READ
11963 032010 004737 006646 JSR PC,LDRD4R ;LOAD, READ AND CHECK VDAL REGISTER
11964 032014 001405 BEQ 8$ ;IF OK THEN CONTINUE
11965 032016 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
11966 032016 104455 TRAP C$ERDF
11967 032020 000003 .WORD 3
11968 032022 002537 .WORD VDALRG
11969 032024 005004 .WORD R4EROR
11970 032026 CKLOOP
11971 032026 104406 TRAP C$CLP1
11972
11973 :PULSE THE SIGNAL XRAS H TO SET THE SIGNAL PAUSE L TO THE LOW STATE AND

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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11974                                     :THE SIGNAL SOP L TO THE HIGH STATE.  THE SIGNALS EDFET H AND BTFET H
11975                                     :WILL BE CLOCKED TO A LOW STATE AS A RESULT OF THE SIGNAL FETCT H BEING
11976                                     :ASSERTED LOW AND A PULSE BEING ISSUED ON THE SIGNAL XRAS H.
11977
11978 032030 004737 007272                8$:  JSR      PC,XRAS                                :GO PULSE XRAS H VIA HDAL12 H
11979
11980                                     :READ THE VDAL REGISTER AND CHECK THE THE SIGNAL EDEOC H IS SET TO A
11981 :ONE AS A RESULT OF THE FOLLOWING SIGNALS BEING SET TO THE STATES LISTED
11982 :
11983 :   INTER L - HIGH
11984 :   REFR L  - HIGH
11985 :   XRAS H  - LOW
11986 :   XCAS L  - HIGH
11987 :   CYCLE L - HIGH
11988 :   ADAL9 H - HIGH
11989 :   ENCLK H - HIGH
11990 :   ENEDC H - HIGH
11991 :   PSM L   - HIGH
11992 :   SOP L   - HIGH
11993 032034 052737 000020 002336        BIS      #VDAL4,R4GOOD                :EXPECT EDEOC h TO BE SET TO A ONE
11994 032042 042737 000040 002336        BIC      #VDAL5,R4GOOD                :EXPECT BTST H TO BE A ZERO
11995 032050 004737 006654                JSR      PC,READR4                    :READ AND CHECK VDAL REGISTER
11996 032054 001405                BEQ      9$                            :IF OK THEN CONTINUE
11997 032056                                ERRDF    3,VDALRG,R4EROR              :EDEOC H PROBABLY NOT SET TO A ONE
11998 032056 104455                TRAP    C$ERDF
11999 032060 000003                .WORD   3
12000 032062 002537                .WORD   VDALRG
12001 032064 005004                .WORD   R4EROR
12002 032066                                CKLOOP
12003 032066 104406                TRAP    C$CLP1
12004
12005                                     :PULSE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
12006 :A PULSE ON XCAS H WILL CLOCK THE PSM FLIP-FLOP TO A ZERO AS A RESULT
12007 :OF THE PSMW FLIP-FLOP BEING SET TO A ONE.  THE ENEDC FLIP-FLOP WILL
12008 :AGAIN BE CLOCKED TO A ONE AS A RESULT OF XCAS L BEING PULSED AND
12009 :ADAL9 H BEING SET TO A ONE.
12010
12011 032070 004737 007376                9$:  JSR      PC,XCAS                                :GO PULSE XCAS H AND XCAS L VIA HDAL13 H
12012
12013                                     :CHECK EDEOC H TO BE A ZERO AS A RESULT OF THE PSM FLIP-FLOP BEING
12014 :CLEARED.  TEH FOLLOWING SIGNALS SHOULD BE ASSERTED IN THE STATES AS
12015 :LISTED BELOW.
12016 :
12017 :   INTER L - HIGH
12018 :   REFR L  - HIGH
12019 :   XRAS H  - LOW
12020 :   XCAS L  - HIGH
12021 :   CYCLE L - HIGH
12022 :   ADAL9 H - HIGH
12023 :   ENCLK H - HIGH
12024 :   ENEDC H - HIGH
12025 :   PSM L   - LOW
12026 :   SOP L   - HIGH
12027 032074 042737 000020 002336        BIC      #VDAL4,R4GOOD                :EXPECT EDEOC H TO BE A ZERO
12028 032102 004737 006654                JSR      PC,READR4                    :READ AND CHECK VDAL REGISTER
12029 032106 001405                BEQ      10$                           :IF OK THEN CONTINUE

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

```

12030 032110 ERRDF 3,VDALRG,R4EROR ;PSM L PROBABLY NOT ASSERTED LOW
12031 032110 104455 TRAP C$ERDF
12032 032112 000003 .WORD 3
12033 032114 002537 .WORD VDALRG
12034 032116 005004 .WORD R4EROR
12035 032120 CKLOOP
12036 032120 104406 TRAP C$CLP1
12037
12038 ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 2.
12039 ;A PULSE ON INVD L WILL CLEAR ALL THE PAUSE STATE MACHINE FLIP-FLOPS.
12040 ;THE EDFET FLIP-FLOP, THE ENCLK AND ENEDC FLIP-FLOPS. THE PAUSE
12041 ;AND PSM FLIP-FLOPS WILL BE PRESET TO A ONE THUS SETTING THE SIGNALS
12042 ;PAUSE L TO THE LOW STATE AND PSM L TO THE HIGH STATE.
12043
12044 032122 005037 002334 10$: CLR R4LOAD ;SETUP TO CLEAR ALL R/W BITS
12045 032126 004737 007712 JSR PC,CLRPSM ;GO PULSE INVD L VIA VDAL2 H
12046
12047 ;PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THE PAUSE
12048 ;MODE FLIP-FLOP WILL BE SET TO RUN MODE AS A RESULT OF ADAL4 H BEING
12049 ;ASSERTED HIGH. THE ENCLK FLIP-FLOP WILL BE CLOCKED TO A ONE AS A
12050 ;RESULT OF ADAL9 H BEING ASSERTED HIGH.
12051
12052 032132 004737 007272 JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
12053
12054 ;READ VDAL REGISTER TO CHECK THAT EDEOC H IS STILL A ZERO AFTER
12055 ;PULSING XRAS H, THE FOLLOWING SIGNALS SHOULD BE ASSERTED AS LISTED
12056 : INTER L - HIGH
12057 : REFR L - HIGH
12058 : XRAS H - LOW
12059 : XCAS L - HIGH
12060 : CYCLE L - HIGH
12061 : ADAL9 H - HIGH
12062 : ENCLK H - HIGH
12063 : ENEDC H - LOW
12064 : PSM L - HIGH
12065 : SOP L - HIGH
12066
12067 032136 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL REGISTER
12068 032142 001405 BEQ 11$ ;IF OK THEN CONTINUE
12069 032144 ERRDF 3,VDALRG,R4EROR ;INVD L PROBABLY NOT O'ED ENEDC F/F
12070 032144 104455 TRAP C$ERDF
12071 032146 000003 .WORD 3
12072 032150 002537 .WORD VDALRG
12073 032152 005004 .WORD R4EROR
12074 032154 CKLOOP
12075 032154 104406 TRAP C$CLP1
12076
12077 ;PULSE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
12078 ;A PULSE ON XCAS H WILL CLOCK THE PSM FLIP-FLOP TO A ONE AND A PULSE ON
12079 ;XCAS L WILL CLOCK THE ENEDC FLIP-FLOP TO A ONE.
12080
12081 032156 004737 007376 11$: JSR PC,XCAS ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
12082
12083 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H WAS SET TO A
12084 ;ONE AS A RESULT OF ENEDC FLIP-FLOP BEING SET TO A ONE. THE FOLLOWING SIGNALS
12085 ;SHOULD BE ASSERTED AS LISTED BELOW

```

TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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12086 : INTER L - HIGH
12087 : REFR L - HIGH
12088 : XRAS H - LOW
12089 : XCAS L - HIGH
12090 : CYCLE L - HIGH
12091 : ADAL9 H - HIGH
12092 : ENCLK H - HIGH
12093 : ENEDC H - HIGH
12094 : PSM L - HIGH
12095 : SOP L - HIGH
12096
12097 032162 052737 000020 002336 BIS #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE ASSERTED
12098 032170 004737 006654 JSR PC,READR4 ;READ AND CHECK VDAL REGISTER
12099 032174 001405 BEQ 12$ ;IF OK THEN CONTINUE
12100 032176 104455 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
12101 032176 000003 TRAP C$ERDF
12102 032200 002537 .WORD 3
12103 032202 005004 .WORD VDALRG
12104 032204 005004 .WORD R4EROR
12105 032206 CKLOOP
12106 032206 104406 TRAP C$CLP1
12107
12108 ;SET THE SIGNALS XCAS H AND XCAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12109 ;BY SETTING HDAL13 H TO A ONE. XCAS H BEING SET HIGH WILL CLOCK THE
12110 ;SINGLE STEP SYNC FLIP-FLOP TO A ONE THUS SETTING THE SIGNAL PSM L TO
12111 ;THE HIGH STATE.
12112
12113 032210 004737 007410 12$: JSR PC,XCASH ;SET XCAS H HIGH AND XCAS L LOW
12114
12115 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12116 ;THE SIGNALS BELOW BEING IN THE FOLLOWING STATE.
12117 : INTER L - HIGH
12118 : REFR L - HIGH
12119 : XRAS H - LOW
12120 : XCAS L - LOW
12121 : ENEDC H - HIGH
12122 : PSM L - HIGH
12123 : SOP L - HIGH
12124
12125 032214 042737 000020 002336 BIC #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ZERO
12126 032222 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12127 032226 001405 BEQ 13$ ;IF OK THEN CONTINUE
12128 032230 104455 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
12129 032230 000003 TRAP C$ERDF
12130 032232 002537 .WORD 3
12131 032234 005004 .WORD VDALRG
12132 032236 005004 .WORD R4EROR
12133 032240 CKLOOP
12134 032240 104406 TRAP C$CLP1
12135
12136 ;SET THE SIGNALS XCAS H AND XCAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12137 ;BY CLEARING HDAL13 H IN THE HDAL REGISTER.
12138
12139 032242 004737 007442 13$: JSR PC,XCASL ;SET XCAS H LOW AND XCAS L HIGH
12140
12141 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

```
12142 ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12143 : INTER L - HIGH
12144 : REFR L - HIGH
12145 : XRAS H - LOW
12146 : XCAS L - HIGH
12147 : ENEDC H - HIGH
12148 : PSM L - HIGH
12149 : SOP L - HIGH
12150
12151 032246 052737 000020 002336 BIS #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
12152 032254 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12153 032260 001405 BEQ 14$ ;IF OK THEN CONTINUE
12154 032262 ERRDF 3,VDALRG,R4EROR ;EDEOC H PROBABLY NOT SET HIGH
12155 032262 104455 TRAP C$ERDF
12156 032264 000003 .WORD 3
12157 032266 002537 .WORD VDALRG
12158 032270 005004 .WORD R4EROR
12159 032272 CKLOOP
12160 032272 104406 TRAP C$CLP1
12161
12162 ;SET THE SIGNAL XRAS H TO THE HIGH STATE BY SETTING HDAL12 H TO A ONE.
12163 ;WHEN ADAL7 H IS A ZERO, THE REFR FLIP-FLOP WILL BE HELD TO THE
12164 ;CLEARED STATE AND WILL NOT BE CLOCKED TO A ONE BY XRAS L WHEN THE
12165 ;SIGNAL INTER L IS ASSERTED HIGH. THEREFORE THE SIGNAL REFR L WILL
12166 ;REMAIN ASSERTED HIGH.
12167
12168 032274 004737 007304 14$: JSR PC,XRASH ;SET XRAS H HIGH AND XRAS L LOW
12169
12170 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12171 ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12172 : INTER L - HIGH
12173 : REFR L - HIGH
12174 : XRAS H - HIGH
12175 : XCAS L - HIGH
12176 : ADAL9 H - HIGH
12177 : PSM L - HIGH
12178 : SOP L - HIGH
12179
12180 032300 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12181 032304 001405 BEQ 15$ ;IF OK THEN CONTINUE
12182 032306 ERRDF 3,VDALRG,R4EROR ;EDEOC H PROBABLY ASSERTED LOW
12183 032306 104455 TRAP C$ERDF
12184 032310 000003 .WORD 3
12185 032312 002537 .WORD VDALRG
12186 032314 005004 .WORD R4EROR
12187 032316 CKLOOP
12188 032316 104406 TRAP C$CLP1
12189
12190 ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
12191 ;LOW STATE. XSEL1 L WILL BE SET LOW BY SETTING HDAL6 H TO A ONE.
12192
12193 032320 052737 000100 002342 15$: BIS #HDAL6,R6LOAD ;SET XSEL1 L TO THE LOW STATE
12194 032326 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
12195 032332 001405 BEQ 16$ ;IF LOADED OK THEN CONTINUE
12196 032334 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
12197 032334 104455 TRAP C$ERDF
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12198 032336 000004 .WORD 4
12199 032340 002605 .WORD HDALRG
12200 032342 005020 .WORD R06ERR
12201 032344 CKLOOP
12202 032344 104406 TRAP C$CLP1
12203
12204 ;CHECK THE SIGNAL BTS1 H TO BE SET TO A ONE AS A RESULT OF THE BTJET
12205 ;FLIP-FLOP BEING CLEARED AND THE SIGNAL INTER L BEING ASSERTED LOW.
12206 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12207 ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12208 :
12209 : INTER L - LOW
12210 : REFR L - HIGH
12211 : XRAS H - HIGH
12212 : XCAS L - HIGH
12213 : ENEDC H - HIGH
12214 : PSM L - HIGH
12215 : SOP L - HIGH
12216 032346 052737 000040 002336 16$: BIS #VDAL5,R4GOOD ;EXPECT BTS1 H TO BE A ONE VIA INTER L
12217 032354 042737 000020 002336 BIC #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ZERO
12218 032362 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12219 032366 001405 BEQ 17$ ;IF OK THEN CONTINUE
12220 032370 ERRDF 3,VDALRG,R4EROR ;EDEOC H NOT 0 WHEN INTER L SET LOW
12221 032370 104455 TRAP C$ERDF
12222 032372 000003 .WORD 3
12223 032374 002537 .WORD VDALRG
12224 032376 005004 .WORD R4EROR
12225 032400 CKLOOP
12226 032400 104406 TRAP C$CLP1
12227
12228 ;SET THE SIGNAL XRAS H TO THE LOW STATE BY CLEARING HDAL12 H.
12229
12230 032402 004737 007336 17$: JSR PC,XRASL ;SET XRAS H TO THE LOW STATE
12231
12232 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12233 ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12234 :
12235 : INTER L - LOW
12236 : REFR L - HIGH
12237 : XRAS H - LOW
12238 : XCAS L - HIGH
12239 : ENEDC H - HIGH
12240 : PSM L - HIGH
12241 : SOP L - HIGH
12242 032406 052737 000020 002336 BIS #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ONE
12243 032414 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12244 032420 001405 BEQ 18$ ;IF OK THEN CONTINUE
12245 032422 ERRDF 3,VDALRG,R4EROR ;EDEOC H NOT 1 WHEN XRAS H SET LOW
12246 032422 104455 TRAP C$ERDF
12247 032424 000003 .WORD 3
12248 032426 002537 .WORD VDALRG
12249 032430 005004 .WORD R4EROR
12250 032432 CKLOOP
12251 032432 104406 TRAP C$CLP1
12252
12253 ;SET THE SIGNAL INTER L BACK TO THE HIGH STATE BY SETTING XSEL1 L HIGH.

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12254                                     :XSEL1 L IS SET HIGH BY CLEARING HDAL6 H IN THE HDAL REGISTER.
12255
12256 032434 042737 000100 002342 18$: BIC #HDAL6,R6LOAD ;SETUP TO SET XSEL1 L TO HIGH STATE
12257 032442 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
12258 032446 001405 BEQ 19$ ;IF LOADED OK TEHN CONTINUE
12259 032450 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
12260 032450 104455 TRAP C$ERDF
12261 032452 000004 .WORD 4
12262 032454 002605 .WORD HDALRG
12263 032456 005020 .WORD R06ERR
12264 032460 CKLOOP
12265 032460 104406 TRAP C$CLP1
12266
12267                                     :CHECK THE SIGNAL BTS1 H TO BE A ZERO AS A RESULT OF THE BTJET FLIP-FLOP
12268                                     :BEING CLEARED AND THE SIGNAL INTER L BEING SET TO THE HIGH STATE.
12269
12270                                     :READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12271                                     :THE FOLLOWING SIGNALS BEING SET AS LISTED BELOW.
12272                                     :
12273                                     : INTER L - HIGH
12274                                     : REFR L - HIGH
12275                                     : XRAS H - LOW
12276                                     : XCAS L - HIGH
12277                                     : ENEDC H - HIGH
12278                                     : PSM L - HIGH
12279                                     : SOP L - HIGH
12280 032462 042737 000040 002336 19$: BIC #VDAL5,R4GOOD ;EXPECT BTS1 H TO BE A 0 VIA INTER L
12281 032470 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12282 032474 001405 BEQ 20$ ;IF OK THEN CONTINUE
12283 032476 ERRDF 3,VDALRG,R4EROR ;EDEOC H NOT A ONE WHEN INTER L HIGH
12284 032476 104455 TRAP C$ERDF
12285 032500 000003 .WORD 3
12286 032502 002537 .WORD VDALRG
12287 032504 005004 .WORD R4EROR
12288 032506 CKLOOP
12289 032506 104406 TRAP C$CLP1
12290
12291                                     :SET THE SIGNAL ADAL7 H TO A ONE. WHEN ADAL7 H IS A ONE, THE REFR FLIP-
12292                                     :FLOP CAN BE CLEARED EITHER BY XCAS H BEING SET HIGH, OR INVD L BEING
12293                                     :SET LOW, OR BY ADAL7 H BEING SET BACK TO A ZERO. THE REFR FLIP-FLOP
12294                                     :CAN NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INVD L BECAUSE OF THE
12295                                     :LOGIC DESIGN.
12296
12297 032510 052737 000200 002330 20$: BIS #ADAL7,R2LOAD ;SETUP BIT TO BE LOADED
12298 032516 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
12299 032522 001405 BEQ 21$ ;IF OK THEN CONTINUE
12300 032524 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
12301 032524 104455 TRAP C$ERDF
12302 032526 000002 .WORD 2
12303 032530 002513 .WORD ADALRG
12304 032532 004770 .WORD R2EROR
12305 032534 CKLOOP
12306 032534 104406 TRAP C$CLP1
12307
12308                                     :SET THE SIGNALS XRAS H AND XRAS L TO THE HIGH AND LOW STATES RESPECTIVELY
12309                                     :BY SETTING HDAL12 H TO A ONE. SETTING XRAS L TO THE LOW STATE WILL

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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12310                                     :CLOCK THE LEVEL OF INTER L, WHICH IS HIGH, INTO THE REFR FLIP-FLOP,
12311                                     :THUS CLOCKING THE FLIP-F OP TO A ONE.  WHEN THE REFR FLIP-FLOP IS
12312                                     :SET TO A ONE, THE SIGNAL REFR L WILL BE ASSERTED TO THE LOW STATE.
12313
12314 032536 004737 007304                21$: JSR      PC,XRASH                      ;SET XRAS H HIGH AND XRAS L LOW
12315
12316                                     :READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12317                                     :THE FOLLOWING SIGNALS BEING SET AS LISTED BELOW.
12318                                     :
12319                                     : INTER L - HIGH
12320                                     : REFR L  - LOW
12321                                     : XRAS H  - HIGH
12322                                     : XCAS L  - HIGH
12323                                     : ENEDC H - HIGH
12324                                     : PSM L   - HIGH
12325                                     : SOP L   - HIGH
12326 032542 042737 000020 002336        BIC      #VDAL4,R4GOOD                ;EXPECT EDEOC H TO BE A ZERO
12327 032550 004737 006654                JSR      PC,READR4                    ;READ VDAL AND PAUSE STATE MACHINE
12328 032554 001405                        BEQ      22$                          ;IF OK THEN CONTINUE
12329 032556                                     ERRDF    3,VDALRG,R4EROR              ;REFR F/F PROBABLY NOT SET TO A ONE
12330 032556 104455                        TRAP     C$ERDF
12331 032560 000003                        .WORD    3
12332 032562 002537                        .WORD    VDALRG
12333 032564 005004                        .WORD    R4EROR
12334 032566                                     CKLOOP
12335 032566 104406                        TRAP     C$CLP1
12336
12337                                     :PULSE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  A PULSE
12338                                     :ON XCAS H WHEN ADAL7 H IS SET TO A ONE WILL CLEAR THE REFR FLIP-FLOP,
12339                                     :THUS SETTING THE SIGNAL REFR L TO THE HIGH STATE.
12340
12341 032570 004737 007376                22$: JSR      PC,XCAS                      ;PULSE XCAS H AND XCAS L VIA HDAL13 H
12342
12343                                     :READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12344                                     :THE FOLLOWING SIGNALS BEING SET AS LISTED
12345                                     :
12346                                     : INTER L - HIGH
12347                                     : REFR L  - HIGH
12348                                     : XRAS H  - HIGH
12349                                     : XCAS L  - HIGH
12350                                     : ENEDC H - HIGH
12351                                     : PSM L   - HIGH
12352                                     : SOP L   - HIGH
12353 032574 052737 000020 002336        BIS      #VDAL4,R4GOOD                ;EXPECT EDEOC H TO BE A ONE
12354 032602 004737 006654                JSR      PC,READR4                    ;READ VDAL AND PAUSE STATE MACHINE
12355 032606 001405                        BEQ      23$                          ;IF OK THEN CONTINUE
12356 032610                                     ERRDF    3,VDALRG,R4EROR              ;REFR F/F NOT CLEARED BY XCAS H
12357 032610 104455                        TRAP     C$ERDF
12358 032612 000003                        .WORD    3
12359 032614 002537                        .WORD    VDALRG
12360 032616 005004                        .WORD    R4EROR
12361 032620                                     CKLOOP
12362 032620 104406                        TRAP     C$CLP1
12363
12364                                     :SET XRAS H AND XRAS L TO THE LOW AND HIGH STATES RESPECTIVELY BY
12365                                     :CLEARING HDAL12 H.  THIS IS DONE SO THAT THE REFR FLIP-FLOP CAN BE

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

```
12366 ;SET TO A ONE AGAIN WHEN XRAS H IS PULSED AGAIN IN THE NEXT SECTION
12367
12368 032622 004737 007336 23$: JSR PC,XRASL ;SET XRAS H LOW AND XRAS L HIGH
12369
12370 ;SET THE SIGNAL XRAS H AND XRAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12371 ;BY SETTING HDAL12 H TO A ONE. SETTING XRAS L TO THE LOW STATE WILL
12372 ;CLOCK THE LEVEL OF INTER L, WHICH IS HIGH, INTO THE REFR FLIP-FLOP,
12373 ;THUS SETTING THE FLIP-FLOP TO A ONE. THE SIGNAL REFR L WILL BE SET TO
12374 ;THE LOW STATE WHEN THE REFR FLIP-FLOP IS SET TO A ONE.
12375
12376 032626 004737 007304 JSR PC,XRASH ;SET XRAS H HIGH AND XRAS L LOW
12377
12378 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12379 ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12380 : INTER L - HIGH
12381 : REFR L - LOW
12382 : XRAS H - HIGH
12383 : XCAS L - HIGH
12384 : ENEDC H - HIGH
12385 : PSM L - HIGH
12386 : SOP L - HIGH
12387
12388 032632 042737 000020 002336 BIC #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ZERO
12389 032640 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12390 032644 001405 BEQ 24$ ;IF OK THEN CONTINUE
12391 032646 ERRDF 3,VDALRG,R4EROR ;REFR F/F PROBABLY NOT SET TO A ONE
12392 032646 104455 TRAP C$ERDF
12393 032650 000003 .WORD 3
12394 032652 002537 .WORD VDALRG
12395 032654 005004 .WORD R4EROR
12396 032656 CKLOOP
12397 032656 104406 TRAP C$CLP1
12398
12399 ;SET THE SIGNAL ADAL7 H TO A ZERO. WHEN ADAL7 H IS SET TO A ZERO, THE
12400 ;REFR FLIP-FLOP WILL BE CLEARED, THUS SETTING THE SIGNAL REFR L TO THE
12401 ;HIGH STATE.
12402
12403 032660 042737 000200 002330 24$: BIC #ADAL7,R2LOAD ;SET ADAL7 H TO A ZERO
12404 032666 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
12405 032672 001405 BEQ 25$ ;IF LOADED OK THEN CONTINUE
12406 032674 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
12407 032674 104455 TRAP C$ERDF
12408 032676 000002 .WORD 2
12409 032700 002513 .WORD ADALRG
12410 032702 004770 .WORD R2EROR
12411 032704 CKLOOP
12412 032704 104406 TRAP C$CLP1
12413
12414 ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12415 ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12416 : INTER L - HIGH
12417 : REFR L - HIGH
12418 : XRAS H - HIGH
12419 : XCAS L - HIGH
12420 : ENEDC H - HIGH
12421 : PSM L - HIGH
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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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12422 : SOP L - HIGH
12423
12424 032706 052737 000020 002336 25$: BIS #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ONE
12425 032714 004737 006654 JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
12426 032720 001405 BEQ 26$ ;IF OK THEN CONTINUE
12427 032722 ERRDF 3,VDALRG,R4EROR ;REFR F/F NOT CLEARED BY ADAL7 H A 0
12428 032722 104455 TRAP C$ERDF
12429 032724 000003 .WORD 3
12430 032726 002537 .WORD VDALRG
12431 032730 005004 .WORD R4EROR
12432 032732 CKLOOP
12433 032732 104406 TRAP C$CLP1
12434
12435 ;SET ADAL7 H BACK TO A ONE. THIS WILL ALLOW THE REFR FLIP-FLOP TO
12436 ;BE CLEARED.
12437
12438 032734 052737 000200 002330 26$: BIS #ADAL7,R2LOAD ;SETUP BIT TO BE LOADED
12439 032742 004737 006614 JSR PC,LDRDR2 ;LOAD, READ AND CHECK ADAL REGISTER
12440 032746 001405 BEQ 27$ ;IF LOADED OK THEN CONTINUE
12441 032750 ERRDF 3,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
12442 032750 104455 TRAP C$ERDF
12443 032752 000003 .WORD 3
12444 032754 002513 .WORD ADALRG
12445 032756 004770 .WORD R2EROR
12446 032760 CKLOOP
12447 032760 104406 TRAP C$CLP1
12448
12449 ;SET THE SIGNALS XRAS H AND XRAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12450 ;BY CLEARING HDAL12 H.
12451
12452 032762 004737 007336 27$: JSR PC,XRASL ;SET XRAS H LOW AND XRAS L HIGH
12453
12454 ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
12455 ;LOW STATE. XSEL1 L IS SET LOW BY SETTING HDAL6 H TO A ONE
12456
12457 032766 052737 000100 002342 BIS #HDAL6,R6LOAD ;SETUP BIT TO BE LOADED
12458 032774 004737 006672 JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
12459 033000 001405 BEQ 28$ ;IF OK THEN CONTINUE
12460 033002 ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
12461 033002 104455 TRAP C$ERDF
12462 033004 000004 .WORD 4
12463 033006 002605 .WORD HDALRG
12464 033010 005020 .WORD R06ERR
12465 033012 CKLOOP
12466 033012 104406 TRAP C$CLP1
12467
12468 ;SET THE SIGNAL XRAS H AND XRAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12469 ;BY SETTING HDAL 12 H TO A ONE. WHEN XRAS L IS SET LOW, THE REFR FLIP-
12470 ;FLOP WILL BE CLOCKED TO A ZERO AS A RESULT OF INTER L BEING ASSERTED
12471 ;LOW. WHEN REFR FLIP-FLOP IS A ZERO, THE SIGNAL REFR L WILL BE ASSERTED
12472 ;TO THE HIGH STATE.
12473
12474 033014 004737 007304 28$: JSR PC,XRASH ;SET XRAS H AND XRAS L LOW
12475
12476 ;CHECK THE SIGNAL BTS1 H TO BE A ONE AS A RESULT OF THE BTJET FLIP-FLOP
12477 ;BEING CLEARED AND THE SIGNAL INTER L BEING ASSERTED TO THE LOW STATE.

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12489 033020 052737 000040 002336
12490 033026 042737 000020 002336
12491 033034 004737 006654
12492 033040 001405
12493 033042
12494 033042 104455
12495 033044 000003
12496 033046 002537
12497 033050 005004
12498 033052
12499 033052 104406
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12504 033054 042737 000100 002342 29$:
12505 033062 004737 006672
12506 033066 001405
12507 033070
12508 033070 104455
12509 033072 000004
12510 033074 002605
12511 033076 005020
12512 033100
12513 033100 104406
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12528 033102 042737 000040 002336 30$:
12529 033110 052737 000020 002336
12530 033116 004737 006654
12531 033122 001405
12532 033124
12533 033124 104455
:
:READ THE VDAL REGISTER AND CHECK EDEOC H TO BE SET TO A ZERO AS A
:RESULT OF THE FOLLOWING SIGNALS BEING SET AS LISTED
:
: INTER L - LOW
: REFR L - HIGH
: XRAS H - HIGH
: XCAS L - HIGH
: ENEDC H - HIGH
: PSM L - HIGH
: SOP L - HIGH
:
BIS #VDAL5,R4GOOD ;EXPECT BTS1 H TO BE A 1 VIA INTER L
BIC #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ZERO
JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
BEQ 29$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;REFR F/F PROBABLY NOT A ZERO
TRAP C$ERDF
.WORD 3
.WORD VDALRG
.WORD R4EROR
CKLOOP
TRAP C$CLP1
:
:SET THE SIGNAL INTER L BACK TO THE HIGH STATE BY SETTING XSEL1 L
:BACK TO THE HIGH STATE BY SETTING HDAL6 H TO A ZERO.
BIC #HDAL6,R6LOAD ;SET XSEL1 L TO THE LOW STATE
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
BEQ 30$ ;IF OK THEN CONTINUE
ERRDF 4,HDALRG,R06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 4
.WORD HDALRG
.WORD R06ERR
CKLOOP
TRAP C$CLP1
:
:CHECK THE SIGNAL BTS1 H TO BE A ZERO AS A RESULT OF THE BTJET FLIP-FLOP
:BEING CLEARED AND THE SIGNAL INTER L BEING SET TO THE HIGH STATE.
:
:READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
:THE FOLLOWING SIGNALS BEING SET AS LISTED
:
: INTER L - HIGH
: REFR L - HIGH
: XRAS H - HIGH
: XCAS L - HIGH
: ENEDC H - HIGH
: PSM L - HIGH
: SOP L - HIGH
:
BIC #VDAL5,R4GOOD ;EXPECT BTS1 H TO BE A 0 VIA INTER L
BIS #VDAL4,R4GOOD ;EXPECT EDEOC H TO BE A ONE
JSR PC,READR4 ;READ VDAL AND PAUSE STATE MACHINE
BEQ 31$ ;IF OK THEN CONTINUE
ERRDF 3,VDALRG,R4EROR ;EDEOC H NOT SET TO A ONE
TRAP C$ERDF

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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

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12534 033126 000003      .WORD 3
12535 033130 002537      .WORD VDALRG
12536 033132 005004      .WORD R4EROR
12537 033134
12538 033134 104406      CKLOOP
12539                                TRAP C$CLP1
12540                                ;SET THE SIGNALS XRAS H AND XRAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12541                                ;BY CLEARING HDAL12 H.
12542
12543 033136 004737 007336      31$: JSR PC,XRASL                                ;SET XRAS H LOW AND XRAS L HIGH
12544
12545                                ;SET ADAL7 H AND ADAL4 H TO ZEROES IN THE ADAL REGISTER. ADAL7 H ON
12546                                ;A ZERO WILL HOLD THE REFR FLIP-FLOP IN THE CLEARED STATE, THUS
12547                                ;CAUSING THE SIGNAL REFR L TO REMAIN HIGH. ADAL4 H ON A ZERO WILL
12548                                ;ALLOW THE PAUSE MODE FLIP-FLOP TO BE CLOCKED TO THE PAUSE MODE WHEN
12549                                ;A PULSE IS ISSUED ON THE SIGNAL XRAS H.
12550
12551 033142 042737 000220 002330      BIC #ADAL7!ADAL4,R2LOAD      ;SETUP BITS TO BE CLEARED
12552 033150 004737 006614      JSR PC,LDRDR2                ;GO LOAD, READ AND CHECK ADAL REGISTER
12553 033154 001405      BEQ 32$                      ;IF LOADED OK THEN CONTINUE
12554 033156                                ERRDF 2,ADALRG,R2EROR        ;ADAL REGISTER NOT EQUAL EXPECTED
12555 033156 104455      TRAP C$ERDF
12556 033160 000002      .WORD 2
12557 033162 002513      .WORD ADALRG
12558 033164 004770      .WORD R2EROR
12559 033166
12560 033166 104406      CKLOOP
12561                                TRAP C$CLP1
12562
12563                                ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. WHEN
12564                                ;XRAS H IS PULSED AND ADAL4 H IS SET TO A ZERO, THE PAUSE MODE FLIP-
12565                                ;FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL PAUSE L TO
12566                                ;THE HIGH STATE. WHEN PAUSE L IS ASSERTED HIGH, THE SIGNAL SOP L
12567                                ;WILL BE ASSERTED LOW, THUS SETTING THE SIGNAL EDEOC H TO THE LOW
12568                                ;STATE.
12569 033170 004737 007272      32$: JSR PC,XRAS                                ;GO PULSE XRAS H VIA HDAL12 H
12570
12571                                ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT
12572                                ;OF THE FOLLOWING SIGNALS BEING SET AS LISTED
12573                                ;
12574                                ; INTER L - HIGH
12575                                ; REFR L - HIGH
12576                                ; XRAS H - LOW
12577                                ; XCAS L - HIGH
12578                                ; ENEDC H - HIGH
12579                                ; PSM L - HIGH
12580                                ; SOP L - LOW
12581 033174 042737 000020 002336      BIC #VDAL4,R4GOOD            ;EXPECT EDEOC H TO BE A ZERO
12582 033202 004737 006654      JSR PC,HEADR4                ;READ VDAL AND PAUSE STATE MACHINE
12583 033206 001405      BEQ 33$                      ;IF OK THEN CONTINUE
12584 033210                                ERRDF 3,VDALRG,R4EROR        ;EDEOC H NOT 0 VIA SOP L SET LOW
12585 033210 104455      TRAP C$ERDF
12586 033212 000003      .WORD 3
12587 033214 002537      .WORD VDALRG
12588 033216 005004      .WORD R4EROR
12589 033220      CKLOOP
  
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TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL

12590 033220 104406
12591
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12594 033222 005037 002334
12595 033226 004737 007712
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12597 033232
12598 033232
12599 033232 104405
12600 033234
12601 033234
12602 033234 104401
12603

TRAP C\$CLP1
;RESET ALL FLIP-FLOPS BY PULSING INVD L VIA VDAL2 H
33\$: CLR R4LOAD ;SETUP TO CLEAR ALL BITS
JSR PC,CLRPSM ;GO PULSE INVD L VIA VDAL2 H
ENDSEG
10000\$: TRAP C\$ESEG
ENDTST
L10074: TRAP C\$ETST

TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

.SBTTL TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

```

:++
: THIS TEST WILL CHECK THE TARGET EMULATOR'S INTERRUPT LOGIC USING THE SIGNALS
: TOBRK H AND BRK H TO CAUSE INTERRUPT REQUESTS. THE TEST WILL CHECK THAT NO
: INTERRUPTS OCCUR WHEN THE INTERRUPT ENABLE BIT IS CLEARED AND THE INTERRUPT
: REQUEST SIGNAL IS ASSERTED HIGH. THE TEST WILL CHECK THAT AN INTERRUPT WILL
: OCCUR WHEN THE INTERRUPT ENABLE BIT IS SET AND THE SIGNAL TOBRK H IS ASSERTED
: HIGH. THE TEST WILL CHECK THAT THE BREAK LATCH FLIP-FLOP CAN BE SET, CLEARED,
: AND THAT IT CAN CAUSE AN INTERRUPT.
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 033236 004737 005510
 033242
 033242 104404
 033244
 033244 012700 000340
 033250 104441
 033252 004737 006754
 033256 012737 000004 002342
 033264 004737 006672
 033270 001405
 033272 104455
 033274 000004
 033276 002605
 033300 005020
 033302 104406
 033304 005037 002330
 033310 004737 007772

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T43:: BGNTST
      JSR    PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
      BGNSEG
      TRAP   C$BSEG
      ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE ANY INTERRUPTS FROM
      ;OCCURRING.
      SETPRI #PRI07             ;RAISE THE CPU PRIORITY LEVEL TO 7
      MOV    #PRI07,R0
      TRAP   C$SPRI
      ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
      JSR    PC,SLHDAL          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
      ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL REGISTER BITS TO
      ;ZEROS. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
      ;TIMING AND CONTROL SIGNALS.
      MOV    #HDAL2,R6LOAD      ;SETUP BITS TO BE LOADED
      JSR    PC,LDRDR6          ;GO LOAD, READ AND CHECK HDAL REGISTER
      BEQ    1$                 ;IF LOADED OK THEN CONTINUE
      ERRDF  4,HDALRG,R06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
      TRAP   C$ERRDF
      .WORD  4
      .WORD  HDALRG
      .WORD  R06ERR
      CKLOOP
      TRAP   C$CLP1
      ;CLEAR ALL ADAL REGISTER BITS. TOGGLE THE SIGNAL BRKRES L BY SETTING
      ;AND CLEARING ADAL REGISTER BIT 0. THE SIGNAL BRKRES L WILL CLEAR THE
      ;SINGLE STEP BREAK FLIP-FLOP, THE MEMORY SIMULATOR BREAK FLIP-FLOP, AND
      ;THE BREAK LATCH FLIP-FLOP.
      1$: CLR    R2LOAD           ;SETUP TO CLEAR ALL ADAL BITS
      JSR    PC,BRKRES          ;GO PULSE BRKRES L VIA ADAL REG BIT 0
      ;TOGGLE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 2.
      ;ALL OTHER VDAL READ/WRITE BITS WILL BE CLEARED AND THE READ ONLY BITS
      ;WILL BE CHECKED TO BE ZERO. THE SIGNAL INVD L WILL SET ALL THE FLIP-
  
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TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

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12660                                     ;FLOPS ON THE MODULE, NOT CLEARED BY BRKRES L, TO A KNOWN STATE.
12661                                     ;A PULSE ON THE SIGNAL INVD L WILL ALSO CLEAR THE TIMEOUT BREAK ONE-
12662                                     ;SHOT, THUS SETTING ITS OUTPUT TO THE HIGH STATE.
12663
12664 033314 005037 002334                CLR      R4LOAD                ;SETUP TO CLEAR ALL VDAL BITS
12665 033320 004737 007712                JSR      PC,CLRPSM            ;GO PULSE INVD L VIA VDAL2 H
12666
12667                                     ;SET INTERRUPT VECTOR TO VECTOR SPECIFIED BY USER AT PROGRAM START TIME.
12668                                     ;THE CPU PRIORITY LEVEL WILL BE RESET TO PRIORITY LEVEL 7 WHEN AN
12669                                     ;INTERRUPT OCCURS.
12670
12671 033324                                     SETVEC  TEVECT,#INTSRV,#PRI07
12672 033324 012746 000340                MOV      #PRI07,-(SP)
12673 033330 012746 006724                MOV      #INTSRV,-(SP)
12674 033334 013746 002312                MOV      TEVECT,-(SP)
12675 033340 012746 000003                MOV      #3,-(SP)
12676 033344 104437                                     TRAP    C$SVEC
12677 033346 062706 000010                ADD      #10,SP
12678 033352 005002                CLR      R2                    ;CLEAR SOFTWARE INTERRUPT FLAG
12679
12680                                     ;SET CPU PRIORITY LEVEL TO ZERO. THIS WILL ALLOW AN INTERRUPT TO OCCUR
12681                                     ;WHEN THE TARGET EMULATOR INTERRUPT ENA$IF BIT IS SET AND A BREAK CONDI-
12682                                     ;TION IS GENERATED.
12683
12684 033354                                     SETPRI  #PRI00                ;LOWER CPU PRIORITY LEVEL TO ZERO
12685 033354 012700 000000                MOV      #PRI00,R0
12686 033360 104441                TRAP    C$SPRI
12687
12688                                     ;ISSUE A DUMMY INSTRUCTION HERE TO CHECK THAT NO INTERRUPT OCCURED
12689
12690 033362 000240                NOP
12691
12692                                     ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12693                                     ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS CLEARED, AND NO
12694                                     ;BREAK CONDITION IS BEING GENERATED.
12695
12696 033364 005702                TST      R2                    ;CHECK SOFTWARE INTERRUPT FLAG
12697 033366 001406                BEQ      2$                    ;IF NO INTERRUPT THEN CONTINUE
12698 033370                                     ERRDF   1,UNEXIN,ROEROR        ;INTERRUPTED WITH INT ENA + BRK H A 0
12699 033370 104455                TRAP    C$ERDF
12700 033372 000001                .WORD   1
12701 033374 002432                .WORD   UNEXIN
12702 033376 004754                .WORD   ROEROR
12703 033400 005002                CLR      R2                    ;CLEAR SOFTWARE INTERRUPT FLAG
12704 033402
12705 033402 104406                CKLOOP
12706                                     TRAP    C$CLP1
12707
12708                                     ;SET TARGET EMULATOR INTERRUPT ENABLE BIT TO A ONE BY SETTING GDAL
12709                                     ;REGISTER BIT 3 TO A ONE. NO INTERRUPT SHOULD OCCUR AT THIS POINT IN
12710                                     ;TIME.
12711 033404 052737 000010 002320 2$:      BIS      #GDAL3,ROLOAD        ;SETUP BIT TO BE LOADED
12712 033412 004737 006554                JSR      PC,LDRDRO            ;GO LOAD, READ AND CHECK GDAL REGISTER
12713 033416 001405                BEQ      3$                    ;IF LOADED OK THEN CONTINUE
12714 033420                                     ERRDF   1,GDALRG,ROEROR        ;GDAL REGISTER NOT EQUAL EXPECTED
12715 033420 104455                TRAP    C$ERDF

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12716 033422 000001      .WORD 1
12717 033424 002406      .WORD GDALRG
12718 033426 004754      .WORD ROEROR
12719 033430             CKLOOP
12720 033430 104406      TRAP C$CLP1
12721
12722                      ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12723                      ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, AND
12724                      ;NO BREAK CONDITION IS BEING GENERATED BY THE PROGRAM.
12725
12726 033432 005702      3$: TST R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12727 033434 001406      BEQ 4$                      ;IF NO INTERRUPT THEN CONTINUE
12728 033436             ERRDF 1,UNEXIN,ROEROR          ;INTERRUPT WITH INT ENA A 1 + BRK H A 0
12729 033436 104455      TRAP C$ERDF
12730 033440 000001      .WORD 1
12731 033442 002432      .WORD UNEXIN
12732 033444 004754      .WORD ROEROR
12733 033446 005002      CLR R2                      ;RESET SOFTWARE INTERRUPT FLAG
12734 033450             CKLOOP
12735 033450 104406      TRAP C$CLP1
12736
12737                      ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THIS IS
12738                      ;DONE TO CHECK THAT THE BREAK INTERRUPT LATCH FLIP-FLOP IS CLOCKED
12739                      ;TO A ZERO WHEN THE SIGNAL BRK H IS ASSERTED LOW.
12740
12741 033452 004737 007272      4$: JSR PC,XRAS                ;GO PULSE XRAS H VIA HDAL12 H
12742
12743                      ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12744                      ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE
12745                      ;BREAK LATCH FLIP-FLOP IS CLEARED, AND NO BREAK CONDITION IS BEING
12746                      ;GENERATED BY THE PROGRAM.
12747
12748 033456 005702      TST R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12749 033460 001406      BEQ 5$                      ;IF NO INTERRUPT THEN CONTINUE
12750 033462             ERRDF 1,UNEXIN,ROEROR          ;CHECK BREAK LATCH FLIP-FLOP TO BE A 0
12751 033462 104455      TRAP C$ERDF
12752 033464 000001      .WORD 1
12753 033466 002432      .WORD UNEXIN
12754 033470 004754      .WORD ROEROR
12755 033472 005002      CLR R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12756 033474             CKLOOP
12757 033474 104406      TRAP C$CLP1
12758
12759                      ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE ANY INTEPRUPTS FROM
12760                      ;OCCURING.
12761
12762 033476             5$: SETPRI #PRI07                ;DISABLE INTERRUPTS
12763 033476 012700 000340      MOV #PRI07,RO
12764 033502 104441      TRAP C$SPRI
12765
12766                      ;SET ADAL REGISTER BIT 8 TO A ONE TO ENABLE THE TIMEOUT BREAK ONE SHOTS
12767                      ;OUTPUT TO THE GDAL REGISTER AND TO THE SIGNAL BRK H. THE TIMEOUT
12768                      ;BREAK ONE SHOT HAS NOT BEEN FIRED, THEREFORE, THE SIGNALS TOBRK H AND
12769                      ;BRK H SHOULD BE ASSERTED HIGH TO INDICATE A BREAK CONDITION. AN
12770                      ;INTERRUPT WILL BE GENERATED BY THE SIGNAL TOBRK H AS SOON AS THE PROGRAM
12771                      ;LOWERS THE CPU PRIORITY LEVEL TO ZERO.

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12828 033612 001005      BNE      9$                :IF INTERRUPTED THEN CONTINUE
12829 033614              ERRDF    1,NOINT,ROEROR   :FAILED TO INTERRUPT
12830 033614 104455      TRAP    C$ERDF
12831 033616 000001      .WORD   1
12832 033620 002467      .WORD   NOINT
12833 033622 004754      .WORD   ROEROR
12834 033624              CKLOOP
12835 033624 104406      TRAP    C$CLP1
12836
12837
12838                      :AT THIS POINT IN TIME THE CPU PRIORITY LEVEL IS AT 7 AS A REUSLT OF
12839                      :AN INTERRUPT. CHECK THE PREVIOUS GDAL REGISTER AGAINST THE GDAL
12840                      :REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
12841 033626 005002      CLR      R2                :CLEAR SOFTWARE INTERRUPT FLAG
12842 033630 023737 002322 002326 9$:  CMP      ROGOOD,ROBAD     :CHECK EXPECTED AGAINST READ FROM INTERRUPT
12843 033636 001405      BEQ      10$              :IF OK THEN CONTINUE
12844 033640              ERRDF    1,GDALRG,ROEROR  :GDAL CHANGED AFTER AN INTERRUPT OCCURED
12845 033640 104455      TRAP    C$ERDF
12846 033642 000001      .WORD   1
12847 033644 002406      .WORD   GDALRG
12848 033646 004754      .WORD   ROEROR
12849 033650              CKLOOP
12850 033650 104406      TRAP    C$CLP1
12851
12852                      :TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THE SIGNAL
12853                      :XRAS H SHOULD CLOCK THE BREAK LATCH FLIP-FLOP TO A ONE AS A RESULT OF
12854                      :THE SIGNAL BRK H BEING ASSERTED HIGH. THE SIGNAL BRK H IS ASSERTED
12855                      :HIGH AS A RESULT OF THE SIGNAL TOBRK H BEING ASSERTED HIGH.
12856
12857 033652 004737 007272 10$: JSR      PC,XRAS          :GO PULSE XRAS H VIA HDAL12 H
12858
12859                      :SET THE SIGNAL TOBRK H TO THE LOW STATE BY SETTING ADAL8 H TO A ZERO.
12860
12861 033656 042737 000400 002330 BIC      #ADAL8,R2LOAD    :SETUP TO SET TOBRK H TO LOW STATE
12862 033664 004737 006614      JSR      PC,LDRDR2       :GO LOAD, READ AND CHECK ADAL REGISTER
12863 033670 001405      BEQ      11$              :IF LOADED OK THEN CONTINUE
12864 033672              ERRDF    2,ADALRG,R2EROR  :ADAL REGISTER NOT EQUAL EXPECTED
12865 033672 104455      TRAP    C$ERDF
12866 033674 000002      .WORD   2
12867 033676 002513      .WORD   ADALRG
12868 033700 004770      .WORD   R2EROR
12869 033702              CKLOOP
12870 033702 104406      TRAP    C$CLP1
12871
12872                      :READ GDAL REGISTER TO CHECK THAT THE SIGNAL TOBRK H IS A ZERO AS A
12873                      :RESULT OF ADAL8 H BEING SET TO A ZERO.
12874
12875 033704 042737 000100 002322 11$: BIC      #TOBRK,ROGOOD    :EXPECT TOBRK H TO BE A ZERO
12876 033712 004737 006570      JSR      PC,READRO       :READ AND CHECK GDAL REGISTER
12877 033716 001405      BEQ      12$              :IF OK THEN CONTINUE
12878 033720              ERRDF    1,GDALRG,ROEROR  :TOBRK H PROBABLY NOT A ZERO
12879 033720 104455      TRAP    C$ERDF
12880 033722 000001      .WORD   1
12881 033724 002406      .WORD   GDALRG
12882 033726 004754      .WORD   ROEROR
12883 033730              CKLOOP

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TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

12884	033730	104406				TRAP	C\$CLP1	
12885								
12886								:AT THIS POINT IN TIME THE BREAK LATCH FLIP-FLOP SHOULD BE SET TO A ONE
12887								:AND THE SIGNALS TOBRK H AND BRK H SHOULD BE ASSERTED LOW. THE PROGRAM
12888								:WILL NOW LOWER THE CPU PRIORITY LEVEL TO ZERO. NO INTERRUPT SHOULD
12889								:OCCUR BECAUSE NEITHER THE REQUEST, ALTHOUGH HIGH, OR THE TARGET EMULATOR
12890								:INTERRUPT ENABLE BIT HAS CHANGED STATE TO CLOCK THE DC003'S INTERRUPT
12891								:REQUEST FLIP-FLOP.
12892								
12893	033732				12\$:	SETPRI	#PRI00	:LOWER PRIORITY TO ENABLE INTERRUPTS
12894	033732	012700	000000			MOV	#PRI00,RO	
12895	033736	104441				TRAP	C\$SPRI	
12896								
12897								:CHECK THAT NO INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
12898								:BEING AT 0, THE TARGET EMULATOR INTERRUPT ENABLE BIT BEING SET, AND
12899								:THE BREAK LATCH FLIP-FLOP BEING SET TO A ONE. NO INTERRUPT SHOULD
12900								:OCCUR UNTIL EITHER THE REQUEST OR THE INTERRUPT ENABLE BIT HAS
12901								:TOGGLED.
12902								
12903	033740	000240				NOP		:SHOULD NOT INTERRUPT HERE
12904	033742	005702				TST	R2	:CHECK SOFTWARE INTERRUPT FLAG
12905	033744	001406				BEQ	13\$:IF NO INTERRUPT THEN CONTINUE
12906	033746					ERRDF	1,UNEXIN,ROEROR	:INTERRUPTED W/O TOGGING I.E. OR RQSTA H
12907	033746	104455				TRAP	C\$ERDF	
12908	033750	000001				.WORD	1	
12909	033752	002432				.WORD	UNEXIN	
12910	033754	004754				.WORD	ROEROR	
12911	033756	005002				CLR	R2	:CLEAR SOFTWARE INTERRUPT FLAG
12912	033760					CKLOOP		
12913	033760	104406				TRAP	C\$CLP1	
12914								
12915								:RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS FROM OCCURING.
12916								
12917	033762				13\$:	SETPRI	#PRI07	:DISABLE INTERRUPTS FROM OCCURING
12918	033762	012700	000340			MOV	#PRI07,RO	
12919	033766	104441				TRAP	C\$SPRI	
12920								
12921								:TO CHECK THAT THE BREAK LATCH FLIP-FLOP IS SET TO A ONE, THE PROGRAM
12922								:MUST CLEAR AND SET THE TARGET EMULATORS INTERRUPT ENABLE BIT TO C'OCK
12923								:THE INTERRUPT REQUEST INTO THE DC003'S INTERRUPT REQUEST FLIP-FLOP.
12924								
12925	033770	042737	000010	002320		BIC	#GDAL3,ROLOAD	:SETUP TO CLEAR I.E. BIT
12926	033776	004737	006554			JSR	PC,LDRDRO	:GO LOAD, READ AND CHECK GDAL REGISTER
12927	034002	001405				BEQ	14\$:IF LOADED OK THEN CONTINUE
12928	034004					ERRDF	1,GDALRG,ROEROR	:GDAL REGISTER NOT EQUAL EXPECTED
12929	034004	104455				TRAP	C\$ERDF	
12930	034006	000001				.WORD	1	
12931	034010	002406				.WORD	GDALRG	
12932	034012	004754				.WORD	ROEROR	
12933	034014					CKLOOP		
12934	034014	104406				TRAP	C\$CLP1	
12935	034016	052737	000010	002320	14\$:	BIS	#GDAL3,ROLOAD	:SETUP TO SET I.E. BIT TO A 1
12936	034024	004737	006554			JSR	PC,LDRDRO	:GO LOAD, READ AND CHECK GDAL REGISTER
12937	034030	001405				BEQ	15\$:IF LOADED OK THEN CONTINUE
12938	034032					ERRDF	1,GDALRG,ROEROR	:GDAL REGISTER NOT EQUAL EXPECTED
12939	034032	104455				TRAP	C\$ERDF	

```

12940 034034 000001      .WORD      '
12941 034036 002406      .WORD      GDALRG
12942 034040 004754      .WORD      ROEROR
12943 034042                CKLOOP
12944 034042 104406      TRAP       C$CLP1
12945
12946                :AT THIS POINT IN TIME THE BREAK LATCH FLIP-FLOP SHOULD BE SET TO A
12947                :ONE AND THE SIGNALS TOBRK H AND BRK H SHOULD BE ASSERTED LOW. THE
12948                :DC003'S INTERRUPT REQUEST FLIP-FLOP SHOULD BE SET TO A ONE AS A
12949                :RESULT OF THE INTERRUPT ENABLE BIT BEING CLEARED AND SET AND THE
12950                :BREAK LATCH FLIP-FLOP BEING SET TO A ONE. THE PROGRAM WILL NOW LOWER
12951                :THE CPU PRIORITY LEVEL TO ZERO AND EXPECT AN INTERRUPT TO OCCUR AS A
12952                :RESULT OF THE BREAK LATCH FLIP-FLOP BEING SET.
12953
12954 034044                15$: SETPRI  #PRI00                :ALLOW INTERURPTS TO OCCUR
12955 034044 012700 000000  MOV     #PRI00,R0
12956 034050 104441      TRAP     C$SPRI
12957
12958                :CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
12959                :BEING AT ZERO, THE TARGET EMULATOR INT'RRUPT ENABLE BIT BEING SET, AND
12960                :THE BREAK LATCH FLIP-FLOP BEING SET TO A ONE.
12961
12962 034052 000240      NOP                :SHOULD INTERRUPT HERE
12963 034054 005702      TST     R2                :CHECK SOFTWARE INTERRUPT FLAG
12964 034056 001005      BNE     16$                :IF INTERRUPTED THEN CONTINUE
12965 034060                ERRDF  1,NOINT,ROEROR        :BREAK F/F FAILED TO SET OR CAUSE INTERRUPT
12966 034060 104455      TRAP     C$ERDF
12967 034062 000001      .WORD      1
12968 034064 002467      .WORD      NOINT
12969 034066 004754      .WORD      ROEROR
12970 034070                CKLOOP
12971 034070 104406      TRAP     C$CLP1
12972
12973                :AT THIS POINT IN TIME, THE CPU PRIORITY LEVEL IS AT 7 AS A RESULT OF
12974                :THE INTERRUPT. CHECK THE PREVIOUS EXPECTED GDAL REGISTER AGAINST THE
12975                :GDAL REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
12976
12977 034072 005002                16$: CLR     R2                :CLEAR THE SOFTWARE INTERRUPT FLAG
12978 034074 023737 002322 002326  CMP     ROGOOD,ROBAD        :CHECK EXPECTED AGAINST READ VIA INTERRUPT
12979 034102 001405      BEQ     17$                :IF OK THEN CONTINUE
12980 034104                ERRDF  1,GDALRG,ROEROR        :GDAL REGISTER NOT EQUAL TO EXPECTED
12981 034104 104455      TRAP     C$ERDF
12982 034106 000001      .WORD      1
12983 034110 002406      .WORD      GDALRG
12984 034112 004754      .WORD      ROEROR
12985 034114                CKLOOP
12986 034114 104406      TRAP     C$CLP1
12987
12988                :AS RESULT OF THE INTERRUPT, THE BREAK LATCH FLIP-FLOP SHOULD HAVE BEEN
12989                :CLEARED BY THE SIGNAL VECTOR H. TO TEST THAT THIS HAPPENED, THE
12990                :PROGRAM MUST CLEAR AND SET THE TARGET EMULATORS INTERRUPT ENABLE BIT
12991                :TO CLOCK THE LEVEL OF THE INTERRUPT REQUEST, WHICH SHOULD BE LOW, INTO
12992                :THE DC003'S INTERRUPT REQUEST FLIP-FLOP, THUS CAUSING THE DC003'S
12993                :INTERRUPT REQUEST FLIP-FLOP TO BE CLOCKED TO A ZERO.
12994
12995 034116 042737 000010 002320 17$: BIC     #GDAL3,ROLOAD        :SETUP TO CLEAR INTERRUPT ENABLE

```


TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

```

12996 034124 004737 006554      JSR    PC,LDRDRO      ;GO LOAD, READ AND CHECK INT ENA
12997 034130 001405              BEQ    18$            ;IF LOADED OK THEN CONTINUE
12998 034132              ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
12999 034132 104455      TRAP  C$ERDF
13000 034134 000001      .WORD 1
13001 034136 002406      .WORD GDALRG
13002 034140 004754      .WORD ROEROR
13003 034142              CKLOOP
13004 034142 104406      TRAP  C$CLP1
13005 034144 052737 000010 002320 18$:  BIS    #GDAL3,ROLOAD ;SETUP TO SET INTERRUPT ENABLE
13006 034152 004737 006554              JSR    PC,LDRDRO      ;GO LOAD, READ AND CHECK GDAL REGISTER
13007 034156 001405              BEQ    19$            ;IF LOADED OK THEN CONTINUE
13008 034160              ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL TO EXPECTED
13009 034160 104455      TRAP  C$ERDF
13010 034162 000001      .WORD 1
13011 034164 002406      .WORD GDALRG
13012 034166 004754      .WORD ROEROR
13013 C,4170              CKLOOP
13014 034170 104406      TRAP  C$CLP1
13015
13016              ;AS A RESULT OF THE INTERRUPT, THE BREAK LATCH FLIP-FLOP SHOULD HAVE
13017              ;BEEN CLEARED BY THE SIGNAL VECTOR H. THE TEST WILL NOW LOWER THE
13018              ;CPU PRIORITY LEVEL AND CHECK THAT NO INTERRUPT WILL OCCUR.
13019
13020 034172              19$:  SETPRI #PRI00          ;ENABLE INTERRUPTS TO OCCUR
13021 034172 012700 000000      MOV    #PRI00,RO
13022 034176 104441      TRAP  C$SPRI
13023
13024              ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT ZERO,
13025              ;THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE SIGNAL
13026              ;TOBRK H IS ASSERTED LOW AND THE BREAK LATCH FLIP-FLOP IS CLEARED.
13027
13028 034200 000240      NOP
13029 034202 005702      TST   R2              ;CHECK SOFTWARE INTERRUPT FLAG
13030 034204 001406      BEQ   20$            ;IF NO INTERRUPT THEN CONTINUE
13031 034206              ERRDF  1,UNEXIN,ROEROR ;BREAK LATCH F/F FAILED TO 0 VIA VECTOR H
13032 034206 104455      TRAP  C$ERDF
13033 034210 000001      .WORD 1
13034 034212 002432      .WORD UNEXIN
13035 034214 004754      .WORD ROEROR
13036 034216 005002      CLR   R2              ;CLEAR SOFTWARE INTERRUPT FLAG
13037 034220              CKLOOP
13038 034220 104406      TRAP  C$CLP1
13039
13040              ;SET THE TARGET EMULATOR INTERRUPT ENABLE BIT TO A ZERO.
13041
13042 034222 042737 000010 002320 20$: BIC    #GDAL3,ROLOAD ;SETUP TO CLEAR TE INT ENA BIT
13043 034230 004737 006554              JSR    PC,LDRDRO      ;GO LOAD, READ AND CHECK GDAL REGISTER
13044 034234 001405              BEQ   21$            ;IF LOADED OK THEN CONTINUE
13045 034236              ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
13046 034236 104455      TRAP  C$ERDF
13047 034240 000001      .WORD 1
13048 034242 002406      .WORD GDALRG
13049 034244 004754      .WORD ROEROR
13050 034246              CKLOOP
13051 034246 104406      TRAP  C$CLP1

```

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13052
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13055
13056
13057 034250 052737 000400 002330 21$: BIS #ADAL8,R2LOAD ;ENABLE TOBRK H AND BRK H TO HIGH STATE
13058 034256 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
13059 034262 001405 BEQ 22$ ;IF OK THEN CONTINUE
13060 034264 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL TO EXPECTED
13061 034264 104455 TRAP C$ERDF
13062 034266 000002 .WORD 2
13063 034270 002513 .WORD ADALRG
13064 034272 004770 .WORD R2EROR
13065 034274 CKLOOP
13066 034274 104406 TRAP C$CLP1
13067
13068 ;CLOCK THE LEVEL OF BRK H, WHICH SHOULD BE ASSERTED HIGH VIA TOBRK H,
13069 ;INTO THE BREAK LATCH FLIP-FLOP, THUS SETTING THE BREAK LATCH FLIP-FLOP
13070 ;TO A ONE. THE BREAK LATCH FLIP-FLOP WILL BE CLOCKED TO A ONE BY
13071 ;PULSING THE SIGNAL XRAS H VIA HDAL12 H.
13072
13073 034276 004737 007272 22$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
13074
13075 ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL WAS AT 0,
13076 ;THE TARGET EMULATOR INTERRUPT ENABLE BIT IS CLEARED, THE TIMEOUT
13077 ;BREAK SIGNAL IS HIGH AND THE BREAK LATCH FLIP-FLOP IS SET TO A ONE.
13078
13079 034302 052737 000100 002322 BIS #TOBRK,ROGOOD ;EXPECT TOBRK H TO BE SET TO A ONE
13080 034310 005702 TST R2 ;CHECK SOFTWARE INTERRUPT FLAG
13081 034312 001406 BEQ 23$ ;IF OK THEN CONTINUE
13082 034314 ERRDF 1,UNEXIN,ROEROR ;INTERRUPTED WITH TE INT ENA CLEARED
13083 034314 104455 TRAP C$ERDF
13084 034316 000001 .WORD 1
13085 034320 002432 .WORD UNEXIN
13086 034322 004754 .WORD ROEROR
13087 034324 005002 CLR R2 ;CLEAR SOFTWARE INTERRUPT FLAG
13088 034326 CKLOOP
13089 034326 104406 TRAP C$CLP1
13090
13091 ;SET THE SIGNAL TOBRK H TO THE LOW STATE BY CLEARING ADAL8 H AND PULSE
13092 ;THE SIGNAL BRKRES L BY SETTING AND CLEARING THE SIGNAL ADALO H. A PULSE
13093 ;ON THE SIGNAL BRKRES L WILL CLEAR THE BREAK LATCH FLIP-FLOP.
13094
13095 034330 005037 002330 23$: CLR R2LOAD ;SETUP TO CLEAP ADAL8 H (TOBRK H = 0)
13096 034334 004737 007772 JSR PC,BRKRES ;GO PULSE BRKRES L VIA ADALO H
13097 034340 042737 000100 002322 BIC #TOBRK,ROGOOD ;EXPECT TOBRK H TO BE A 0
13098
13099 ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS
13100
13101 034346 SETPRI #PRI07
13102 034346 012700 000340 MOV #PRI07,R0
13103 034352 104441 TRAP C$SPRI
13104
13105 ;SET THE TARGET EMULATOR INTERRUPT ENABLE BIT TO A ONE BY SETTING
13106 ;GDAL REGISTER BIT 3 TO A ONE
13107

```

TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST

```

13108 034354 052737 000010 002320      BIS      #GDAL3,ROLOAD      ;SETUP BIT TO BE LOADED
13109 034362 004737 006554              JSR      PC,LDRDRO         ;GO LOAD, READ AND CHECK GDAL REGISTER
13110 034366 001405                      BEQ      24$              ;IF LOADED OK THEN CONTINUE
13111 034370                                ERRDF    1,GDALRG,ROEROR   ;GDAL REGISTER NOT EQUAL TO EXPECTED
13112 034370 104455                      TRAP    C$ERDF
13113 034372 000001                      .WORD   1
13114 034374 002406                      .WORD   GDALRG
13115 034376 004754                      .WORD   ROEROR
13116 034400                                CKLOOP
13117 034400 104406                      TRAP    C$CLP1
13118
13119
13120                                ;LOWER THE CPU PRIORITY BACK TO ZERO TO ALLOW INTERRUPTS TO OCCUR.
13121                                ;NO INTERRUPTS SHOULD OCCUR BECAUSE THE BREAK LATCH FLIP-FLOP
13122                                ;SHOULD HAVE BEEN CLEARED BY THE SIGNAL BRKRES L ABOVE.
13123 034402                                24$:  SETPRI  #PRI00              ;LOWER THE CPU PRIORITY LEVEL TO 0
13124 034402 012700 000000                      MOV     #PRI00,RO
13125 034406 104441                      TRAP    C$SPRI
13126
13127                                ;CHECK THAT NO INTERRUPTS OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
13128                                ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE
13129                                ;SIGNAL TOBRK H IS ASSERTED LOW, AND THE BREAK LATCH FLIP-FLOP IS CLEARED
13130
13131 034410 000240                      NOP
13132 034412 005702                      TST     R2                ;CHECK THE SOFTWARE INTERRUPT FLAG
13133 034414 001406                      BEQ     25$              ;IF NO INTERRUPT THEN CONTINUE
13134 034416                                ERRDF    1,UNEXIN,ROEROR  ;BREAK LATCH F/F NOT CLEARED BY BRKRES L
13135 034416 104455                      TRAP    C$ERDF
13136 034420 000001                      .WORD   1
13137 034422 002432                      .WORD   UNEXIN
13138 034424 004754                      .WORD   ROEROR
13139 034426 005002                      CLR     R2                ;CLEAR SOFTWARE INTERRUPT FLAG
13140 034430                                CKLOOP
13141 034430 104406                      TRAP    C$CLP1
13142
13143                                ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS
13144
13145 034432                                25$:  SETPRI  #PRI07              ;RAISE CPU PRIORITY LEVEL TO 7
13146 034432 012700 000340                      MOV     #PRI07,RO
13147 034436 104441                      TRAP    C$SPRI
13148
13149                                ;RETURN THE TARGET EMULATOR INTERRUPT VECTOR BACK TO THE DIAGNOSTIC
13150                                ;SUPERVISOR VECTOR HANDLER
13151
13152 034440                                CLRVEC  TEVECT
13153 034440 013700 002312                      MOV     TEVECT,RO
13154 034444 104436                      TRAP    C$VECT
13155
13156 034446                                ENDSEG
13157 034446                                10000$:
13158 034446 104405                      TRAP    C$ESEG
13159 034450                                L10075:
13160 034450                                ENDTST
13161 034450 104401                      TRAP    C$SETST
13162

```

TEST 44: INITO L AND INITO H LOGIC TEST

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 13174
 13175 034452
 13176 034452
 13177
 13178 034452 004737 005510
 13179
 13180
 13181
 13182
 13183
 13184
 13185 034456
 13186 034456
 13187 034456 104402
 13188 034460 005037 002346
 13189
 13190
 13191
 13192 034464 012737 177373 002330
 13193 034472 004737 006614
 13194 034476 001405
 13195 034500
 13196 034500 104455
 13197 034502 000002
 13198 034504 002513
 13199 034506 004770
 13200 034510
 13201 034510 104406
 13202
 13203
 13204
 13205
 13206 034512 004737 007006
 13207
 13208
 13209
 13210
 13211
 13212 034516 012737 177777 002342
 13213 034524 004737 006672
 13214 034530 001405
 13215 034532
 13216 034532 104455
 13217 034534 000004
 13218 034536 002631

.SBTTL TEST 44: INITO L AND INITO H LOGIC TEST

```

:++
: THIS TEST WILL CHECK THAT THE SIGNALS ADAL 15:9, ADAL 7:3, ADAL 1:0, HDAL 15:0,
: FDAL7 H - FDALO H, VDAL7 H, VDAL2 H - VDALO H, GDAL15 H, GDAL2 H - GDALO H,
: AND MR15 H - MRO H CAN ALL BE SET TO ONES. THEN A BRESSET INSTRUCTION IS
: ISSUED AND THESE SIGNALS ARE TESTED TO THEN BE ZEROS. THEN THE PAUSE STATE
: WORKING FLIP-FLOP AND THE SINGLE STEP BREAK FLIP-FLOP ARE SET TO ONES AND
: AGAIN A BRESSET INSTRUCTION IS ISSUED AND THESE FLIP-FLOPS ARE TESTED TO THEN
: BE ZEROS.
:--

```

T44:: BGNTST

JSR PC,INITTE ;SELECT AND INITIALIZE TARGET EMULATOR

```

:CHECK TO SEE IF ADAL15 H - ADALO H, HDAL15 H - HDALO H, FDAL7 H -
:FDALO H, VDAL7 H, VDAL2 H - VDALO H, GDAL15 H, GDAL2 H - GDALO H, AND
:MR15 H - MRO H CAN BE SET TO ONES AND THEN CLEARED BY ISSUING A BRESSET
:INSTRUCTION.

```

T44.1: BGNSUB

TRAP C\$BSUB ;CLEAR REG 6 MASK WORD
 CLR R6MASK

;LOAD, READ AND CHECK BITS ADAL 15:9, ADAL 7:3, AND ADAL 1:0 WITH ALL ONES.

```

MOV #177373,R2LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK REG 2
BEQ 1$ ;IF LOADED OK THEN CONT
ERRDF 2,ADALRG,R2EROR ;REG 2 NOT EQUAL 177777
TRAP C$ERDF
.WORD 2
.WORD ADALRG
.WORD R2EROR
CKLOOP
TRAP C$CLP1

```

```

;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

```

1\$: JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0

```

;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF ALL
:ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
:WITH GDAL2 SET IN CONTROL REGISTER 0.

```

```

MOV #177777,R6LOAD ;SETUP DATA TO BE LOADED
JSR PC,LDRDR6 ;GO LOAD, READ AND CHECK MODE REG
BEQ 2$ ;IF LOADED OK THEN CONT.
ERRDF 4,MODREG,R06ERR ;MODE REGISTER NOT EQUAL 177777
TRAP C$ERDF
.WORD 4
.WORD MODREG

```

```

13219 034540 005020          .WORD   R06ERR
13220 034542                CKLOOP
13221 034542 104406          TRAP    C$CLP1
13222
13223                        ;LOAD, READ AND CHECK BITS VDAL7 H, VDAL2 H - VDAL0 H WITH ONES.
13224
13225 054544 012737 000207 002334 2$:  MOV    #VDAL7!VDAL2!VDAL1!VDALO,R4LOAD ;SET ALL R/W BITS TO ONE
13226 034552 004737 006640          JSR    PC,LDRDR4 ;GO LOAD, READ AND CHECK REG 4
13227 034556 001405          BEQ    3$ ;IF LOADED OK THEN CONT
13228 034560          ERRDF  3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
13229 034560 104455          TRAP   C$ERDF
13230 034562 000003          .WORD   3
13231 034564 002537          .WORD   VDALRG
13232 034566 005004          .WORD   R4EROR
13233 034570                CKLOOP
13234 034570 104406          TRAP    C$CLP1
13235
13236                        ;SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
13237                        ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13238
13239 034572 004737 006754          3$:   JSR    PC,SLHDAL ;SELECT HDAL REG VIA GDAL BITS 2:0
13240
13241                        ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF ALL
13242                        ;ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13243                        ;WITH GDAL1 AND GDALO SET IN CONTROL REGISTER 0.
13244
13245 034576 012737 177777 002342  MOV    #177777,R6LOAD ;SETUP DATA TO BE LOADED
13246 034604 004737 006672          JSR    PC,LDRDR6 ;GO LOAD, READ AND CHECK HDAL REGISTER
13247 034610 001405          BEQ    4$ ;IF LOADED OK THEN CONT.
13248 034612          ERRDF  4,HDALRG,R06ERR ;HDAL REG NOT EQUAL 177777
13249 034612 104455          TRAP   C$ERDF
13250 034614 000004          .WORD   4
13251 034616 002605          .WORD   HDALRG
13252 034620 005020          .WORD   R06ERR
13253 034622                CKLOOP
13254 034622 104406          TRAP    C$CLP1
13255
13256                        ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
13257                        ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13258
13259 034624 004737 007154          4$:   JSR    PC,SLFDAL ;GO SELECT FDAL REG VIA GDAL BITS 2:0
13260
13261                        ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
13262                        ;ONES (377) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13263                        ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
13264
13265 034630 012737 177400 002346  MOV    #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE
13266 034636 012737 000377 002342  MOV    #377,R6LOAD ;SETUP DATA TO BE LOADED
13267 034644 004737 006672          JSR    PC,LDRDR6 ;GO LOAD, READ AND CHECK FDAL REG
13268 034650 001405          BEQ    5$ ;IF DATA LOADED OK THEN CONT
13269 034652          ERRDF  4,FDALRG,R06ERR ;FDAL REG NOT EQUAL TO 377
13270 034652 104455          TRAP   C$ERDF
13271 034654 000004          .WORD   4
13272 034656 002653          .WORD   FDALRG
13273 034660 005020          .WORD   R06ERR
13274 034662                CKLOOP

```

```

13275 034662 104406 TRAP C$CLP1
13276
13277 ;CHECK THAT GDAL BITS 2:0 AND GDAL BIT 15 CAN BE SET TO ONES
13278
13279 034664 013737 002316 002322 5$: MOV IDTYPE,ROGOOD ;SETUP EXPECTED DATA
13280 034662 052737 000007 002322 BIS #GDAL2!GDAL1!GDALO,ROGOOD ;SETUP EXPECTED DATA
13281 034700 052737 100007 002320 BIS #GDAL15!GDAL2!GDAL1!GDALO,ROLOAD ;SETUP BITS TO BE LOADED
13282 034706 004737 006562 JSR PC,LDRDOR ;GO LOAD, READ AND CHECK REG 0
13283 034712 001405 BEQ 6$ ;IF LOADED OK THEN CONT
13284 034714 ERRDF 1,GDALRG,ROEROR ;REG 0 NOT EQUAL 100007
13285 034714 104455 TRAP C$ERDF
13286 034716 000001 .WORD 1
13287 034720 002406 .WORD GDALRG
13288 034722 004754 .WORD ROEROR
13289 034724 CKLOOP
13290 034724 104406 TRAP C$CLP1
13291
13292 ;ISSUE A BRESET INSTRUCTION
13293
13294 034726 6$: BRESET ;ASSERT INITO L AND INITO H
13295 034726 104433 TRAP C$RESET
13296 034730 SETVEC #4,#7$,#PRI07
13297 034730 012746 000340 MOV #PRI07,-(SP)
13298 034734 012746 035002 MOV #7$,-(SP)
13299 034740 012746 000004 MOV #4,-(SP)
13300 034744 012746 000003 MOV #3,-(SP)
13301 034750 104437 TRAP C$SVEC
13302 034752 062706 000010 ADD #10,SP
13303 034756 013705 002300 MOV REG0,R5 ;SAVE ADDRESS OF REG 0
13304 034762 113765 002311 000001 MOV# IDDEV+1,1(R5) ;SAVE ID NUMBER
13305 034770 000240 NOP
13306 034772 CLRVEC #4 ;RELEASE DEVICE TIMEOUT VECTOR
13307 034772 012700 000004 MOV #4,R0
13308 034776 104436 TRAP C$CVEC
13309 035000 000421 BR 8$ ;IF NO DEVICE TIMEOUT THEN CONTINUE
13310
13311 ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS NO DEVICE #0
13312 ;IN THE SYSTEM, THEREFORE, THE TARGET EMULATOR HAS TO BE RESELECTED BY
13313 ;DOING A 'MOV WORD' OPERATION. A 'MOV#' OPERATION PERFORMED ABOVE DOES
13314 ;A READ/MODIFY WRITE. THEREFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM,
13315 ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13316
13317 035002 005726 7$: TST (SP)+ ;CLEAN UP STACK AFTER DEVICE TIMEOUT
13318 035004 005726 TST (SP)+
13319 035006 CLRVEC #4 ;RELEASE DEVICE TIMEOUT VECTOR
13320 035006 012700 000004 MOV #4,R0
13321 035012 104436 TRAP C$CVEC
13322 035014 013737 002310 002320 MOV IDDEV,ROLOAD ;GET TAR EMULATORS DEVICE NUMBER
13323 035022 004737 006554 JSR PC,LDRDOR ;LOAD, READ AND CHECK CONTROL REG 0
13324 035026 001424 BEQ 9$ ;IF OK THEN CONTINUE
13325 035030 ERRDF 1,GDALRG,ROEROR ;REGISTER 0 NOT EQUAL EXPECTED
13326 035030 104455 TRAP C$ERDF
13327 035032 000001 .WORD 1
13328 035034 002406 .WORD GDALRG
13329 035036 004754 .WORD ROEROR
13330 035040 CKLOOP
  
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13331 035040 104406          TRAP  C$CLP1
13332 035042 000416          BR    9$                ;PROCEED IF LOOPING NOT INVOKED
13333
13334          ;READ AND CHECK GDAL BITS 2:0 AND GDAL BIT 15 FOR ALL ZEROS.
13335
13336 035044 013737 002310 002322 8$:  MOV    IDDEV,ROGOOD        ;GET USER DEFINED DEVICE NUMBER
13337 035052 013737 002322 002320  MOV    ROGOOD,ROLOAD      ;SETUP EXPECTED DATA
13338 035060 004737 006570          JSR    PC,READRO         ;READ AND CHECK REG 0
13339 035064 001405          BEQ    9$                ;IF ALL ZEROS THEN CONT.
13340 035066          ERRDF  1,GDALRG,ROEROR    ;REGISTER 0 NOT EQUAL 0
13341 035066 104455          TRAP  C$ERDF
13342 035070 000001          .WORD 1
13343 035072 002406          .WORD GDALRG
13344 035074 004754          .WORD ROEROR
13345 035076          CKLOOP
13346 035076 104406          TRAP  C$CLP1
13347
13348          ;READ AND CHECK BITS ADAL15 H - ADALO H FOR ALL ZEROS.
13349
13350 035100 005037 002330          9$:  CLR    R2LOAD            ;SETUP EXPECTED DATA
13351 035104 004737 006622          JSR    PC,READR2        ;READ AND CHECK REG 2
13352 035110 001405          BEQ    10$              ;IF ALL ZEROS THEN CONT
13353 035112          ERRDF  2,ADALRG,R2EROR  ;REG 2 NOT EQUAL TO 0
13354 035112 104455          TRAP  C$ERDF
13355 035114 000002          .WORD 2
13356 035116 002513          .WORD ADALRG
13357 035120 004770          .WORD R2EROR
13358 035122          CKLOOP
13359 035122 104406          TRAP  C$CLP1
13360
13361          ;READ AND CHECK BITS VDAL7 H, VDAL2 H - VDALO H FOR ALL ZEROS.
13362
13363 035124 005037 002336          10$: CLR    R4GOOD            ;SETUP EXPECTED DATA
13364 035130 004737 006654          JSR    PC,READR4        ;GO READ AND CHECK REG 4
13365 035134 001405          BEQ    11$              ;IF ALL ZEROS THEN CONT
13366 035136          ERRDF  3,VDALRG,R4EROR  ;VDAL REGISTER NOT EQUAL EXPECTED
13367 035136 104455          TRAP  C$ERDF
13368 035140 000003          .WORD 3
13369 035142 002537          .WORD VDALRG
13370 035144 005004          .WORD R4EROR
13371 035146          CKLOOP
13372 035146 104406          TRAP  C$CLP1
13373
13374          ;SET GDAL1 AND GDALO TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
13375          ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13376
13377 035150 004737 006754          11$: JSR    PC,SLHDAL          ;SELECT HDAL REG VIA GDAL BITS 2:0
13378
13379          ;READ AND CHECK HDAL REGISTER BITS 15:0 FOR A DATA PATTERN OF ALL
13380          ;ZEROS BY ISSUING A READ COMMAN TO CONTRO REGISTER 6 WITH GDAL1 AND
13381          ;GDALO SET IN CONTROL REGISTER 0.
13382
13383 035154 005037 002342          CLR    R6LOAD            ;SETUP EXPECTED DATA
13384 035160 004737 006700          JSR    PC,READR6        ;READ AND CHECK REG 6
13385 035164 001405          BEQ    12$              ;IF ALL ZEROS THEN CONT.
13386 035166          ERRDF  4,HDALRG,R06ERR  ;HDAL REGISTER NOT EQUAL 0

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13387 035166 104455 TRAP C$ERDF
13388 035170 000004 .WORD 4
13389 035172 002605 .WORD HDALRG
13390 035174 005020 .WORD R06ERR
13391 035176 CKLOOP
13392 035176 104406 TRAP C$CLP1
13393
13394 ;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
13395 ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13396
13397 035200 004737 007006 12$: JSR PC,SLMODR ;GO SELECT MODE REG VIA GDAL BITS 2:0
13398
13399 ;READ AND CHECK MODE REGISTER BITS 15:0 FOR A DATA PATTERN OF ALL
13400 ;ZEROS BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13401 ;WITH GDAL2 SET IN CONTROL REGISTER 0.
13402
13403 035204 005037 002342 CLR R6LOAD ;SETUP EXPECTED DATA
13404 035210 004737 006700 JSR PC,READR6 ;READ AND CHECK REG 6
13405 035214 001405 BEQ 13$ ;IF LOADED OK THEN CONT.
13406 035216 ERRDF 4,MODREG,R06ERR ;MODE REG NOT EQUAL 0
13407 035216 104455 TRAP C$ERDF
13408 035220 000004 .WORD 4
13409 035222 002631 .WORD MODREG
13410 035224 005020 .WORD R06ERR
13411 035226 CKLOOP
13412 035226 104406 TRAP C$CLP1
13413
13414 ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
13415 ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13416
13417 035230 004737 007154 13$: JSR PC,SLFDAL ;GO SELECT FDAL REG VIA GDAL BITS 2:0
13418
13419 ;READ AND CHECK FDAL REGISTER BITS 7:0 FOR A DATA PATTERN OF ALL ZEROS
13420 ;BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1
13421 ;SET TO A ONE IN CONTROL REGISTER 0.
13422
13423 035234 012737 177400 002346 MOV #177400,R6MASK ;SETUP TO IGNORE HIGH BYTE
13424 035242 005037 002342 CLR R6LOAD ;SETUP EXPECTED DATA
13425 035246 004737 006700 JSR PC,READR6 ;READ AND CHECK REG 6
13426 035252 001404 BEQ 14$ ;IF DATA LOADED OK THEN CONT
13427 035254 ERRDF 4,FDALRG,R06ERR ;FDAL REGISTER NOT EQUAL TO 0
13428 035254 104455 TRAP C$ERDF
13429 035256 000004 .WORD 4
13430 035260 002653 .WORD FDALRG
13431 035262 005020 .WORD R06ERR
13432 035264 14$: ENDSUB
13433 035264 L10077:
13434 035264 104403 TRAP C$ESUB
13435
13436 ;CHECK TO SEE IF PAUSE STATE WORKING FLIP-FLOP CAN BE SET TO ONE AND
13437 ;THEN CLEARED BY INITO H. ALSO CHECK TO SEE IF SINGLE STEP BREAK FLIP-
13438 ;FLOP CAN BE SET TO ONE AND THEN CLEARED BY INITO L.
13439
13440 035266 BGNSUB
13441 035266 T44.2:
13442 035266 104402 TRAP C$BSUB

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13443
13444 ;SET VDAL2 H TO A ONE AND THEN A ZERO. VDAL2 H ON A ONE WILL CLEAR
13445 ;THE PAUSE STATE MACHINE FLIP-FLOPS, AND PRESET THE SINGLE STEP SYNC
13446 ;FLIP-FLOP.
13447
13448 035270 005037 002334 CLR R4LOAD ;SETUP TO CLEAR ALL VDAL BITS
13449 035274 004737 007712 JSR PC,CLRPSM ;GO PULSE VDAL2 H
13450
13451 ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
13452
13453 035300 012737 000200 002334 MOV #VDAL7,R4LOAD ;SETUP BIT TO SET FETCT H TO HIGH STATE
13454 035306 004737 006640 JSR PC,LDRDR4 ;GO LOAD, READ AND CHECK REG 4
13455 035312 001405 BEQ 1$ ;IF LOADED OK THEN CONT
13456 035314 ERRDF 3,VDALRG,R4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
13457 035314 104455 TRAP C$ERDF
13458 035316 000003 .WORD 3
13459 035320 002537 .WORD VDALRG
13460 035322 005004 .WORD R4EROR
13461 035324 CKLOOP
13462 035324 104406 TRAP C$CLP1
13463
13464 ;LOAD, READ AND CHECK ADAL REGISTER. ADAL8 H ON A ZERO WILL DISABLE THE
13465 ;TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK CONDITION. ADAL4 H ON A ZERO
13466 ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN
13467 ;THE SIGNAL XRAS H IS PULSED. ADAL5 H ON A ONE WILL ENABLE A ONE TO BE
13468 ;CLOCKED INTO THE SINGLE STEP BREAK FLIP-FLOP WHEN XRAS H IS PULSED.
13469 ;ADALO H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC.
13470
13471 035326 012737 000040 002330 1$: MOV #ADAL5,R2LOAD ;SETUP BIT TO BE LOADED
13472 035334 004737 007772 JSR PC,BRKRES ;GO PULSE ADALO H TO CLEAR BREAK LOGIC
13473
13474 ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDALO
13475 ;TO ONES.
13476
13477 035340 004737 006754 JSR PC,SLHDAL ;GO SELECT HDAL REG VIA GDAL 2:0
13478
13479 ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. THE SIGNAL
13480 ;XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS HIGH, INTO
13481 ;THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE.
13482 ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SINGLE STEP SYNC FLIP-
13483 ;FLOP, WHICH IS HIGH, INTO THE SINGLE STEP BREAK FLIP-FLOP WHEN ADAL5 H
13484 ;AND FETCT H ARE ONES, THUS SETTING THE SIGNAL SSBK H TO THE HIGH STATE.
13485 ;WHEN SSBK H IS SET HIGH THE SIGNAL BRK H WILL ALSO BE SET HIGH. WHEN
13486 ;THE SIGNALS BRK H AND FETCT H ARE BOTH SET HIGH THE PAUSE STATE MACHINE
13487 ;WILL BE IN THE PAUSE MODE, THUS SETTING SOP H TO THE HIGH STATE. WHEN
13488 ;THE SIGNALS SOP H AND EDFET H ARE BOTH SET HIGH THE PAUSE STATE WORKING
13489 ;FLIP-FLOP WILL BE DIRECTLY SET TO THE HIGH STATE, THUS SETTING THE SIGNAL
13490 ;PSMW H TO THE HIGH STATE.
13491
13492 035344 005037 002346 CLR R6MASK ;SETUP TO READ ALL BITS
13493 035350 005037 002342 CLR R6LOAD ;CLEAR OUT OLD DATA
13494 035354 004737 007272 JSR PC,XRAS ;GO PULSE XRAS H VIA SIGNAL HDAL12
13495
13496 ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE WORKING FLIP-
13497 ;FLOP IS SET TO A ONE.
13498

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TEST 44: INITO L AND INITO H LOGIC TEST

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13499 035360 052737 001200 002336      BIS      #VDAL9!VDAL7,R4GOOD      ;SETUP BITS TO BE READ
13500 035366 004737 006654              JSR      PC,READR4              ;GO READ VDAL REG
13501 035372 001405                      BEQ      2$                     ;IF OK THEN CONT
13502 035374                      ERRDF   3,VDALRG,R4EROR        ;PSMW H PROBABLY NOT SET IN VDAL REG
13503 035374 104455                      TRAP    C$ERDF
13504 035376 000003                      .WORD   3
13505 035400 002537                      .WORD   VDALRG
13506 035402 005004                      .WORD   R4EROR
13507 035404                      CKLOOP
13508 035404 104406                      TRAP    C$CLP1
13509
13510                      ;READ THE GDAL REGISTER AND CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
13511                      ;IS SET TO A ONE.
13512
13513 035406 052737 000200 002322 2$:    BIS      #GDAL7,ROGOOD          ;SETUP EXPECTED BITS
13514 035414 004737 006570              JSR      PC,READRO            ;GO READ GDAL REG
13515 035420 001405                      BEQ      3$                     ;IF OK THEN CONT.
13516 035422                      ERRDF   1,GDALRG,ROEROR        ;GDAL REGISTER NOT EQUAL EXPECTED
13517 035422 104455                      TRAP    C$ERDF
13518 035424 000001                      .WORD   1
13519 035426 002406                      .WORD   GDALRG
13520 035430 004754                      .WORD   ROEROR
13521 035432                      CKLOOP
13522 035432 104406                      TRAP    C$CLP1
13523
13524                      ;ISSUE A BRESET INSTRUCTION
13525
13526 035434                      3$:    BRESET                    ;ASSERT INITO L AND INITO H
13527 035434 104433                      TRAP    C$RESET
13528 035436                      SETVEC  #4,#4$,#PRI07
13529 035436 012746 000340                  MOV     #PRI07,-(SP)
13530 035442 012746 035510                  MOV     #4,-(SP)
13531 035446 012746 000004                  MOV     #4,-(SP)
13532 035452 012746 000003                  MOV     #3,-(SP)
13533 035456 104437                      TRAP    C$SVEC
13534 035460 062706 000010                  ADD     #10,SP
13535 035464 013705 002300                  MOV     REG0,R5                ;SAVE ADDRESS OF REG 0
13536 035470 113765 002311 000001          MOVB   IDDEV+1,1(R5)           ;SAVE ID NUMBER
13537 035476 000240                      NOP
13538 035500                      CLRVEC #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13539 035500 012700 000004                  MOV     #4,R0
13540 035504 104436                      TRAP    C$CVEC
13541 035506 000420                      BR      5$                      ;NO TIMEOUT OCCURED - CONTINUE
13542
13543                      ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS DEVICE #0
13544                      ;IN THE SYSTEM, THEREFORE, THE TARGET EMULATOR HAS TO BE RESELECTED BY
13545                      ;DOING A 'MOV WORD' OPERATION. A 'MOVB' OPERATION PERFORMED ABOVE DOES
13546                      ;A READ/MODIFY WRITE. THEREFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM,
13547                      ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13548
13549 035510 005726                      4$:    TST     (SP)+              ;CLEAN UP STACK AFTER DEVICE TIMEOUT
13550 035512 005726                      TST     (SP)+
13551 035514                      CLRVEC #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13552 035514 012700 000004                  MOV     #4,R0
13553 035520 104436                      TRAP    C$CVEC
13554 035522 013737 002310 002320          MOV     IDDEV,ROLOAD          ;GET THE DEVICE NUMBER

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13555 035530 004737 006554      JSR    PC,LDRDRO      ;GO LOAD, READ AND CHECK REGISTER 0
13556 035534 001405              BEQ    5$             ;IF LOADED OK THEN CONTINUE
13557 035536              ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
13558 035536 104455      TRAP  C$ERDF
13559 035540 000001      .WORD 1
13560 035542 002406      .WORD GDALRG
13561 035544 004754      .WORD ROEROR
13562 035546      CKLOOP
13563 035546 104406      TRAP  C$CLP1
13564
13565              ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE WORKING
13566              ;FLIP-FLOP IS NOW SET TO A ZERO.
13567
13568 035550 005037 002336      5$: CLR    R4GOOD      ;SETUP BITS TO BE READ
13569 035554 004737 006654      JSR    PC,READR4     ;GO READ VDAL REG
13570 035560 001405      BEQ    6$             ;IF OK THEN CONT.
13571 035562              ERRDF  3,VDALRG,R4EROR ;VDAL REG NOT EQUAL EXPECTED
13572 035562 104455      TRAP  C$ERDF
13573 035564 000003      .WORD 3
13574 035566 002537      .WORD VDALRG
13575 035570 005004      .WORD R4EROR
13576 035572      CKLOOP
13577 035572 104406      TRAP  C$CLP1
13578
13579              ;READ THE GDAL REGISTER AND CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
13580              ;IS NOW SET TO A ZERO.
13581
13582 035574 105037 002322      6$: CLRB   R0GOOD     ;SETUP EXPECTED BITS
13583 035600 004737 006570      JSR    PC,READRO    ;GO READ GDAL REG
13584 035604 001404      BEQ    7$             ;IF OK THEN CONT.
13585 035606              ERRDF  1,GDALRG,ROEROR ;GDAL REGISTER NOT EQUAL EXPECTED
13586 035606 104455      TRAP  C$ERDF
13587 035610 000001      .WORD 1
13588 035612 002406      .WORD GDALRG
13589 035614 004754      .WORD ROEROR
13590 035616      ENDSUB
13591 035616              7$:
13592 035616 104403      L10100: TRAP  C$ESUB
13593
13594 035620              ENDTST
13595 035620              L10076:
13596 035620 104401      TRAP  C$ETST
```

TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODES

.SBTTL TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODES

:+
: THIS TEST WILL CHECK THAT THE T-11 CAN BE POWERED UP TO ALL ITS STARTING
: ADDRESSES AND THAT IT CAN RUN WITH DIFFERENT MODES SELECTED. THE PROGRAM WILL
: USE THE PAUSE STATE MACHINE TO CHECK THAT THE T-11 POWERED UP TO THE
: STARTING ADDRESS SELECTED BY THE MODE REGISTER. THE PROGRAM WILL SELECT THE
: FOLLOWING T-11 MODES: 16 BIT STATIC, 16 BIT DYNAMIC 4K/16K, 16 BIT DYNAMIC 64K,
: 8 BIT STATIC, 8 BIT DYNAMIC 4K/16K AND 8 BIT DYNAMIC 64K. FOR EACH MODE
: SELECTED, THE PROGRAM WILL CHECK THAT THE T-11 CAN BE POWERED UP AT EACH OF
: ITS STARTING ADDRESSES. THE PROGRAM WILL SELECT THE CLOCK ON THE TARGET
: EMULATOR MODULE TO PROVIDE THE TIMING TO THE T-11 CHIP. THE TEST WILL ALSO
: CHECK THAT THE NEW FORCE JUMP ADDRESS REGISTER CAN BE LOADED AND THAT ITS
: CONTENTS CAN BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER.
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035622 004737 005510
035626 012701 036266
035632 005002
035634 012703 036304
035640
035640 104404
035642 005037 002330
035646 004737 006614
035652 001405
035654
035654 104455
035656 000002
035660 002513
035662 004770
035664
035664 104406
035666 004737 007772
035672 005037 002334
035676 004737 007712

```
T45::      BGNTST
           JSR      PC,INITTE          ;SELECT AND INITIALIZE TARGET EMULATOR
           MOV      #14$,R1           ;ADDRESS OF T-11 MODE REGISTER TABLE
           CLR      R2                ;T-11 STARTING ADDRESS MODE PARAMTER
           MOV      #15$,R3           ;ADDRESS OF EXPECTED STARTING ADDRESS TABLE

1$:        BGNSEG
           TRAP     C$BSEG

           ;LOAD ADAL REGISTER WITH ALL ZEROES TO TURN OFF THE T-11 CHIP AND
           ;TO DISABLE CERTAIN BUSES FROM OTHER BUSES

           CLR      R2LOAD            ;SETUP TO CLEAR ALL BITS
           JSR      PC,LDRDR2         ;GO LOAD, READ AND CHECK ADAL REGISTER
           BEQ      2$                ;IF LOADED OK THEN CONTINUE
           ERRDF   2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
           TRAP     C$ERDF
           .WORD   2
           .WORD   ADALRG
           .WORD   R2EROR
           CKLOOP
           TRAP     C$CLP1

           ;PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.
           ;THE SIGNAL BRKRES L WILL CLEAR THE BREAK LATCH FLIP-FLOP, THE SINGLE
           ;STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK FLIP-FLOP.

2$:        JSR      PC,BRKRES          ;GO PULSE BRKRES L VIA ADALO H

           ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 4.
           ;A PULSE ON THE SIGNAL INVD L WILL INITIALIZE ALL OTHER FLIP-FLOPS ON
           ;THE MODULE TO A KNOWN STATE EXCEPT FOR THOSE CLEARED BY THE SIGNAL
           ;BRKRES L ABOVE.

           CLR      R4LOAD            ;SETUP TO CLEAR ALL VDAL R/W BITS
           JSR      PC,CLRPSM         ;GO PULSE INVD L VIA VDAL2 H
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13653                                     ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
13654
13655 035702 004737 006754                JSR    PC,SLHDAL                        ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
13656
13657                                     ;CLEAR ALL BITS IN THE HDAL REGISTER. HDAL2 H ON A ZERO WILL ALLOW THE
13658                                     ;T-11 CHIP TO GENERATE ALL THE T-11 TIMING AND CONTROL SIGNALS.
13659
13660 035706 005037 002342                CLR    R6LOAD                          ;SETUP TO CLEAR ALL HDAL BITS
13661 035712 004737 006672                JSR    PC,LDRDR6                       ;GO LOAD, READ AND CHECK HDAL REGISTER
13662 035716 001405                        BEQ    3$                               ;IF LOADED OK THEN CONTINUE
13663 035720                                ERRDF  4,HDALRG,R06ERR                 ;HDAL REGISTER NOT EQUAL EXPECTED
13664 035720 104455                        TRAP   C$ERDF
13665 035722 000004                        .WORD  4
13666 035724 002605                        .WORD  HDALRG
13667 035726 005020                        .WORD  R06ERR
13668 035730                                CKLOOP
13669 035730 104406                        TRAP   C$CLP1
13670
13671                                     ;SELECT THE FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
13672
13673 035732 004737 007154                3$: JSR    PC,SLFDAL                      ;SELECT FDAL AND EOAI REG VIA GDAL 2:0
13674
13675                                     ;SET ALL BITS IN THE EOAI REGISTER TO ZERO. SET FDALO H TO A ONE SO
13676                                     ;THAT THE EOAI REGISTER CAN BE READBACK ON A READ COMMAND TO CONTROL
13677                                     ;REGISTER 6 INSTEAD OF THE CTL REGISTER.
13678
13679 035736 012737 000001 002342          MOV    #FDALO,R6LOAD                   ;SETUP BITS TO BE LOADED
13680 035744 004737 006672                JSR    PC,LDRDR6                       ;LOAD, READ AND CHECK FDAL AND EOAI REG
13681 035750 001405                        BEQ    4$                               ;IF LOADED OK THEN CONTINUE
13682 035752                                ERRDF  4,EOAIFD,R06ERR                 ;EOAI OR FDAL REGISTER ERROR
13683 035752 104455                        TRAP   C$ERDF
13684 035754 000004                        .WORD  4
13685 035756 002676                        .WORD  EOAIFD
13686 035760 005020                        .WORD  R06ERR
13687 035762                                CKLOOP
13688 035762 104406                        TRAP   C$CLP1
13689
13690                                     ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
13691
13692 035764 004737 007006                4$: JSR    PC,SLMODR                    ;SELECT MODE REGISTER VIA GDAL BITS 2:0
13693
13694                                     ;LOAD THE T-11 MODE SELECT PARAMETERS FROM THE MODE TABLE INTO THE
13695                                     ;MODE REGISTER. THESE PARAMETERS WILL BE USED BY THE T-11 CHIP ON
13696                                     ;ITS POWER-UP SEQUENCE.
13697
13698 035770 011137 002342                MOV    (R1),R6LOAD                     ;GET T-11 MODE SELECT PARAMETER
13699 035774 050237 002342                BIS    R2,R6LOAD                       ;ADD STARTING ADDRESS MODE PARAMETER
13700 036000 004737 006672                JSR    PC,LDRDR6                       ;GO LOAD, READ AND CHECK MODE REGISTER
13701 036004 001405                        BEQ    5$                               ;IF LOADED OK THEN CONTINUE
13702 036006                                ERRDF  4,MODREG,R06ERR                 ;MODE REGISTER NOT EQUAL EXPECTED
13703 036006 104455                        TRAP   C$ERDF
13704 036010 000004                        .WORD  4
13705 036012 002631                        .WORD  MODREG
13706 036014 005020                        .WORD  R06ERR
13707 036016                                CKLOOP
13708 036016 104406                        TRAP   C$CLP1

```

TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODES

```

13709
13710
13711
13712
13713
13714
13715
13716
13717
13718
13719
13720
13721
13722
13723 036020 012737 032006 002330 5$: MOV #ADAL13!ADAL12!ADAL10!ADAL2!ADAL1,R2LOAD ;SETUP BITS TO BE LOADED
13724 036026 004737 006614 JSR PC,LDRDR2 ;GO LOAD, READ AND CHECK ADAL REGISTER
13725 036032 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
13726 036034 ERRDF 2,ADALRG,R2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
13727 036034 104455 TRAP C$ERDF
13728 036036 000002 .WORD 2
13729 036040 002513 .WORD ADALRG
13730 036042 004770 .WORD R2EROR
13731 036044 CKLOOP
13732 036044 104406 TRAP C$CLP1
13733
13734
13735
13736
13737
13738
13739 036046 012705 000002 6$: MOV #2,R5 ;SETUP DOUBLE PRECISION COUNTER
13740 036052 005004 CLR R4 ;CLEAR SINGLE PRECISSION COUNTER
13741 036054 032777 001000 144222 7$: BIT #VDAL9,@REG4 ;CHECK PAUSE STATE WORKING F/F
13742 036062 001011 BNE 8$ ;IF SET THEN PAUSE STATE ENTERED
13743 036064 005304 DEC R4 ;DECREMET FIRST COUNTER
13744 036066 001372 BNE 7$ ;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
13745 036070 005305 DEC R5 ;DECREMENT DOUBLE PRECISSION COUNTER
13746 036072 001370 BNE 7$ ;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
13747 036074 ERRDF 5,NOPSM,R026ER ;PAUSE STATE NOT ENTERED WHEN T-11 IS ON
13748 036074 104455 TRAP C$ERDF
13749 036076 000005 .WORD 5
13750 036100 003773 .WORD NOPSM
13751 036102 005034 .WORD R026ER
13752 036104 CKLOOP
13753 036104 104406 TRAP C$CLP1
13754
13755
13756
13757
13758
13759
13760
13761
13762 036106 004737 007040 8$: JSR PC,SLFJAR ;SELECT FJA REG VIA GDAL BITS 2:0
13763
13764 ;READ THE FORCE JUMP ADDRESS READBACK REGISTER BACK TO THE LSI-11
  
```

```

;SET ADAL REGISTER BITS 13, 12, 10, 2, AND 1 TO ONES AND ALL OTHER ADAL
;REGISTER BITS TO ZEROES. ADAL12 H ON A ONE WILL ENABLE THE MODE
;REGISTER TO THE T-11 CHIP WHEN THE SIGNAL PBCLR H IS ASSERTED HIGH
;AND THE T-11 IS IN ITS POWER-UP SEQUENCE. ADAL10 H ON A ONE WILL
;ENABLE THE EIAI BUS TO THE CTL BUS AND THE EIDAL BUS TO THE ADDRESS
;BUS. ADAL2 H ON A ONE WILL CAUSE THE SIGNAL CPUP L TO BE ASSERTED
;LOW. WHEN CPUP L IS ASSERTED LOW, THE T-11 CHIP WILL START ITS POWER-
;UP SEQUENCE. ADAL1 H ON A ONE WILL SELECT THE 5.068 MHZ CLOCK ON THE
;TARGET EMULATOR MODULE. ADAL4 H ON A ZERO WILL CAUSE THE PAUSE STATE
;MACHINE TO BE IN PAUSE MODE ON THE FIRST PULSE OF XRAS H.
;ADAL13 H ON A ONE WILL ALLOW THE T-11 TO EXAMINE THE AI LINES DURING
;THE T-11 POWER UP SEQUENCE.
  
```

```

;SETUP TIMEOUT COUNTERS TO WAIT FOR THE PAUSE STATE MACHINE TO BE
;ENTERED. THE PAUSE STATE WORKING FLIP-FLOP SHOULD BE SET WHEN THE
;T-11 CAUSES THE SIGNAL FETCT H TO BE ASSERTED HIGH AND THE T-11
;GENERATES A PULSE ON THE SIGNAL XRAS H.
  
```

```

;SETUP DOUBLE PRECISION COUNTER
;CLEAR SIGNLE PRECISSION COUNTER
;CHECK PAUSE STATE WORKING F/F
;IF SET THEN PAUSE STATE ENTERED
;DECREMET FIRST COUNTER
;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
;DECREMENT DOUBLE PRECISSION COUNTER
;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
;PAUSE STATE NOT ENTERED WHEN T-11 IS ON
  
```

```

;READ THE FORCE JUMP ADDRESS REGISTER TO CHECK THAT THE T-11 PLACED
;THE CORRECT STARTING ADDRESS ONTO THE ADDRESS BUS FOR THE MODE
;SELECTED IN THE MODE REGISTER. THE ADDRESS BUS IS CLOCKED INTO
;THE FORCE JUMP ADDRESS READBACK REGISTER WHEN THE EDFET FLIP-FLOP
;IS SET TO A ONE AND A PULSE IS ISSUED ON THE SIGNAL RASP H. THE
;CLOCKING SIGNAL GENERATED IS CALLED DFET H.
  
```

```

13765
13766 036112 011337 002342      MOV      (R3),R6LOAD      ;GET EXPECTED ADDRESS FROM THE TABLE
13767 036116 004737 006700      JSR      PC,READR6        ;READ FJA READBACK REGISTER AND CHECK IT
13768 036122 001405                BEQ      9$                ;IF STARTING ADDRESS = EXPECTED - CONT
13769 036124                ERRDF   5,FJSTAD,R026ER    ;FJA NOT EQUAL EXPECTED T-11 STARTING ADDRESS
13770 036124 104455                TRAP    C$ERDF
13771 036126 000005                .WORD   5
13772 036130 004060                .WORD   FJSTAD
13773 036132 005034                .WORD   R026ER
13774 036134                CKLOOP
13775 036134 104406                TRAP    C$CLP1
13776
13777
13778 ;THE TEST WILL NOW LOAD THE NEW FORCE JUMP ADDRESS REGISTER WITH AN
13779 ;ADDRESS DIFFERENT FROM THE STARTING ADDRESS THAT THE T-11 POWERED UP
13780 ;WITH. THE NEW ADDRESS LOADED WILL CORRESPOND TO ONE OF THE FOLLOWING:
13781 ; IF STARTING ADDRESS = 140000 THEN NEW ADDRESS = 037777
13782 ; IF STARTING ADDRESS = 100000 THEN NEW ADDRESS = 052525
13783 ; IF STARTING ADDRESS = 040000 THEN NEW ADDRESS = 125252
13784 ; IF STARTING ADDRESS = 020000 THEN NEW ADDRESS = 146314
13785 ; IF STARTING ADDRESS = 010000 THEN NEW ADDRESS = 031463
13786 ; IF STARTING ADDRESS = 000000 THEN NEW ADDRESS = 177777
13787 ; IF STARTING ADDRESS = 173000 THEN NEW ADDRESS = 004777
13788 ; IF STARTING ADDRESS = 172000 THEN NEW ADDRESS = 005777
13789 036136 016377 000020 144142 9$:  MOV      20(R3),@REG6      ;WRITE NEW FORCE JUMP ADDRESS REGISTER
13790                                ;WITH NEW ADDRESS FROM TABLE
13791
13792 ;READ THE FORCE JUMP ADDRESS READBACK REGISTER TO CHECK THAT THE NEW
13793 ;FORCE JUMP ADDRESS WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER
13794
13795 036144 016337 000020 002342      MOV      20(R3),R6LOAD      ;GET ADDRESS LOADED INTO NEW FJA REG
13796 036152 012704 000004                MOV      #4,R4              ;SETUP TO READ 4 TIMES BEFORE FLAGGING
13797                                ;THAT AN ERROR OCCURED
13798 036156 017737 144124 002344 10$:  MOV      @REG6,R6READ        ;READ FJA READBACK REGISTER
13799 036164 023737 002342 002344      CMP      R6LOAD,R6READ      ;CHECK DATA LOADED AGAINST DATA READ
13800 036172 001407                BEQ      11$                ;IF LOADED OK THEN CONTINUE
13801 036174 005304                DEC      R4                  ;CHECK IF ALLOTTED READS OCCURED
13802 036176 001367                BNE     10$                  ;IF NOT THEN READ FJA READBACK REG AGAIN
13803 036200                ERRDF   5,FJADRG,R026ER    ;NEW FJA NOT LOADED INTO OLD FJA REG
13804 036200 104455                TRAP    C$ERDF
13805 036202 000005                .WORD   5
13806 036204 002766                .WORD   FJADRG
13807 036206 005034                .WORD   R026ER
13808 036210                CKLOOP
13809 036210 104406                TRAP    C$CLP1
13810
13811 ;CLEAR ALL ADAL REGISTER BITS. THIS WILL TURN THE T-11 CHIP OFF AGAIN.
13812
13813 036212 005037 002330 11$:  CLR      R2LOAD              ;SETUP TO CLEAR ALL ADAL REGISTER BITS
13814 036216 004737 006614                JSR      PC,LDRDR2          ;GO LOAD, READ AND CHECK ADAL REGISTER
13815 036222 001404                BEQ      12$                ;IF LOADED OK THEN CONTINUE
13816 036224                ERRDF   2,ADALRG,R2EROR    ;ADAL REGISTER NOT EQUAL EXPECTED
13817 036224 104455                TRAP    C$ERDF
13818 036226 000002                .WORD   2
13819 036230 002513                .WORD   ADALRG
13820 036232 004770                .WORD   R2EROR

```

TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODES

```
13821 036234          12$:  ENDSEG
13822 036234          10000$:
13823 036234 104405   TRAP    C$ESEG
13824
13825 036236 062702 020000   ADD    #BIT13,R2      ;UPDATE T-11 STARTING ADDRESS PARAMETER
13826 036242 001403          BEQ    13$            ;IF DONE THEN CONTINUE
13827 036244 005723          TST   (R3)+          ;UPDATE STARTING ADDRESS TABLE POINTER
13828 036246 000137 035640   JMP    1$            ;GO LOAD AND CHECK NEXT ADDRESS IN THIS MODE
13829
13830 036252 012703 036304   13$:  MOV    #15$,R3      ;RESET STARTING ADDRESS TABLE POINTER
13831 036256 005721          TST   (R1)+          ;UPDATE TABLE MODE PARAMETER POINTER
13832 036260 001431          BEQ    16$            ;IF 0 THEN EXIT THE TEST
13833 036262 000137 035640   JMP    1$            ;GO LOAD NEXT PARAMETER
13834
13835                  ;T-11 MODE SELECT PARAMTER TABLE WITHOUT STARTING ADDRESS PARAMTER
13836
13837 036266 011003          14$:  .WORD  011003      ;16 BIT STATIC MODE
13838 036270 012003          .WORD  012003      ;16 BIT DYNAMIC MODE 4/16 K
13839 036272 010003          .WORD  010003      ;16 BIT DYNAMIC MODE 64K
13840 036274 015003          .WORD  015003      ;8 BIT STATIC MODE
13841 036276 016003          .WORD  016003      ;8 BIT DYNAMIC MODE 4/16K
13842 036300 014003          .WORD  014003      ;8 BIT BYNAMIC MODE 64K
13843 036302 000000          .WORD  0           ;TABLE TERMINATOR
13844
13845                  ;EXPECTED T-11 STARTING ADDRESS TABLE
13846
13847 036304 140000          15$:  .WORD  140000
13848 036306 100000          .WORD  100000
13849 036310 040000          .WORD  040000
13850 036312 020000          .WORD  020000
13851 036314 010000          .WORD  010000
13852 036316 000000          .WORD  000000
13853 036320 173000          .WORD  173000
13854 036322 172000          .WORD  172000
13855
13856                  ;ADDRESSES TO BE LOADED INTO NEW FORCE JUMP ADDRESS REGISTER
13857
13858 036324 037777          .WORD  037777
13859 036326 052525          .WORD  052525
13860 036330 125252          .WORD  125252
13861 036332 146314          .WORD  146314
13862 036334 031463          .WORD  031463
13863 036336 177777          .WORD  177777
13864 036340 004777          .WORD  004777
13865 036342 005777          .WORD  005777
13866
13867 036344          16$:  ENDTST
13868 036344          L10101:
13869 036344 104401          TRAP    C$ETST
13870
13871 036346          ENDMOD
13872
```



```

13873
13874
13875
13876
13877 036346
13878
13879
13880
13881
13882
13883
13884
13885
13886
13887
13888 036346
13889 036346 000015
13890 036350
13891
13892
13893
13894
13895
13896
13897
13898
13899
13900 036350
13901 036350 000031
13902 036352 036402
13903 036354 160000
13904 036356 177770
13905 036360
13906 036360 001031
13907 036362 036416
13908 036364 000370
13909 036366 000370
13910 036370
13911 036370 002032
13912 036372 036435
13913 036374 177777
13914 036376 000000
13915 036400 000017
13916
13917
13918
13919 036402
13920
13921 036402

```

```

.TITLE PARAMETER CODING
.SBTTL  HARDWARE PARAMETER CODING SECTION
      BGNMOD
      :
      :++
      : THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
      : THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
      : MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
      : INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
      : MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
      : WITH THE OPERATOR.
      :--
      BGNHRD
      .WORD L10102-L$HARD/2
L$HARD::
      :
      : HARDWARE P-TABLE QUESTIONS
      :
      : ASK FOR CDS TARGET EMULATOR CSR ADDRESS
      : ASK FOR CDS TARGET EMULATOR VECTOR ADDRESS
      : ASK FOR CDS TARGET EMULATOR DEVICE NUMBER
      :
      GPRMA  MSG1,0,0,160000,177770,YES
      .WORD  T$CODE
      .WORD  MSG1
      .WORD  T$LLOLIM
      .WORD  T$HILIM
      GPRMA  MSG2,2,0,000370,000000370,YES
      .WORD  T$CODE
      .WORD  MSG2
      .WORD  T$LLOLIM
      .WORD  T$HILIM
      GPRMD  MSG3,4,0,177777,0,000017,YES
      .WORD  T$CODE
      .WORD  MSG3
      .WORD  177777
      .WORD  T$LLOLIM
      .WORD  T$HILIM
      ENDHRD
      .EVEN
L10102:

```

```

13922
13923
13924
13925
13926
13927 036402 051503 020122 042101 MSG1: .ASCIZ /CSR ADDRESS/
13928 036410 051104 051505 000123
13929 036416 042526 052103 051117 MSG2: .ASCIZ /VECTOR ADDRESS/
13930 036424 040440 042104 042522
13931 036432 051523 000
13932 036435 104 053105 041511 MSG3: .ASCIZ /DEVICE NUMBER/
13933 036442 020105 052516 041115
13934 036450 051105 000
13935
13936
13937
13938
13939
13940
13941
13942
13943
13944
13945
13946
13947
13948 036454
13949 036454 000000
13950 036456
13951
13952
13953
13954
13955 036456
13956
13957 036456
13958
13959
13960
13961 036456
13962 036456 000030
13963
13964
13965 036536
13966
13967 036536 036554
13968 036540 000005
13969 036542
13970 036542
13971
13972
13973
13974 036542
13975 036542
13976 036542 000000
13977 036544 000003
  
```

Hardware P-Table Messages

.SBTTL SOFTWARE PARAMETER CODING SECTION

++
 : THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS
 : THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES. THE
 : MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
 : INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES. THE
 : MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
 : WITH THE OPERATOR.
 --

```

          BGNSFT
          .WORD L10103-L$SOFT/2
L$SOFT::
          .EVEN
          ENDSFT
          .EVEN
L10103:
$PATCH::
          .BLKW 30
          LASTAD
          .EVEN
          .WORD T$FREE
          .WORD T$SIZE
L$LAST::
          ENDMOD
          BGNSETUP          1.
          BGNPTAB
          .WORD 0
          .WORD L10106-./2-1
  
```

13978 036546
13979 036546 163010
13980 036550 000370
13981 036552 000002
13982 036554
13983 036554
13984 036554
13985 000001

L10104:
.WORD 163010
.WORD 370
.WORD 2
ENDPTAB
L10106:
ENDSETUP
.END

ADALRG	002513	G	1906#	2582	2605	3149	3159	3588	3605	3638	3656	3686	3718	4900	5348
			5824	6345	6373	6497	6567	6680	6721	6752	6891	7258	9297	9477	9633
			9865	10315	10419	10558	10675	10739	10767	11376	11801	11862	11952	12303	12409
			12444	12557	12779	12867	13063	13198	13356	13634	13729	13819			
ADALO =	000001	G	1705#	2574	3143	3153	5342	5818	9859	10669					
ADAL1 =	000002	G	1704#	13723											
ADAL10 =	002000	G	1693#	9291	9627	9859	10669	10733	10761	11370	11795	13723			
ADAL11 =	004000	G	1692#												
ADAL12 =	010000	G	1691#	4894	9627	13723									
ADAL13 =	020000	G	1690#	9291	9471	9859	10309	10413	13723						
ADAL14 =	040000	G	1688#												
ADAL15 =	100000	G	1687#												
ADAL2 =	000004	G	1703#	13723											
ADAL3 =	000010	G	1702#												
ADAL4 =	000020	G	1700#	6339	6885	11946	12551								
ADAL5 =	000040	G	1698#	6885	7252	13471									
ADAL6 =	000100	G	1697#												
ADAL7 =	000200	G	1696#	12297	12403	12438	12551								
ADAL8 =	000400	G	1695#	3692	3723	6367	6491	6561	6674	6715	6746	12773	12861	13057	
ADAL9 =	001000	G	1694#	11856											
ADDRRG	002735	G	1941#	4531	4555	4634	4658	4741	4826	5056	5141	5332	5808	7551	8262
			9848												
ADDR0 =	000001	G	1809#												
ADDR1 =	000002	G	1808#												
ADDR10 =	002000	G	1799#												
ADDR11 =	004000	G	1798#												
ADDR12 =	010000	G	1797#												
ADDR13 =	020000	G	1796#												
ADDR14 =	040000	G	1795#												
ADDR15 =	100000	G	1794#												
ADDR2 =	000004	G	1807#												
ADDR3 =	000010	G	1806#												
ADDR4 =	000020	G	1805#												
ADDR5 =	000040	G	1804#												
ADDR6 =	000100	G	1803#												
ADDR7 =	000200	G	1802#												
ADDR8 =	000400	G	1801#	4831											
ADDR9 =	001000	G	1800#												
ADR =	000020	G	1637#												
ASSEMB =	000010		1368												
BIT0 =	000001	G	1610#	1676	1705	1726	1752	1774	1787	1809					
BIT00 =	000001	G	1599#	1610											
BIT01 =	000002	G	1598#	1609											
BIT02 =	000004	G	1597#	1608											
BIT03 =	000010	G	1596#	1607											
BIT04 =	000020	G	1595#	1606											
BIT05 =	000040	G	1594#	1605											
BIT06 =	000100	G	1593#	1604											
BIT07 =	000200	G	1592#	1603											
BIT08 =	000400	G	1591#	1602											
BIT09 =	001000	G	1590#	1601											
BIT1 =	000002	G	1609#	1675	1704	1725	1751	1773	1786	1808					
BIT10 =	002000	G	1589#	1665	1693	1716	1737	1764	1799						
BIT11 =	004000	G	1588#	1664	1692	1715	1736	1762	1798						
BIT12 =	010000	G	1587#	1662	1691	1714	1735	1761	1797						
BIT13 =	020000	G	1586#	1661	1690	1713	1734	1760	1796	13825					

BIT14 = 040000 G	1585#	1660	1688	1712	1733	1759	1795							
BIT15 = 100000 G	1584#	1654	1687	1711	1732	1758	1794							
BIT2 = 000004 G	1608#	1674	1703	1724	1748	1772	1785	1807	2983					
BIT3 = 000010 G	1607#	1673	1702	1723	1747	1771	1784	1806						
BIT4 = 000020 G	1606#	1672	1700	1722	1746	1770	1783	1805						
BIT5 = 000040 G	1605#	1671	1698	1721	1745	1769	1782	1804						
BIT6 = 000100 G	1604#	1670	1697	1720	1744	1768	1781	1803						
BIT7 = 000200 G	1603#	1669	1696	1719	1743	1767	1780	1802						
BIT8 = 000400 G	1602#	1667	1695	1718	1742	1766	1801	4456	9567					
BIT9 = 001000 G	1601#	1666	1694	1717	1738	1765	1800							
BOE = 000400 G	1641#													
BRKRES 007772 G	3141#	6829	7033	7145	7195	7348	7563	8275	9014	12655	13096	13472	13643	
CLRPSM 007712 G	3110#	5066	5224	5357	5400	5833	6249	6358	6790	6874	7103	7146	7198	
	7355	7453	7570	7610	8282	8943	9022	9212	9284	9347	9602	9874	10151	
	10407	10686	11306	11387	11673	11741	11829	12045	12595	12665	13449	13651		
CTLFDL 003232 G	1976#	9391	9461	9561										
C\$AU = 000052	1368#	3376												
C\$AUTO= 000061	1368#	3304												
C\$BRK = 000022	1368#													
C\$BSEG= 000004	1368#	2397	2441	2460	2523	2556	2628	2740	2760	2782	2802	2822	2842	
	2862	2882	2911	2931	2962	2982	3011	3030	3059	3078	3111	3142	3446	
	3463	3495	3513	3548	3578	3595	3627	3645	3680	3712	3748	3797	3821	
	3861	3887	3930	3978	4023	4048	4089	4114	4156	4204	4248	4274	4314	
	4340	4381	4428	4487	4538	4590	4641	4696	4781	4856	5006	5272	5746	
	6292	6823	7325	7491	8199	8985	9242	9596	9790	10399	10603	11329	11768	
	12621	13623												
C\$BSUB= 000002	1368#	13187	13442											
C\$CEFG= 000045	1368#													
C\$CLCK= 000062	1368#													
C\$CLEA= 000012	1368#	3332												
C\$CLOS= 000035	1368#													
C\$CLP1= 000006	1368#	2422	2471	2502	2534	2585	2595	2608	2654	2665	3121	3152	4509	
	4612	4718	4803	4888	4903	4926	4949	5032	5059	5103	5126	5144	5158	
	5194	5219	5292	5314	5335	5351	5393	5451	5478	5508	5550	5578	5623	
	5670	5693	5766	5788	5811	5827	5867	5925	5958	5988	6027	6060	6089	
	6123	6163	6212	6237	6310	6329	6348	6376	6391	6405	6434	6449	6471	
	6485	6500	6514	6528	6554	6570	6585	6608	6632	6647	6669	6683	6710	
	6724	6741	6755	6783	6848	6866	6894	6908	6943	6958	6981	6994	7016	
	7028	7047	7060	7083	7095	7123	7138	7159	7187	7212	7232	7246	7261	
	7280	7342	7374	7387	7417	7448	7511	7533	7554	7603	7663	7692	7722	
	7768	7800	7830	7877	7906	7949	7994	8024	8066	8115	8141	8219	8241	
	8265	8316	8374	8409	8439	8481	8515	8546	8583	8613	8661	8692	8733	
	8780	8812	8853	8904	8932	9004	9044	9080	9109	9135	9161	9187	9206	
	9259	9277	9300	9325	9394	9413	9464	9480	9500	9515	9636	9653	9672	
	9695	9714	9809	9831	9851	9868	9888	9949	9985	10018	10046	10081	10118	
	10137	10188	10211	10240	10255	10278	10304	10318	10338	10422	10441	10461	10483	
	10504	10524	10546	10561	10622	10643	10661	10678	10713	10726	10742	10757	10770	
	10784	10801	10815	10834	10847	10870	10893	10915	10933	10953	10969	10983	11004	
	11022	11036	11050	11068	11083	11103	11119	11132	11148	11177	11195	11210	11225	
	11245	11262	11287	11300	11346	11365	11379	11403	11418	11436	11450	11488	11505	
	11515	11532	11559	11574	11591	11619	11636	11667	11690	11707	11735	11786	11804	
	11850	11865	11901	11939	11955	11971	12003	12036	12075	12106	12134	12160	12188	
	12202	12226	12251	12265	12289	12306	12335	12362	12397	12412	12433	12447	12466	
	12499	12513	12538	12560	12590	12647	12705	12720	12735	12757	12782	12797	12812	
	12835	12850	12870	12884	12913	12934	12944	12971	12986	13004	13014	13038	13051	
	13066	13089	13117	13141	13201	13221	13234	13254	13275	13290	13331	13346	13359	

	13372	13392	13412	13462	13508	13522	13563	13577	13637	13669	13688	13708	13732
	13753	13775	13809										
C\$CVEC= 000036	1368#	2433	2513	2598	2668	13154	13308	13321	13540	13553			
C\$DCLN= 000044	1368#												
C\$DODU= 000051	1368#												
C\$DRPT= 000024	1368#												
C\$DU = 000053	1368#	3353											
C\$EDIT= 000003	1368#	1430											
C\$ERDF= 000055	1368#	2417	2427	2447	2466	2497	2507	2529	2547	2580	2590	2603	2619
	2649	2660	2673	2745	2765	2787	2807	2827	2847	2867	2887	2916	2937
	2967	2988	3016	3036	3064	3084	3116	3126	3147	3157	3454	3471	3504
	3522	3552	3586	3603	3636	3654	3684	3716	3758	3812	3831	3877	3898
	3944	3992	4038	4058	4104	4124	4170	4218	4264	4284	4330	4350	4394
	4448	4504	4529	4553	4607	4632	4656	4713	4739	4798	4824	4883	4898
	4921	4944	4966	5027	5054	5098	5121	5139	5153	5189	5212	5287	5309
	5330	5346	5388	5446	5473	5501	5545	5573	5618	5665	5688	5761	5783
	5806	5822	5862	5920	5953	5981	6022	6055	6084	6118	6158	6207	6232
	6305	6324	6343	6371	6386	6400	6429	6444	6466	6480	6495	6509	6523
	6549	6565	6580	6603	6627	6642	6664	6678	6705	6719	6736	6750	6778
	6843	6861	6889	6903	6938	6953	6976	6989	7011	7023	7042	7055	7078
	7090	7118	7133	7154	7182	7207	7227	7241	7256	7275	7290	7337	7369
	7382	7412	7443	7506	7528	7549	7598	7658	7687	7717	7763	7795	7825
	7872	7901	7944	7989	8019	8061	8110	8136	8214	8236	8260	8311	8369
	8404	8434	8476	8510	8541	8578	8608	8656	8687	8728	8775	8807	8848
	8899	8927	8999	9039	9075	9104	9130	9156	9182	9201	9254	9272	9295
	9320	9389	9408	9459	9475	9495	9510	9559	9631	9648	9667	9690	9709
	9744	9804	9826	9846	9863	9883	9944	9980	10013	10041	10076	10113	10132
	10183	10206	10235	10250	10273	10299	10313	10333	10358	10417	10436	10456	10478
	10499	10519	10541	10556	10573	10617	10638	10656	10673	10708	10721	10737	10752
	10765	10779	10796	10810	10829	10842	10865	10888	10910	10928	10948	10964	10978
	10999	11017	11031	11045	11063	11078	11098	11114	11127	11143	11172	11190	11205
	11220	11240	11257	11282	11295	11341	11360	11374	11398	11413	11431	11445	11483
	11500	11510	11527	11554	11569	11586	11614	11631	11662	11685	11702	11730	11781
	11799	11845	11860	11896	11934	11950	11966	11998	12031	12070	12101	12129	12155
	12183	12197	12221	12246	12260	12284	12301	12330	12357	12392	12407	12428	12442
	12461	12494	12508	12533	12555	12585	12642	12699	12715	12729	12751	12777	12792
	12806	12830	12845	12865	12879	12907	12929	12939	12966	12981	12999	13009	13032
	13046	13061	13083	13112	13135	13196	13216	13229	13249	13270	13285	13326	13341
	13354	13367	13387	13407	13428	13457	13503	13517	13558	13572	13586	13632	13664
	13683	13703	13727	13748	13770	13804	13817						
C\$ERHR= 000056	1368#												
C\$ERRO= 000060	1368#												
C\$ERSF= 000054	1368#												
C\$ERSO= 000057	1368#												
C\$ESCA= 000010	1368#												
C\$SEGE= 000005	1368#	2436	2453	2516	2553	2625	2679	2751	2771	2793	2813	2833	2853
	2873	2893	2922	2943	2973	2994	3022	3042	3070	3090	3132	3163	3460
	3477	3510	3528	3558	3592	3609	3642	3660	3690	3722	3764	3818	3837
	3883	3904	3950	3998	4044	4064	4110	4130	4176	4224	4270	4290	4336
	4356	4400	4454	4535	4559	4638	4662	4745	4830	4972	5227	5701	6253
	6794	7296	7457	8150	8947	9216	9565	9750	10364	10579	11310	11745	12599
	13158	13823											
C\$ESUB= 000003	1368#	13434	13592										
C\$ETST= 000001	1368#	3431	3480	3531	3564	3612	3663	3696	3727	3777	3840	3908	3956
	4003	4068	4134	4182	4229	4294	4360	4405	4460	4562	4665	4750	4835
	4988	5243	5717	6269	6797	7299	7460	8167	8965	9219	9572	9766	10380

INITTE 005510 G	2396#	3424	3443	3492	3543	3575	3624	3675	3707	3743	3794	3858	3925
	3973	4020	4086	4151	4199	4245	4311	4376	4424	4484	4587	4692	4777
	4851	5001	5267	5741	6289	6821	7322	7486	8194	8982	9238	9591	9785
	10395	10601	11326	11766	12618	13178	13616						
INTSRV 006724 G	2725#	12673											
ISR = 000100 G	1639#												
IXE = 004000 G	1644#												
ISAU = 000041	1368#	3364#	3377#										
ISAUTO= 000041	1368#	3299#	3305#										
ISCLN = 000041	1368#	3314#	3324	3333#									
ISDU = 000041	1368#	3341#	3354#										
ISHRD = 000041	13889#	13922#											
ISINIT= 000041	1368#	3218#	3280	3289#									
ISMOD = 000041	1368#	1375#	1568#	1573#	3168#	3173#	3379#	3385#	13872#	13878#	13971#		
ISMSG = 000041	1368#	2144#	2151#	2153#	2160#	2162#	2169#	2171#	2178#	2180#	2187#	2189#	2199#
	2201#	2211#	2213#	2223#	2225#	2235#							
ISPROT= 000040	1368#	3202#											
ISPTAB= 000041	1368#	13976#	13983#										
ISPWR = 000041	1368#												
ISRPT = 000041	1368#	3180#	3193#										
ISSEG = 000041	1368#	2397#	2437#	2441#	2454#	2460#	2517#	2523#	2554#	2556#	2626#	2628#	2680#
	2740#	2752#	2760#	2772#	2782#	2794#	2802#	2814#	2822#	2834#	2842#	2854#	2862#
	2874#	2882#	2894#	2911#	2923#	2931#	2944#	2962#	2974#	2982#	2995#	3011#	3023#
	3030#	3043#	3059#	3071#	3078#	3091#	3111#	3133#	3142#	3164#	3423	3442	3446#
	3461#	3463#	3478#	3491	3495#	3511#	3513#	3520#	3542	3548#	3559#	3574	3578#
	3593#	3595#	3610#	3623	3627#	3643#	3645#	3661#	3674	3680#	3691#	3706	3712#
	3723#	3742	3748#	3765#	3793	3797#	3819#	3821#	3838#	3857	3861#	3884#	3887#
	3905#	3924	3930#	3951#	3972	3978#	3999#	4019	4023#	4045#	4048#	4065#	4085
	4089#	4111#	4114#	4131#	4150	4156#	4177#	4198	4204#	4225#	4244	4248#	4271#
	4274#	4291#	4310	4314#	4337#	4340#	4357#	4375	4381#	4401#	4423	4428#	4455#
	4483	4487#	4536#	4538#	4560#	4586	4590#	4639#	4641#	4663#	4691	4696#	4746#
	4776	4781#	4831#	4850	4856#	4973#	5000	5006#	5228#	5266	5272#	5702#	5740
	5746#	6254#	6288	6292#	6795#	6820	6823#	7297#	7321	7325#	7458#	7485	7491#
	8151#	8193	8199#	8948#	8981	8985#	9217#	9237	9242#	9566#	9590	9596#	9751#
	9784	9790#	10365#	10394	10399#	10580#	10600	10603#	11311#	11325	11329#	11746#	11765
	11768#	12600#	12617	12621#	13159#	13176	13186	13441	13614	13623#	13824#		
ISSETU= 000041	1368#	13975#	13976	13985#									
ISSFT = 000041	13949#	13958#											
ISSRV = 000041	1368#	2725#	2733#										
ISSUB = 000041	1368#	3423	3442	3491	3542	3574	3623	3674	3706	3742	3793	3857	3924
	3972	4019	4085	4150	4198	4244	4310	4375	4423	4483	4586	4691	4776
	4850	5000	5266	5740	6288	6820	7321	7485	8193	8981	9237	9590	9784
	10394	10600	11325	11765	12617	13176	13186#	13433#	13435#	13441#	13591#	13593#	13614
ISTST = 000041	1368#	3423#	3430#	3432#	3442#	3479#	3481#	3491#	3530#	3532#	3542#	3563#	3565#
	3574#	3611#	3613#	3623#	3662#	3664#	3674#	3695#	3697#	3706#	3726#	3728#	3742#
	3776#	3778#	3793#	3839#	3841#	3857#	3907#	3909#	3924#	3955#	3957#	3972#	4002#
	4004#	4019#	4067#	4069#	4085#	4133#	4135#	4150#	4181#	4183#	4198#	4228#	4230#
	4244#	4293#	4295#	4310#	4359#	4361#	4375#	4404#	4406#	4423#	4459#	4461#	4483#
	4561#	4563#	4586#	4664#	4666#	4691#	4749#	4751#	4776#	4834#	4836#	4850#	4987#
	4989#	5000#	5242#	5244#	5266#	5716#	5718#	5740#	6268#	6270#	6288#	6796#	6798#
	6820#	7298#	7300#	7321#	7459#	7461#	7485#	8166#	8168#	8193#	8964#	8966#	8981#
	9218#	9220#	9237#	9571#	9573#	9590#	9765#	9767#	9784#	10379#	10381#	10394#	10587#
	10589#	10600#	11312#	11314#	11325#	11747#	11749#	11765#	12601#	12603#	12617#	13160#	13162#
	13176#	13186	13441	13595#	13597#	13614#	13868#	13870#					
JSJMP = 000167	1368#	3184	3345	3368									
LDRDRO 006554 G	2463	2526	2616	2689#	2742	2762	2784	2804	2824	2844	2864	2884	3451

LSLOAD	002100	G	1452#	
LSLUN	002074	G	1448#	
LSMREV	002050	G	1428#	
LSNAME	002000	G	1385#	
LSPRIO	002042	G	1422#	
LSPROT	010060	G	1463	3202#
LSPRT	002112	G	1412#	
LSREPP	002062	G	1458#	
LSREV	002010	G	1394#	
LSRPT	010052	G	3180#	
LSSOFT	036456	G	13949	13950#
LSSPC	002056	G	1434#	
LSSPCP	002020	G	1404#	
LSSPTP	002024	G	1408#	
LSSTA	002030	G	1412#	
LSSW	002270	G	1559	1560#
LSTEST	002114	G	1464#	
LSTIML	002014	G	1400#	
LSUNIT	002012	G	1398#	
L10000	002266		1537	1547#
L10001	002270		1559	1565#
L10002	004766		2149#	
L10003	005002		2158#	
L10004	005016		2167#	
L10005	005032		2176#	
L10006	005046		2185#	
L10007	005070		2197#	
L10010	005112		2209#	
L10011	005134		2221#	
L10012	005156		2233#	
L10013	006736		2729#	
L10014	010056		3185	3191#
L10016	010274		3281	3287#
L10017	010276		3303#	
L10020	010326		3325	3331#
L10021	010334		3346	3352#
L10022	010342		3369	3375#
L10023	010350		3430#	
L10024	010434		3479#	
L10025	010522		3530#	
L10026	010572		3563#	
L10027	010656		3611#	
L10030	010744		3662#	
L10031	011014		3695#	
L10032	011060		3726#	
L10033	011156		3776#	
L10034	011246		3839#	
L10035	011340		3907#	
L10036	011414		3955#	
L10037	011464		4002#	
L10040	011554		4067#	
L10041	011646		4133#	
L10042	011722		4181#	
L10043	011772		4228#	
L10044	012070		4293#	
L10045	012170		4359#	

REG2EQ	004330	G	2082#	2281															
REG4	002304	G	1832#	2644*	2645	2708*	2709	13741											
REG4EQ	004342	G	2084#	2299															
REG6	002306	G	1833#	2491*	2492	2716*	2717	5378*	5850*	7588*	8299*	9375*	9449*	13789*	13798				
REG6EQ	004354	G	2086#	2318															
ROBAD	002326	G	1843#	2268	2412*	2413*	2414	2691*	2692*	2693	2726*	12842	12978						
ROEROR	004754	G	2144#	2420	2450	2469	2532	2622	2748	2768	2790	2810	2830	2850	2870				
			2890	3457	3474	3507	3525	3555	6389	6432	6469	6512	6583	6630	6941				
			6992	7014	7045	7081	7121	7157	7185	7210	7230	7278	12702	12718	12732				
			12754	12795	12809	12833	12848	12882	12910	12932	12942	12969	12984	13002	13012				
			13035	13049	13086	13115	13138	13288	13329	13344	13520	13561	13589						
ROGOOD	002322	G	1841#	2269	2410*	2414	2443*	2689*	2693	6382*	6505*	6623*	6934*	7038*	7114*				
			7150*	7178*	7203*	12788*	12842	12875*	12978	13079*	13097*	13279*	13280*	13336*	13337				
			13513*	13582*															
ROLOAD	002320	G	1840#	2270	2409*	2410	2411	2442*	2461*	2462*	2524*	2525*	2615*	2689	2690				
			2741*	2761*	2783*	2803*	2823*	2843*	2863*	2883*	3450*	3467*	3500*	3518*	3545*				
			3559*	3560	12711*	12925*	12935*	12995*	13005*	13042*	13108*	13281*	13322*	13337*	13554*				
ROMASK	002324	G	1842#	2408*	2413	2614*	2681*	2692											
ROTM	005050	G	2189#	2430															
RO26ER	005034	G	2180#	4924	4969	9392	9462	9562	9670	9693	9712	9747	10116	10135	10209				
			10276	10302	10361	10544	13751	13773	13807										
RO6ERR	005020	G	2171#	2500	2550	2919	2940	2970	2991	3019	3039	3067	3087	3815	3834				
			3880	3901	3947	3995	4041	4061	4107	4127	4173	4221	4267	4287	4333				
			4353	4397	4451	4507	4532	4556	4610	4635	4659	4716	4742	4801	4827				
			4886	4947	5030	5057	5124	5142	5215	5290	5312	5333	5504	5621	5764				
			5786	5809	5984	6161	6308	6327	6846	6864	7340	7372	7509	7531	7552				
			7720	7828	7947	8064	8217	8239	8263	8437	8611	8731	8851	9002	9042				
			9257	9275	9323	9411	9498	9651	9807	9829	9849	10079	10238	10336	10439				
			10459	10481	10502	10522	10576	10620	10641	10659	10711	10799	10832	10931	10967				
			11034	11066	11101	11130	11193	11223	11298	11344	11363	11401	11434	11530	11572				
			11589	11634	11688	11705	11784	12200	12263	12464	12511	12645	13219	13252	13273				
			13390	13410	13431	13667	13686	13706											
R2EROR	004770	G	2153#	2583	2606	3150	3160	3589	3606	3639	3657	3687	3719	4901	5349				
			5825	6346	6374	6498	6568	6681	6722	6753	6892	7259	9298	9478	9634				
			9866	10316	10420	10559	10676	10740	10768	11377	11802	11863	11953	12304	12410				
			12445	12558	12780	12868	13064	13199	13357	13635	13730	13820							
R2LOAD	002330	G	1845#	2288	2574*	2575	2577	2599*	2699	2701	3143*	3153*	3582*	3599*	3632*				
			3650*	3677*	3691*	3692	3709*	3723*	4894*	5342*	5818*	6339*	6367*	6491*	6561*				
			6674*	6715*	6746*	6828*	6885*	7252*	7347*	7562*	8274*	9013*	9291*	9471*	9627*				
			9859*	10309*	10413*	10552*	10669*	10733*	10761*	11370*	11795*	11856*	11946*	12297*	12403*				
			12438*	12551*	12654*	12773*	12861*	13057*	13095*	13192*	13350*	13471*	13628*	13723*	13813*				
R2READ	002332	G	1846#	2287	2576*	2577	2700*	2701											
R2TM	005072	G	2201#	2593															
R4BAD	002340	G	1850#	2305	2645*	2646	270*	2710											
R4EROR	005004	G	2162#	2652	2676	3119	3129	3761	5101	5156	5192	5391	5449	5476	5548				
			5576	5668	5691	5865	5923	5956	6025	6058	6087	6121	6210	6235	6403				
			6447	6483	6526	6552	6606	6645	6667	6708	6739	6781	6906	6956	6979				
			7026	7058	7093	7136	7244	7293	7385	7415	7446	7601	7661	7690	7766				
			7798	7875	7904	7992	8022	8113	8139	8314	8372	8407	8479	8513	8544				
			8581	8659	8690	8778	8810	8902	8930	9078	9107	9133	9159	9185	9204				
			9513	9886	9947	9983	10016	10044	10186	10253	10724	10755	10782	10813	10845				
			10868	10891	10913	10951	10981	11002	11020	11048	11081	11117	11146	11175	11208				
			11243	11260	11285	11416	11448	11486	11503	11513	11557	11617	11665	11733	11848				
			11899	11937	11969	12001	12034	12073	12104	12132	12158	12186	12224	12249	12287				
			12333	12360	12395	12431	12497	12536	12588	13232	13370	13460	13506	13575					
R4GOOD	002336	G	1849#	2306	2643*	2646	2707*	2710	5094*	5149*	5384*	5441*	5442*	5469*	5568*				

SLMODR 007006 G	2759#	4028	4094	4161	4209	4874	5277	5751	6296	6834	7329	7496	8204
	8990	9246	9484	9640	9795	10607	10919	11333	11578	11623	11677	13206	13397
	13692												
SSBRK = 000200 G	1678#	2408	6934	7038	7114	7150	7178	7203					
SVCGBL = 000000	1368#	1385	1386	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403
	1404	1405	1406	1407	1408	1409	1410	1411	1412	1413	1414	1415	1416
	1417	1418	1419	1420	1421	1422	1423	1424	1425	1426	1427	1428	1429
	1431	1432	1434	1435	1436	1437	1438	1439	1440	1441	1442	1443	1444
	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455	1456	1457
	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1480
	1481	1538	1539	1540	1560	1561	1562	1820	1821	1867	1868	1876	1877
	2144	2145	2153	2154	2162	2163	2171	2172	2180	2181	2189	2190	2201
	2202	2213	2214	2225	2226	2725	2726	3180	3181	3202	3203	3218	3219
	3299	3300	3314	3315	3341	3342	3364	3365	13890	13891	13950	13951	13969#
	13970												
SVCINS = 000000	1368#	1386	1387	1388	1389	1390	1391	1392	1393	1394	1395	1396	1397
	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407	1408	1409	1410
	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436
	1437	1438	1439	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449
	1450	1451	1452	1453	1454	1455	1456	1457	1458	1459	1460	1461	1462
	1463	1464	1465	1466	1467	1468	1469	1470	1479	1480	1481	1482	1483
	1484	1485	1486	1487	1488	1489	1490	1491	1492	1493	1494	1495	1496
	1497	1498	1499	1500	1501	1502	1503	1504	1505	1506	1507	1508	1509
	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519	1520	1521	1522
	1523	1524	1525	1526	1537	1538	1559	1560	1868	1870	1871	1877	1881
	1882	2150	2151	2159	2160	2168	2169	2177	2178	2186	2187	2191	2192
	2193	2194	2195	2196	2198	2199	2203	2204	2205	2206	2207	2208	2210
	2211	2215	2216	2217	2218	2219	2220	2222	2223	2227	2228	2229	2230
	2231	2232	2234	2235	2239	2240	2241	2242	2243	2244	2262	2263	2264
	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2281
	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294
	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311
	2312	2313	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328
	2329	2330	2331	2397	2398	2399	2400	2401	2402	2403	2404	2405	2417
	2418	2419	2420	2421	2422	2423	2427	2428	2429	2430	2431	2432	2433
	2434	2436	2437	2441	2442	2447	2448	2449	2450	2451	2453	2454	2460
	2461	2466	2467	2468	2469	2470	2471	2472	2483	2484	2485	2486	2487
	2488	2489	2497	2498	2499	2500	2501	2502	2503	2507	2508	2509	2510
	2511	2512	2513	2514	2516	2517	2523	2524	2529	2530	2531	2532	2533
	2534	2535	2547	2548	2549	2550	2551	2553	2554	2556	2557	2568	2569
	2570	2571	2572	2573	2574	2580	2581	2582	2583	2584	2585	2586	2590
	2591	2592	2593	2594	2595	2596	2597	2598	2599	2603	2604	2605	2606
	2607	2608	2609	2619	2620	2621	2622	2623	2625	2626	2628	2629	2636
	2637	2638	2639	2640	2641	2642	2649	2650	2651	2652	2653	2654	2655
	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2673	2674	2675
	2676	2677	2679	2680	2730	2731	2732	2733	2740	2741	2745	2746	2747
	2748	2749	2751	2752	2760	2761	2765	2766	2767	2768	2769	2771	2772
	2782	2783	2787	2788	2789	2790	2791	2793	2794	2802	2803	2807	2808
	2809	2810	2811	2813	2814	2822	2823	2827	2828	2829	2830	2831	2833
	2834	2842	2843	2847	2848	2849	2850	2851	2853	2854	2862	2863	2867
	2868	2869	2870	2871	2873	2874	2882	2883	2887	2888	2889	2890	2891
	2893	2894	2911	2912	2916	2917	2918	2919	2920	2922	2923	2931	2932
	2937	2938	2939	2940	2941	2943	2944	2962	2963	2967	2968	2969	2970
	2971	2973	2974	2982	2983	2988	2989	2990	2991	2992	2994	2995	3011
	3012	3016	3017	3018	3019	3020	3022	3023	3030	3031	3036	3037	3038

3039	3040	3042	3043	3059	3060	3064	3065	3066	3067	3068	3070	3071
3078	3079	3084	3085	3086	3087	3088	3090	3091	3111	3112	3116	3117
3118	3119	3120	3121	3122	3126	3127	3128	3129	3130	3132	3133	3142
3143	3147	3148	3149	3150	3151	3152	3153	3157	3158	3159	3160	3161
3163	3164	3184	3185	3186	3192	3193	3220	3221	3222	3223	3224	3225
3226	3227	3228	3229	3230	3231	3232	3233	3234	3235	3236	3237	3238
3239	3240	3241	3242	3243	3244	3245	3246	3247	3248	3250	3251	3252
3253	3254	3256	3257	3258	3259	3260	3261	3275	3276	3277	3280	3281
3282	3288	3289	3304	3305	3316	3317	3318	3324	3325	3326	3332	3333
3345	3346	3347	3353	3354	3368	3369	3370	3376	3377	3431	3432	3446
3447	3454	3455	3456	3457	3458	3460	3461	3463	3464	3471	3472	3473
3474	3475	3477	3478	3480	3481	3495	3496	3504	3505	3506	3507	3508
3510	3511	3513	3514	3522	3523	3524	3525	3526	3528	3529	3531	3532
3548	3549	3552	3553	3554	3555	3556	3558	3559	3564	3565	3578	3579
3586	3587	3588	3589	3590	3592	3593	3595	3596	3603	3604	3605	3606
3607	3609	3610	3612	3613	3627	3628	3636	3637	3638	3639	3640	3642
3643	3645	3646	3654	3655	3656	3657	3658	3660	3661	3663	3664	3680
3681	3684	3685	3686	3687	3688	3690	3691	3696	3697	3712	3713	3716
3717	3718	3719	3720	3722	3723	3727	3728	3748	3749	3758	3759	3760
3761	3762	3764	3765	3777	3778	3797	3798	3812	3813	3814	3815	3816
3818	3819	3821	3822	3831	3832	3833	3834	3935	3837	3838	3840	3841
3861	3862	3877	3878	3879	3880	3881	3883	3884	3887	3888	3898	3899
3900	3901	3902	3904	3905	3908	3909	3930	3931	3944	3945	3946	3947
3948	3950	3951	3956	3957	3978	3979	3992	3993	3994	3995	3996	3998
3999	4003	4004	4023	4024	4038	4039	4040	4041	4042	4044	4045	4048
4049	4058	4059	4060	4061	4062	4064	4065	4068	4069	4089	4090	4104
4105	4106	4107	4108	4110	4111	4114	4115	4124	4125	4126	4127	4128
4130	4131	4134	4135	4156	4157	4170	4171	4172	4173	4174	4176	4177
4182	4183	4204	4205	4218	4219	4220	4221	4222	4224	4225	4229	4230
4248	4249	4264	4265	4266	4267	4268	4270	4271	4274	4275	4284	4285
4286	4287	4288	4290	4291	4294	4295	4314	4315	4330	4331	4332	4333
4334	4336	4337	4340	4341	4350	4351	4352	4353	4354	4356	4357	4360
4361	4381	4382	4394	4395	4396	4397	4398	4400	4401	4405	4406	4428
4429	4448	4449	4450	4451	4452	4454	4455	4460	4461	4487	4488	4504
4505	4506	4507	4508	4509	4510	4529	4530	4531	4532	4533	4535	4536
4538	4539	4553	4554	4555	4556	4557	4559	4560	4562	4563	4590	4591
4607	4608	4609	4610	4611	4612	4613	4632	4633	4634	4635	4636	4638
4639	4641	4642	4656	4657	4658	4659	4660	4662	4663	4665	4666	4696
4697	4713	4714	4715	4716	4717	4718	4719	4739	4740	4741	4742	4743
4745	4746	4750	4751	4781	4782	4798	4799	4800	4801	4802	4803	4804
4824	4825	4826	4827	4828	4830	4831	4835	4836	4856	4857	4883	4884
4885	4886	4887	4888	4889	4898	4899	4900	4901	4902	4903	4904	4921
4922	4923	4924	4925	4926	4927	4944	4945	4946	4947	4948	4949	4950
4966	4967	4968	4969	4970	4972	4973	4988	4989	5006	5007	5027	5028
5029	5030	5031	5032	5033	5054	5055	5056	5057	5058	5059	5060	5098
5099	5100	5101	5102	5103	5104	5121	5122	5123	5124	5125	5126	5127
5139	5140	5141	5142	5143	5144	5145	5153	5154	5155	5156	5157	5158
5159	5189	5190	5191	5192	5193	5194	5195	5212	5213	5214	5215	5216
5219	5220	5227	5228	5243	5244	5272	5273	5287	5288	5289	5290	5291
5292	5293	5309	5310	5311	5312	5313	5314	5315	5330	5331	5332	5333
5334	5335	5336	5346	5347	5348	5349	5350	5351	5352	5388	5389	5390
5391	5392	5393	5394	5446	5447	5448	5449	5450	5451	5452	5473	5474
5475	5476	5477	5478	5479	5501	5502	5503	5504	5505	5508	5509	5545
5546	5547	5548	5549	5550	5551	5573	5574	5575	5576	5577	5578	5579
5618	5619	5620	5621	5622	5623	5624	5665	5666	5667	5668	5669	5670
5671	5688	5689	5690	5691	5692	5693	5694	5701	5702	5717	5718	5746

5747	5761	5762	5763	5764	5765	5766	5767	5783	5784	5785	5786	5787
5788	5789	5806	5807	5808	5809	5810	5811	5812	5822	5823	5824	5825
5826	5827	5828	5862	5863	5864	5865	5866	5867	5868	5920	5921	5922
5923	5924	5925	5926	5953	5954	5955	5956	5957	5958	5959	5981	5982
5983	5984	5985	5988	5989	6022	6023	6024	6025	6026	6027	6028	6055
6056	6057	6058	6059	6060	6061	6084	6085	6086	6087	6088	6089	6090
6118	6119	6120	6121	6122	6123	6124	6158	6159	6160	6161	6162	6163
6164	6207	6208	6209	6210	6211	6212	6213	6232	6233	6234	6235	6236
6237	6238	6253	6254	6269	6270	6292	6293	6305	6306	6307	6308	6309
6310	6311	6324	6325	6326	6327	6328	6329	6330	6343	6344	6345	6346
6347	6348	6349	6371	6372	6373	6374	6375	6376	6377	6386	6387	6388
6389	6390	6391	6392	6400	6401	6402	6403	6404	6405	6406	6429	6430
6431	6432	6433	6434	6435	6444	6445	6446	6447	6448	6449	6450	6466
6467	6468	6469	6470	6471	6472	6480	6481	6482	6483	6484	6485	6486
6495	6496	6497	6498	6499	6500	6501	6509	6510	6511	6512	6513	6514
6515	6523	6524	6525	6526	6527	6528	6529	6549	6550	6551	6552	6553
6554	6555	6565	6566	6567	6568	6569	6570	6571	6580	6581	6582	6583
6584	6585	6586	6603	6604	6605	6606	6607	6608	6609	6627	6628	6629
6630	6631	6632	6633	6642	6643	6644	6645	6646	6647	6648	6664	6665
6666	6667	6668	6669	6670	6678	6679	6680	6681	6682	6683	6684	6705
6706	6707	6708	6709	6710	6711	6719	6720	6721	6722	6723	6724	6725
6736	6737	6738	6739	6740	6741	6742	6750	6751	6752	6753	6754	6755
6756	6778	6779	6780	6781	6782	6783	6784	6794	6795	6797	6798	6823
6824	6843	6844	6845	6846	6847	6848	6849	6861	6862	6863	6864	6865
6866	6867	6889	6890	6891	6892	6893	6894	6895	6903	6904	6905	6906
6907	6908	6909	6938	6939	6940	6941	6942	6943	6944	6953	6954	6955
6956	6957	6958	6959	6976	6977	6978	6979	6980	6981	6982	6989	6990
6991	6992	6993	6994	6995	7011	7012	7013	7014	7015	7016	7017	7023
7024	7025	7026	7027	7028	7029	7042	7043	7044	7045	7046	7047	7048
7055	7056	7057	7058	7059	7060	7061	7078	7079	7080	7081	7082	7083
7084	7090	7091	7092	7093	7094	7095	7096	7118	7119	7120	7121	7122
7123	7124	7133	7134	7135	7136	7137	7138	7139	7154	7155	7156	7157
7158	7159	7160	7182	7183	7184	7185	7186	7187	7188	7207	7208	7209
7210	7211	7212	7213	7227	7228	7229	7230	7231	7232	7233	7241	7242
7243	7244	7245	7246	7247	7256	7257	7258	7259	7260	7261	7262	7275
7276	7277	7278	7279	7280	7281	7290	7291	7292	7293	7294	7296	7297
7299	7300	7325	7326	7337	7338	7339	7340	7341	7342	7343	7369	7370
7371	7372	7373	7374	7375	7382	7383	7384	7385	7386	7387	7388	7412
7413	7414	7415	7416	7417	7418	7443	7444	7445	7446	7447	7448	7449
7457	7458	7460	7461	7491	7492	7506	7507	7508	7509	7510	7511	7512
7528	7529	7530	7531	7532	7533	7534	7549	7550	7551	7552	7553	7554
7555	7598	7599	7600	7601	7602	7603	7604	7658	7659	7660	7661	7662
7663	7664	7687	7688	7689	7690	7691	7692	7693	7717	7718	7719	7720
7721	7722	7723	7763	7764	7765	7766	7767	7768	7769	7795	7796	7797
7798	7799	7800	7801	7825	7826	7827	7828	7829	7830	7831	7872	7873
7874	7875	7876	7877	7878	7901	7902	7903	7904	7905	7906	7907	7944
7945	7946	7947	7948	7949	7950	7989	7990	7991	7992	7993	7994	7995
8019	8020	8021	8022	8023	8024	8025	8061	8062	8063	8064	8065	8066
8067	8110	8111	8112	8113	8114	8115	8116	8136	8137	8138	8139	8140
8141	8142	8150	8151	8167	8168	8199	8200	8214	8215	8216	8217	8218
8219	8220	8236	8237	8238	8239	8240	8241	8242	8260	8261	8262	8263
8264	8265	8266	8311	8312	8313	8314	8315	8316	8317	8369	8370	8371
8372	8373	8374	8375	8404	8405	8406	8407	8408	8409	8410	8434	8435
8436	8437	8438	8439	8440	8476	8477	8478	8479	8480	8481	8482	8510
8511	8512	8513	8514	8515	8516	8541	8542	8543	8544	8545	8546	8547
8578	8579	8580	8581	8582	8583	8584	8608	8609	8610	8611	8612	8613

8614	8656	8657	8658	8659	8660	8661	8662	8687	8688	8689	8690	8691
8692	8693	8728	8729	8730	8731	8732	8733	8734	8775	8776	8777	8778
8779	8780	8781	8807	8808	8809	8810	8811	8812	8813	8848	8849	8850
8851	8852	8853	8854	8899	8900	8901	8902	8903	8904	8905	8927	8928
8929	8930	8931	8932	8933	8947	8948	8965	8966	8985	8986	8999	9000
9001	9002	9003	9004	9005	9039	9040	9041	9042	9043	9044	9045	9075
9076	9077	9078	9079	9080	9081	9104	9105	9106	9107	9108	9109	9110
9130	9131	9132	9133	9134	9135	9136	9156	9157	9158	9159	9160	9161
9162	9182	9183	9184	9185	9186	9187	9188	9201	9202	9203	9204	9205
9206	9207	9216	9217	9219	9220	9242	9243	9254	9255	9256	9257	9258
9259	9260	9272	9273	9274	9275	9276	9277	9278	9295	9296	9297	9298
9299	9300	9301	9320	9321	9322	9323	9324	9325	9326	9389	9390	9391
9392	9393	9394	9395	9408	9409	9410	9411	9412	9413	9414	9459	9460
9461	9462	9463	9464	9465	9475	9476	9477	9478	9479	9480	9481	9495
9496	9497	9498	9499	9500	9501	9510	9511	9512	9513	9514	9515	9516
9559	9560	9561	9562	9563	9565	9566	9572	9573	9596	9597	9631	9632
9633	9634	9635	9636	9637	9648	9649	9650	9651	9652	9653	9654	9667
9668	9669	9670	9671	9672	9673	9690	9691	9692	9693	9694	9695	9696
9709	9710	9711	9712	9713	9714	9715	9744	9745	9746	9747	9748	9750
9751	9766	9767	9790	9791	9804	9805	9806	9807	9808	9809	9810	9826
9827	9828	9829	9830	9831	9832	9846	9847	9848	9849	9850	9851	9852
9863	9864	9865	9866	9867	9868	9869	9883	9884	9885	9886	9887	9888
9889	9944	9945	9946	9947	9948	9949	9950	9980	9981	9982	9983	9984
9985	9986	10013	10014	10015	10016	10017	10018	10019	10041	10042	10043	10044
10045	10046	10047	10076	10077	10078	10079	10080	10081	10082	10113	10114	10115
10116	10117	10118	10119	10132	10133	10134	10135	10136	10137	10138	10183	10184
10185	10186	10187	10188	10189	10206	10207	10208	10209	10210	10211	10212	10235
10236	10237	10238	10239	10240	10241	10250	10251	10252	10253	10254	10255	10256
10273	10274	10275	10276	10277	10278	10279	10299	10300	10301	10302	10303	10304
10305	10313	10314	10315	10316	10317	10318	10319	10333	10334	10335	10336	10337
10338	10339	10358	10359	10360	10361	10362	10364	10365	10380	10381	10399	10400
10417	10418	10419	10420	10421	10422	10423	10436	10437	10438	10439	10440	10441
10442	10456	10457	10458	10459	10460	10461	10462	10478	10479	10480	10481	10482
10483	10484	10499	10500	10501	10502	10503	10504	10505	10519	10520	10521	10522
10523	10524	10525	10541	10542	10543	10544	10545	10546	10547	10556	10557	10558
10559	10560	10561	10562	10573	10574	10575	10576	10577	10579	10580	10588	10589
10603	10604	10617	10618	10619	10620	10621	10622	10623	10638	10639	10640	10641
10642	10643	10644	10656	10657	10658	10659	10660	10661	10662	10673	10674	10675
10676	10677	10678	10679	10708	10709	10710	10711	10712	10713	10714	10721	10722
10723	10724	10725	10726	10727	10737	10738	10739	10740	10741	10742	10743	10752
10753	10754	10755	10756	10757	10758	10765	10766	10767	10768	10769	10770	10771
10779	10780	10781	10782	10783	10784	10785	10796	10797	10798	10799	10800	10801
10802	10810	10811	10812	10813	10814	10815	10816	10829	10830	10831	10832	10833
10834	10835	10842	10843	10844	10845	10846	10847	10848	10865	10866	10867	10868
10869	10870	10871	10888	10889	10890	10891	10892	10893	10894	10910	10911	10912
10913	10914	10915	10916	10928	10929	10930	10931	10932	10933	10934	10948	10949
10950	10951	10952	10953	10954	10964	10965	10966	10967	10968	10969	10970	10978
10979	10980	10981	10982	10983	10984	10999	11000	11001	11002	11003	11004	11005
11017	11018	11019	11020	11021	11022	11023	11031	11032	11033	11034	11035	11036
11037	11045	11046	11047	11048	11049	11050	11051	11063	11064	11065	11066	11067
11068	11069	11078	11079	11080	11081	11082	11083	11084	11098	11099	11100	11101
11102	11103	11104	11114	11115	11116	11117	11118	11119	11120	11127	11128	11129
11130	11131	11132	11133	11143	11144	11145	11146	11147	11148	11149	11172	11173
11174	11175	11176	11177	11178	11190	11191	11192	11193	11194	11195	11196	11205
11206	11207	11208	11209	11210	11211	11220	11221	11222	11223	11224	11225	11226
11240	11241	11242	11243	11244	11245	11246	11257	11258	11259	11260	11261	11262

11263	11282	11283	11284	11285	11286	11287	11288	11295	11296	11297	11298	11299
11300	11301	11310	11311	11313	11314	11329	11330	11341	11342	11343	11344	11345
11346	11347	11360	11361	11362	11363	11364	11365	11366	11374	11375	11376	11377
11378	11379	11380	11398	11399	11400	11401	11402	11403	11404	11413	11414	11415
11416	11417	11418	11419	11431	11432	11433	11434	11435	11436	11437	11445	11446
11447	11448	11449	11450	11451	11483	11484	11485	11486	11487	11488	11489	11500
11501	11502	11503	11504	11505	11506	11510	11511	11512	11513	11514	11515	11516
11527	11528	11529	11530	11531	11532	11533	11554	11555	11556	11557	11558	11559
11560	11569	11570	11571	11572	11573	11574	11575	11586	11587	11588	11589	11590
11591	11592	11614	11615	11616	11617	11618	11619	11620	11631	11632	11633	11634
11635	11636	11637	11662	11663	11664	11665	11666	11667	11668	11685	11686	11687
11688	11689	11690	11691	11702	11703	11704	11705	11706	11707	11708	11730	11731
11732	11733	11734	11735	11736	11745	11746	11748	11749	11768	11769	11781	11782
11783	11784	11785	11786	11787	11799	11800	11801	11802	11803	11804	11805	11845
11846	11847	11848	11849	11850	11851	11860	11861	11862	11863	11864	11865	11866
11896	11897	11898	11899	11900	11901	11902	11934	11935	11936	11937	11938	11939
11940	11950	11951	11952	11953	11954	11955	11956	11966	11967	11968	11969	11970
11971	11972	11998	11999	12000	12001	12002	12003	12004	12031	12032	12033	12034
12035	12036	12037	12070	12071	12072	12073	12074	12075	12076	12101	12102	12103
12104	12105	12106	12107	12129	12130	12131	12132	12133	12134	12135	12155	12156
12157	12158	12159	12160	12161	12183	12184	12185	12186	12187	12188	12189	12197
12198	12199	12200	12201	12202	12203	12221	12222	12223	12224	12225	12226	12227
12246	12247	12248	12249	12250	12251	12252	12260	12261	12262	12263	12264	12265
12266	12284	12285	12286	12287	12288	12289	12290	12301	12302	12303	12304	12305
12306	12307	12330	12331	12332	12333	12334	12335	12336	12357	12358	12359	12360
12361	12362	12363	12392	12393	12394	12395	12396	12397	12398	12407	12408	12409
12410	12411	12412	12413	12428	12429	12430	12431	12432	12433	12434	12442	12443
12444	12445	12446	12447	12448	12461	12462	12463	12464	12465	12466	12467	12494
12495	12496	12497	12498	12499	12500	12508	12509	12510	12511	12512	12513	12514
12533	12534	12535	12536	12537	12538	12539	12555	12556	12557	12558	12559	12560
12561	12585	12586	12587	12588	12589	12590	12591	12599	12600	12602	12603	12621
12622	12627	12628	12629	12642	12643	12644	12645	12646	12647	12648	12672	12673
12674	12675	12676	12677	12678	12685	12686	12687	12699	12700	12701	12702	12703
12705	12706	12715	12716	12717	12718	12719	12720	12721	12729	12730	12731	12732
12733	12735	12736	12751	12752	12753	12754	12755	12757	12758	12763	12764	12765
12777	12778	12779	12780	12781	12782	12783	12792	12793	12794	12795	12796	12797
12798	12806	12807	12808	12809	12810	12812	12813	12819	12820	12821	12830	12831
12832	12833	12834	12835	12836	12845	12846	12847	12848	12849	12850	12851	12865
12866	12867	12868	12869	12870	12871	12879	12880	12881	12882	12883	12884	12885
12894	12895	12896	12907	12908	12909	12910	12911	12913	12914	12918	12919	12920
12929	12930	12931	12932	12933	12934	12935	12939	12940	12941	12942	12943	12944
12945	12955	12956	12957	12966	12967	12968	12969	12970	12971	12972	12981	12982
12983	12984	12985	12986	12987	12999	13000	13001	13002	13003	13004	13005	13009
13010	13011	13012	13013	13014	13015	13021	13022	13023	13032	13033	13034	13035
13036	13038	13039	13046	13047	13048	13049	13050	13051	13052	13061	13062	13063
13064	13065	13066	13067	13083	13084	13085	13086	13087	13089	13090	13102	13103
13104	13112	13113	13114	13115	13116	13117	13118	13124	13125	13126	13135	13136
13137	13138	13139	13141	13142	13146	13147	13148	13153	13154	13155	13158	13159
13161	13162	13187	13188	13196	13197	13198	13199	13200	13201	13202	13216	13217
13218	13219	13220	13221	13222	13229	13230	13231	13232	13233	13234	13235	13249
13250	13251	13252	13253	13254	13255	13270	13271	13272	13273	13274	13275	13276
13285	13286	13287	13288	13289	13290	13291	13295	13296	13297	13298	13299	13300
13301	13302	13303	13307	13308	13309	13320	13321	13322	13326	13327	13328	13329
13330	13331	13332	13341	13342	13343	13344	13345	13346	13347	13354	13355	13356
13357	13358	13359	13360	13367	13368	13369	13370	13371	13372	13373	13387	13388
13389	13390	13391	13392	13393	13407	13408	13409	13410	13411	13412	13413	13428

13429	13430	13431	13432	13434	13435	13442	13443	13457	13458	13459	13460	13461
13462	13463	13503	13504	13505	13506	13507	13508	13509	13517	13518	13519	13520
13521	13522	13523	13527	13528	13529	13530	13531	13532	13533	13534	13535	13539
13540	13541	13552	13553	13554	13558	13559	13560	13561	13562	13563	13564	13572
13573	13574	13575	13576	13577	13578	13586	13587	13588	13589	13590	13592	13593
13596	13597	13623	13624	13632	13633	13634	13635	13636	13637	13638	13664	13665
13666	13667	13668	13669	13670	13683	13684	13685	13686	13687	13688	13689	13703
13704	13705	13706	13707	13708	13709	13727	13728	13729	13730	13731	13732	13733
13748	13749	13750	13751	13752	13753	13754	13770	13771	13772	13773	13774	13775
13776	13804	13805	13806	13807	13808	13809	13810	13817	13818	13819	13820	13821
13823	13824	13869	13870	13889	13890	13901	13902	13903	13904	13905	13906	13907
13908	13909	13910	13911	13912	13913	13914	13915	13916	13920	13921	13949	13950
13956	13957	13966	13967	13968	13969	13976	13977	13978				
1368#	13186	13187	13441	13442								
1368#	1547	1548	1565	1566	2149	2150	2158	2159	2167	2168	2176	2177
2185	2186	2197	2198	2209	2210	2221	2222	2233	2234	2435	2436	2452
2453	2515	2516	2552	2553	2624	2625	2678	2679	2729	2730	2750	2751
2770	2771	2792	2793	2812	2813	2832	2833	2852	2853	2872	2873	2892
2893	2921	2922	2942	2943	2972	2973	2993	2994	3021	3022	3041	3042
3069	3070	3089	3090	3131	3132	3162	3163	3191	3192	3287	3288	3303
3304	3331	3332	3352	3353	3375	3376	3430	3431	3459	3460	3476	3477
3479	3480	3509	3510	3527	3528	3530	3531	3557	3558	3563	3564	3591
3592	3608	3609	3611	3612	3641	3642	3659	3660	3662	3663	3689	3690
3695	3696	3721	3722	3726	3727	3763	3764	3776	3777	3817	3818	3836
3837	3839	3840	3882	3883	3903	3904	3907	3908	3949	3950	3955	3956
3997	3998	4002	4003	4043	4044	4063	4064	4067	4068	4109	4110	4129
4130	4133	4134	4175	4176	4181	4182	4223	4224	4228	4229	4269	4270
4289	4290	4293	4294	4335	4336	4355	4356	4359	4360	4399	4400	4404
4405	4453	4454	4459	4460	4534	4535	4558	4559	4561	4562	4637	4638
4661	4662	4664	4665	4744	4745	4749	4750	4829	4830	4834	4835	4971
4972	4987	4988	5226	5227	5242	5243	5243	5700	5701	5716	5717	6252
6268	6269	6793	6794	6796	6797	7295	7296	7298	7299	7456	7457	7459
7460	8149	8150	8166	8167	8946	8947	8964	8965	9215	9216	9218	9219
9564	9565	9571	9572	9749	9750	9765	9766	10363	10364	10379	10380	10578
10579	10587	10588	11309	11310	11312	11313	11744	11745	11747	11748	12598	12599
12601	12602	13157	13158	13160	13161	13433	13434	13591	13592	13595	13596	13822
13823	13868	13869	13921	13922	13957	13958	13978	13979	13983	13984		
1368#	3423	3424	3442	3443	3491	3492	3542	3543	3574	3575	3623	3624
3674	3675	3706	3707	3742	3743	3793	3794	3857	3858	3924	3925	3972
3973	4019	4020	4085	4086	4150	4151	4198	4199	4244	4245	4310	4311
4375	4376	4423	4424	4483	4484	4586	4587	4691	4692	4776	4777	4850
4851	5000	5001	5266	5267	5740	5741	6288	6289	6820	6821	7321	7322
7485	7486	8193	8194	8981	8982	9237	9238	9590	9591	9784	9785	10394
10395	10600	10601	11325	11326	11765	11766	12617	12618	13176	13177	13614	13615
1368#	1548#	1566#	2150#	2159#	2168#	2177#	2186#	2198#	2210#	2222#	2234#	2397#
2441#	2460#	2523#	2556#	2628#	2730#	2740#	2760#	2782#	2802#	2822#	2842#	2862#
2882#	2911#	2931#	2962#	2982#	3011#	3030#	3059#	3078#	3111#	3142#	3192#	3288#
3304#	3332#	3353#	3376#	3431#	3446#	3463#	3480#	3495#	3513#	3531#	3548#	3564#
3578#	3595#	3612#	3627#	3645#	3663#	3680#	3696#	3712#	3727#	3748#	3777#	3797#
3821#	3840#	3861#	3887#	3908#	3930#	3956#	3978#	4003#	4023#	4048#	4068#	4089#
4114#	4134#	4156#	4182#	4204#	4229#	4248#	4274#	4294#	4314#	4340#	4360#	4381#
4405#	4428#	4460#	4487#	4538#	4562#	4590#	4641#	4665#	4696#	4750#	4781#	4835#
4856#	4988#	5006#	5243#	5272#	5717#	5746#	6269#	6292#	6797#	6823#	7299#	7325#
7460#	7491#	8167#	8199#	8965#	8985#	9219#	9242#	9572#	9596#	9766#	9790#	10380#
10399#	10588#	10603#	11313#	11329#	11748#	11768#	12602#	12621#	13161#	13434#	13592#	13596#
13623#	13869#	13922#	13958#									

SVCSUB= 000000
SVCTAG= 000000

SVCTST= 000000

SSLSYM= 010000

TDLEOD 003607 G
TEVECT 002312 G
TOBRK = 000100 G
TSARGC= 000003

TSCODE= 002032
TSERRN= 000002

TSEXCP= 000000
TSFLAG= 000050
TSFREE= 036554
TSGMAN= 000000
TSHILI= 000017
TSLAST= 000001
TSLOLI= 000000
TSLSYM= 010000

TSLTNO= 000055
TSNEST= 177777

2018#	10301													
1836#	3270*	12674	13153											
1679#	2408	6382	6505	6617	6623	12788	12875	13079	13097					
1386#	1387#	1388#	1389#	1390#	1391#	2191#	2195	2203#	2207	2215#	2219	2227#		
2231	2239#	2243	2262#	2266	2268#	2275	2281#	2285	2287#	2293	2299#	2303		
2305#	2312	2318#	2322	2324#	2330									
13901#	13906#	13911#												
1368#	2418#	2428#	2448#	2467#	2498#	2508#	2530#	2548#	2581#	2591#	2604#	2620#		
2650#	2661#	2674#	2746#	2766#	2788#	2808#	2828#	2848#	2868#	2888#	2917#	2938#		
2968#	2989#	3017#	3037#	3065#	3085#	3117#	3127#	3148#	3158#	3455#	3472#	3505#		
3523#	3553#	3587#	3604#	3637#	3655#	3685#	3717#	3759#	3813#	3832#	3878#	3899#		
3945#	3993#	4039#	4059#	4105#	4125#	4171#	4219#	4265#	4285#	4331#	4351#	4395#		
4449#	4505#	4530#	4554#	4608#	4633#	4657#	4714#	4740#	4799#	4825#	4884#	4899#		
4922#	4945#	4967#	5028#	5055#	5099#	5122#	5140#	5154#	5190#	5213#	5288#	5310#		
5331#	5347#	5389#	5447#	5474#	5502#	5546#	5574#	5619#	5666#	5689#	5762#	5784#		
5807#	5823#	5863#	5921#	5954#	5982#	6023#	6056#	6085#	6119#	6159#	6208#	6233#		
6306#	6325#	6344#	6372#	6387#	6401#	6430#	6445#	6467#	6481#	6496#	6510#	6524#		
6550#	6566#	6581#	6604#	6628#	6643#	6665#	6679#	6706#	6720#	6737#	6751#	6779#		
6844#	6862#	6890#	6904#	6939#	6954#	6977#	6990#	7012#	7024#	7045#	7056#	7079#		
7091#	7119#	7134#	7155#	7183#	7208#	7228#	7242#	7257#	7276#	7291#	7338#	7370#		
7383#	7413#	7444#	7507#	7529#	7550#	7599#	7659#	7688#	7718#	7764#	7796#	7826#		
7873#	7902#	7945#	7990#	8020#	8062#	8111#	8137#	8215#	8237#	8261#	8312#	8370#		
8405#	8435#	8477#	8511#	8542#	8579#	8609#	8657#	8688#	8729#	8776#	8808#	8849#		
8900#	8928#	9000#	9040#	9076#	9105#	9131#	9157#	9183#	9202#	9255#	9273#	9296#		
9321#	9390#	9409#	9460#	9476#	9496#	9511#	9560#	9632#	9649#	9668#	9691#	9710#		
9745#	9805#	9827#	9847#	9864#	9884#	9945#	9981#	10014#	10042#	10077#	10114#	10133#		
10184#	10207#	10236#	10251#	10274#	10300#	10314#	10334#	10359#	10418#	10437#	10457#	10479#		
10500#	10520#	10542#	10557#	10574#	10618#	10639#	10657#	10674#	10709#	10722#	10738#	10753#		
10766#	10780#	10797#	10811#	10830#	10843#	10866#	10889#	10911#	10929#	10949#	10965#	10979#		
11000#	11018#	11032#	11046#	11064#	11079#	11099#	11115#	11128#	11144#	11173#	11191#	11206#		
11221#	11241#	11258#	11283#	11296#	11342#	11361#	11375#	11399#	11414#	11432#	11446#	11484#		
11501#	11511#	11528#	11555#	11570#	11587#	11615#	11632#	11663#	11686#	11703#	11731#	11782#		
11800#	11846#	11861#	11897#	11935#	11951#	11967#	11999#	12032#	12071#	12102#	12130#	12156#		
12184#	12198#	12222#	12247#	12261#	12285#	12302#	12331#	12358#	12393#	12408#	12429#	12443#		
12462#	12495#	12509#	12534#	12556#	12586#	12643#	12700#	12716#	12730#	12752#	12778#	12793#		
12807#	12831#	12846#	12866#	12880#	12908#	12930#	12940#	12967#	12982#	13000#	13010#	13033#		
13047#	13062#	13084#	13113#	13136#	13197#	13217#	13230#	13250#	13271#	13286#	13327#	13342#		
13355#	13368#	13388#	13408#	13429#	13458#	13504#	13518#	13559#	13573#	13587#	13633#	13665#		
13684#	13704#	13728#	13749#	13771#	13805#	13818#								
13901#	13905	13906#	13910	13911#	13916									
3184#	3186	3280#	3324#	3345#	3347	3368#	3370							
13967	13985#													
1368#														
13901#	13904	13906#	13909	13911#	13915									
1368#	13967#	13975												
13901#	13903	13906#	13908	13911#	13914									
1368#	1548	1566	2150	2159	2168	2177	2186	2198	2210	2222	2234	2730		
3192	3288	3304	3332	3353	3376	3431	3480	3531	3564	3612	3663	3696		
3727	3777	3840	3908	3956	4003	4068	4134	4182	4229	4294	4360	4405		
4460	4562	4665	4750	4835	4988	5243	5717	6269	6797	7299	7460	8167		
8965	9219	9572	9766	10380	10588	11313	11748	12602	13161	13434	13592	13596		
13869	13922	13958												
13970#														
1368#	1375#	1537#	1547#	1559#	1565#	1568#	1573#	2144#	2149#	2153#	2158#	2162#		
2167#	2171#	2176#	2180#	2185#	2189#	2197#	2201#	2209#	2213#	2221#	2225#	2233#		
2397#	2435#	2441#	2452#	2460#	2515#	2523#	2552#	2556#	2624#	2628#	2678#	2725#		

2729#	2740#	2750#	2760#	2770#	2782#	2792#	2802#	2812#	2822#	2832#	2842#	2852#
2862#	2872#	2882#	2892#	2911#	2921#	2931#	2942#	2962#	2972#	2982#	2993#	3011#
3021#	3030#	3041#	3059#	3069#	3078#	3089#	3111#	3131#	3142#	3162#	3168#	3173#
3180#	3191#	3202#	3209#	3218#	3287#	3299#	3303#	3314#	3331#	3341#	3352#	3364#
3375#	3379#	3385#	3424#	3430#	3443#	3446#	3459#	3463#	3476#	3479#	3492#	3495#
3509#	3513#	3527#	3530#	3543#	3548#	3557#	3563#	3575#	3578#	3591#	3595#	3608#
3611#	3624#	3627#	3641#	3645#	3659#	3662#	3675#	3680#	3689#	3695#	3707#	3712#
3721#	3726#	3743#	3748#	3763#	3776#	3794#	3797#	3817#	3821#	3836#	3839#	3858#
3861#	3882#	3887#	3903#	3907#	3925#	3930#	3949#	3955#	3973#	3978#	3997#	4002#
4020#	4023#	4043#	4048#	4063#	4067#	4086#	4089#	4109#	4114#	4129#	4133#	4151#
4156#	4175#	4181#	4199#	4204#	4223#	4228#	4245#	4248#	4269#	4274#	4289#	4293#
4311#	4314#	4335#	4340#	4355#	4359#	4376#	4381#	4399#	4404#	4424#	4428#	4453#
4459#	4484#	4487#	4534#	4538#	4558#	4561#	4587#	4590#	4637#	4641#	4661#	4664#
4692#	4696#	4744#	4749#	4777#	4781#	4829#	4834#	4851#	4856#	4971#	4987#	5001#
5006#	5226#	5242#	5267#	5272#	5700#	5716#	5741#	5746#	6252#	6268#	6289#	6292#
6793#	6796#	6821#	6823#	7295#	7298#	7322#	7325#	7456#	7459#	7486#	7491#	8149#
8166#	8194#	8199#	8946#	8964#	8982#	8985#	9215#	9218#	9238#	9242#	9564#	9571#
9591#	9596#	9749#	9765#	9785#	9790#	10363#	10379#	10395#	10399#	10578#	10587#	10001#
10603#	11309#	11312#	11326#	11329#	11744#	11747#	11766#	11768#	12598#	12601#	12618#	12621#
13157#	13160#	13177#	13187#	13433#	13442#	13591#	13595#	13615#	13623#	13822#	13868#	13872#
13878#	13889#	13920#	13949#	13956#	13971#							
1375#	1568	1573#	3168	3173#	3379	3385#	13872	13878#	13971			
1537#	1547	1559#	1565	2144#	2149	2153#	2158	2162#	2167	2171#	2176	2180#
2185	2189#	2197	2201#	2209	2213#	2221	2225#	2233	2397#	2435	2441#	2452
2460#	2515	2523#	2552	2556#	2624	2628#	2678	2725#	2729	2740#	2750	2760#
2770	2782#	2792	2802#	2812	2822#	2832	2842#	2852	2862#	2872	2882#	2892
2911#	2921	2931#	2942	2962#	2972	2982#	2993	3011#	3021	3030#	3041	3059#
3069	3078#	3089	3111#	3131	3142#	3162	3180#	3191	3202#	3209	3218#	3287
3299#	3303	3314#	3331	3341#	3352	3364#	3375	3424#	3430	3443#	3479	3492#
3530	3543#	3563	3575#	3611	3624#	3662	3675#	3695	3707#	3726	3743#	3776
3794#	3839	3858#	3907	3925#	3955	3973#	4002	4020#	4067	4080#	4133	4151#
4181	4199#	4228	4245#	4293	4311#	4359	4376#	4404	4424#	4459	4484#	4561
4587#	4664	4692#	4749	4777#	4834	4851#	4987	5001#	5242	5267#	5716	5741#
6268	6289#	6796	6821#	7298	7322#	7459	7486#	8166	8194#	8964	8982#	9218
9238#	9571	9591#	9765	9785#	10379	10395#	10587	10601#	11312	11326#	11747	11766#
12601	12618#	13160	13177#	13595	13615#	13868	13889#	13920	13949#	13956		
3446#	3459	3463#	3476	3495#	3509	3513#	3527	3548#	3557	3578#	3591	3595#
3608	3627#	3641	3645#	3659	3680#	3689	3712#	3721	3748#	3763	3797#	3817
3821#	3836	3861#	3882	3887#	3903	3930#	3949	3978#	3997	4023#	4043	4048#
4063	4089#	4109	4114#	4129	4156#	4175	4204#	4223	4248#	4269	4274#	4289
4314#	4335	4340#	4355	4381#	4399	4428#	4453	4487#	4534	4538#	4558	4590#
4637	4641#	4661	4696#	4744	4781#	4829	4856#	4971	5006#	5226	5272#	5700
5746#	6252	6292#	6793	6823#	7295	7325#	7456	7491#	8149	8199#	8946	8985#
9215	9242#	9564	9596#	9749	9790#	10363	10399#	10578	10603#	11309	11329#	11744
11768#	12598	12621#	13157	13187#	13433	13442#	13591	13623#	13822			
13975#	13976#											
13976#	13979											
1399	13985#											
1368#	13979#	13985										
1368#												
1368#	2397#	2435#	2437	2441#	2452#	2454	2460#	2515#	2517	2523#	2552#	2554
2556#	2624#	2626	2628#	2678#	2680	2740#	2750#	2752	2760#	2770#	2772	2782#
2792#	2794	2802#	2812#	2814	2822#	2832#	2834	2842#	2852#	2854	2862#	2872#
2874	2882#	2892#	2894	2911#	2921#	2923	2931#	2942#	2944	2962#	2972#	2974
2982#	2993#	2995	3011#	3021#	3023	3030#	3041#	3043	3059#	3069#	3071	3078#
3089#	3091	3111#	3131#	3133	3142#	3162#	3164	3446#	3459#	3461	3463#	3476#

T\$NSO = 000000
T\$NS1 = 000005

T\$NS2 = 000003

T\$PCNT= 000000
T\$PTAB= 010105
T\$PTHV= 000001
T\$PTMU= 000001
T\$SAVL= 177777
T\$SEGL= 177777

T\$SEKO= 010000

T\$SIZE= 000005
T\$SUBN= 000000

T\$TAGL= 177777
T\$TAGN= 010107

T\$TEMP= 000000

T\$TEST= 000055

3478	3495#	3509#	3511	3513#	3527#	3529	3548#	3557#	3559	3578#	3591#	3593
3595#	3608#	3610	3627#	3641#	3643	3645#	3659#	3661	3680#	3689#	3691	3712#
3721#	3723	3748#	3763#	3765	3797#	3817#	3819	3821#	3836#	3838	3861#	3882#
3884	3887#	3903#	3905	3930#	3949#	3951	3978#	3997#	3999	4023#	4043#	4045
4048#	4063#	4065	4089#	4109#	4111	4114#	4129#	4131	4156#	4175#	4177	4204#
4223#	4225	4248#	4269#	4271	4274#	4289#	4291	4314#	4335#	4337	4340#	4355#
4357	4381#	4399#	4401	4428#	4453#	4455	4487#	4534#	4536	4538#	4558#	4560
4590#	4637#	4639	4641#	4661#	4663	4696#	4744#	4746	4781#	4829#	4831	4856#
4971#	4973	5006#	5226#	5228	5272#	5700#	5702	5746#	6252#	6254	6292#	6793#
6795	6823#	7295#	7297	7325#	7456#	7458	7491#	8149#	8151	8199#	8946#	8948
8985#	9215#	9217	9242#	9564#	9566	9596#	9749#	9751	9790#	10363#	10365	10399#
10578#	10580	10603#	11309#	11311	11329#	11744#	11746	11768#	12598#	12600	12621#	13157#
13159	13623#	13822#	13824									
2397#	2435	2441#	2452	2460#	2515	2523#	2552	2556#	2624	2628#	2678	2740#
2750	2760#	2770	2782#	2792	2802#	2812	2822#	2832	2842#	2852	2862#	2872
2882#	2892	2911#	2921	2931#	2942	2962#	2972	2982#	2993	3011#	3021	3030#
3041	3059#	3069	3078#	3089	3111#	3131	3142#	3162	3446#	3459	3463#	3476
3495#	3509	3513#	3527	3548#	3557	3578#	3591	3595#	3608	3627#	3641	3645#
3659	3680#	3689	3712#	3721	3748#	3763	3797#	3817	3821#	3836	3861#	3882
3887#	3903	3930#	3949	3978#	3997	4023#	4043	4048#	4063	4089#	4109	4114#
4129	4156#	4175	4204#	4223	4248#	4269	4274#	4289	4314#	4335	4340#	4355
4381#	4399	4428#	4453	4487#	4534	4538#	4558	4590#	4637	4641#	4661	4696#
4744	4781#	4829	4856#	4971	5006#	5226	5272#	5700	5746#	6252	6292#	6793
6823#	7295	7325#	7456	7491#	8149	8199#	8946	8985#	9215	9242#	9564	9596#
9749	9790#	10363	10399#	10578	10603#	11309	11329#	11744	11768#	12598	12621#	13157
13623#	13822											
13968	13985#											
1368#	3423#	3442#	3491#	3542#	3574#	3623#	3674#	3706#	3742#	3793#	3857#	3924#
3972#	4019#	4085#	4150#	4198#	4244#	4310#	4375#	4423#	4483#	4586#	4691#	4776#
4850#	5000#	5266#	5740#	6288#	6820#	7321#	7485#	8193#	8981#	9237#	9590#	9784#
10394#	10600#	11325#	11765#	12617#	13176#	13186#	13441#	13614#				
1368#												
1368#	1537#	1559#	2144#	2153#	2162#	2171#	2180#	2189#	2201#	2213#	2225#	2725#
3180#	3202#	3218#	3299#	3314#	3341#	3364#	3424#	3443#	3492#	3543#	3575#	3624#
3675#	3707#	3743#	3794#	3858#	3925#	3973#	4020#	4086#	4151#	4199#	4245#	4311#
4376#	4424#	4484#	4587#	4692#	4777#	4951#	5001#	5267#	5741#	6289#	6821#	7322#
7486#	8194#	8982#	9238#	9591#	9785#	10395#	10601#	11326#	11766#	12618#	13177#	13187#
13442#	13615#	13889#	13949#	13975#	13976#	13977#						
1481#	1482#	1483#	1484#	1485#	1486#	1487#	1488#	1489#	1490#	1491#	1492#	1493#
1494#	1495#	1496#	1497#	1498#	1499#	1500#	1501#	1502#	1503#	1504#	1505#	1506#
1507#	1508#	1509#	1510#	1511#	1512#	1513#	1514#	1515#	1516#	1517#	1518#	1519#
1520#	1521#	1522#	1523#	1524#	1525#	1526#	1547#	1565#	1568#	2149#	2158#	2167#
2176#	2185#	2197#	2209#	2221#	2233#	2435#	2452#	2515#	2552#	2624#	2678#	2729#
2750#	2770#	2792#	2812#	2832#	2852#	2872#	2892#	2921#	2942#	2972#	2993#	3021#
3041#	3069#	3089#	3131#	3162#	3168#	3184#	3185	3191#	3209#	3280#	3281	3287#
3303#	3324#	3325	3331#	3345#	3346	3352#	3368#	3369	3375#	3379#	3430#	3459#
3476#	3479#	3509#	3527#	3530#	3557#	3563#	3591#	3608#	3611#	3641#	3659#	3662#
3689#	3695#	3721#	3726#	3763#	3776#	3817#	3836#	3839#	3882#	3903#	3907#	3949#
3955#	3997#	4002#	4043#	4063#	4067#	4109#	4129#	4133#	4175#	4181#	4223#	4228#
4269#	4289#	4293#	4335#	4355#	4359#	4399#	4404#	4453#	4459#	4534#	4558#	4561#
4637#	4661#	4664#	4744#	4749#	4829#	4834#	4971#	4987#	5226#	5242#	5700#	5716#
6252#	6268#	6793#	6796#	7295#	7298#	7456#	7459#	8149#	8166#	8946#	8964#	9215#
9218#	9564#	9571#	9749#	9765#	10363#	10379#	10578#	10587#	11309#	11312#	11744#	11747#
12598#	12601#	13157#	13160#	13433#	13591#	13595#	13822#	13868#	13872#	13901#	13906#	13911#
13920#	13956#	13971#										
1368#	3423#	3442#	3491#	3542#	3574#	3623#	3674#	3706#	3742#	3793#	3857#	3924#

TSTSTM= 177777

3972#	4019#	4085#	4150#	4198#	4244#	4310#	4375#	4423#	4483#	4586#	4691#	4776#
4850#	5000#	5266#	5740#	6288#	6820#	7321#	7485#	8193#	8981#	9237#	9590#	9784#
10394#	10600#	11325#	11765#	12617#	13176#	13186	13441	13614#	13970			
1368#	2150	2159	2168	2177	2186	2194	2198	2206	2210	2218	2222	2230
2234	2242	2265	2274	2284	2292	2302	2311	2321	2329	2397	2403	2417
2422	2427	2433	2436	2441	2447	2453	2460	2466	2471	2487	2497	2502
2507	2513	2516	2523	2529	2534	2547	2553	2556	2572	2580	2585	2590
2595	2598	2603	2608	2619	2625	2628	2640	2649	2654	2660	2665	2668
2673	2679	2740	2745	2751	2760	2765	2771	2782	2787	2793	2802	2807
2813	2822	2827	2833	2842	2847	2853	2862	2867	2873	2882	2887	2893
2911	2916	2922	2931	2937	2943	2962	2967	2973	2982	2988	2994	3011
3016	3022	3030	3036	3042	3059	3064	3070	3078	3084	3090	3111	3116
3121	3126	3132	3142	3147	3152	3157	3163	3192	3221	3226	3231	3235
3241	3245	3251	3257	3276	3280	3288	3304	3317	3324	3332	3353	3376
3431	3446	3454	3460	3463	3471	3477	3480	3495	3504	3510	3513	3522
3528	3531	3548	3552	3558	3564	3578	3586	3592	3595	3603	3609	3612
3627	3636	3642	3645	3654	3660	3663	3680	3684	3690	3696	3712	3716
3722	3727	3748	3758	3764	3777	3797	3812	3818	3821	3831	3837	3840
3861	3877	3883	3887	3898	3904	3908	3930	3944	3950	3956	3978	3992
3998	4003	4023	4038	4044	4048	4058	4064	4068	4089	4104	4110	4114
4124	4130	4134	4156	4170	4176	4182	4204	4218	4224	4229	4248	4264
4270	4274	4284	4290	4294	4314	4330	4336	4340	4350	4356	4360	4381
4394	4400	4405	428	4448	4454	4460	4487	4504	4509	4529	4535	4538
4553	4559	4562	4590	4607	4612	4632	4638	4641	4656	4662	4665	4696
4713	4718	4739	4745	4750	4781	4798	4803	4824	4830	4835	4856	4883
4888	4898	4903	4921	4926	4944	4949	4966	4972	4988	5006	5027	5032
5054	5059	5098	5103	5121	5126	5139	5144	5153	5158	5189	5194	5212
5219	5227	5243	5272	5287	5292	5309	5314	5330	5335	5346	5351	5388
5393	5446	5451	5473	5478	5501	5508	5545	5550	5573	5578	5618	5623
5665	5670	5688	5693	5701	5717	5746	5761	5766	5783	5788	5806	5811
5822	5827	5862	5867	5920	5925	5953	5958	5981	5988	6022	6027	6055
6060	6084	6089	6118	6123	6158	6163	6207	6212	6232	6237	6253	6269
6292	6305	6310	6324	6329	6343	6348	6371	6376	6386	6391	6400	6405
6429	6434	6444	6449	6466	6471	6480	6485	6495	6500	6509	6514	6523
6528	6549	6554	6565	6570	6580	6585	6603	6608	6627	6632	6642	6647
6664	6669	6678	6683	6705	6710	6719	6724	6736	6741	6750	6755	6778
6783	6794	6797	6823	6843	6848	6861	6866	6889	6894	6903	6908	6938
6943	6953	6958	6976	6981	6989	6994	7011	7016	7023	7028	7042	7047
7055	7060	7078	7083	7090	7095	7118	7123	7133	7138	7154	7159	7182
7187	7207	7212	7227	7232	7241	7246	7256	7261	7275	7280	7290	7296
7299	7325	7337	7342	7369	7374	7382	7387	7412	7417	7443	7448	7457
7460	7491	7506	7511	7528	7533	7549	7554	7598	7603	7658	7663	7687
7692	7717	7722	7763	7768	7795	7800	7825	7830	7872	7877	7901	7906
7944	7949	7989	7994	8019	8024	8061	8066	8110	8115	8136	8141	8150
8167	8199	8214	8219	8236	8241	8260	8265	8311	8316	8369	8374	8404
8409	8434	8439	8476	8481	8510	8515	8541	8546	8578	8583	8608	8613
8656	8661	8687	8692	8728	8733	8775	8780	8807	8812	8848	8853	8899
8904	8927	8932	8947	8965	8985	8999	9004	9039	9044	9075	9080	9104
9109	9130	9135	9156	9161	9182	9187	9201	9206	9216	9219	9242	9254
9259	9272	9277	9295	9300	9320	9325	9389	9394	9408	9413	9459	9464
9475	9480	9495	9500	9510	9515	9559	9565	9572	9596	9631	9636	9648
9653	9667	9672	9690	9695	9709	9714	9744	9750	9766	9790	9804	9809
9826	9831	9846	9851	9863	9868	9883	9888	9944	9949	9980	9985	10013
10018	10041	10046	10076	10081	10113	10118	10132	10137	10183	10188	10206	10211
10235	10240	10250	10255	10273	10278	10299	10304	10313	10318	10333	10338	10358
10364	10380	10399	10417	10422	10436	10441	10456	10461	10478	10483	10499	10504

10519	10524	10541	10546	10556	10561	10573	10579	10588	10603	10617	10622	10638	
10643	10656	10661	10673	10678	10708	10713	10721	10726	10737	10742	10752	10757	
10765	10770	10779	10784	10796	10801	10810	10815	10829	10834	10842	10847	10865	
10870	10888	10893	10910	10915	10928	10933	10948	10953	10964	10969	10978	10983	
10999	11004	11017	11022	11031	11036	11045	11050	11063	11068	11078	11083	11098	
11103	11114	11119	11127	11132	11143	11148	11172	11177	11190	11195	11205	11210	
11220	11225	11240	11245	11257	11262	11282	11287	11295	11300	11310	11313	11329	
11341	11346	11360	11365	11374	11379	11398	11403	11413	11418	11431	11436	11445	
11450	11483	11488	11500	11505	11510	11515	11527	11532	11554	11559	11569	11574	
11586	11591	11614	11619	11631	11636	11662	11667	11685	11690	11702	11707	11730	
11735	11745	11748	11768	11781	11786	11799	11804	11845	11850	11860	11865	11896	
11901	11934	11939	11950	11955	11966	11971	11998	12003	12051	12036	12070	12075	
12101	12106	12129	12134	12155	12160	12183	12188	12197	12202	12221	12226	12246	
12251	12260	12265	12284	12289	12301	12306	12330	12335	12357	12362	12392	12397	
12407	12412	12428	12433	12442	12447	12461	12466	12494	12499	12508	12513	12533	
12538	12555	12560	12585	12590	12599	12602	12621	12628	12642	12647	12676	12686	
12699	12705	12715	12720	12729	12735	12751	12757	12764	12777	12782	12792	12797	
12806	12812	12820	12830	12835	12845	12850	12865	12870	12879	12884	12895	12907	
12913	12919	12929	12934	12939	12944	12956	12966	12971	12981	12986	12999	13004	
13009	13014	13022	13032	13038	13046	13051	13061	13066	13083	13089	13103	13112	
13117	13125	13135	13141	13147	13154	13158	13161	13187	13196	13201	13216	13221	
13229	13234	13249	13254	13270	13275	13285	13290	13295	13301	13308	13321	13326	
13331	13341	13346	13354	13359	13367	13372	13387	13392	13407	13412	13428	13434	
13442	13457	13462	13503	13508	13517	13522	13527	13533	13540	13553	13558	13563	
13572	13577	13586	13592	13596	13623	13632	13637	13664	13669	13683	13688	13703	
13708	13727	13732	13748	13753	13770	13775	13804	13809	13817	13823	13869		
TSTSTS= 000001	1368#	3424#	3443#	3492#	3543#	3575#	3624#	3675#	3707#	3743#	3794#	3858#	3925#
	3973#	4020#	4086#	4151#	4199#	4245#	4311#	4376#	4424#	4484#	4587#	4692#	4777#
	4851#	5001#	5267#	5741#	6283#	6821#	7322#	7486#	8194#	8982#	9238#	9591#	9785#
	10395#	10601#	11326#	11766#	12618#	13177#	13615#						
TSSAU = 010022	3364#	3368	3375										
TSSAUT= 010017	3299#	3303											
TSSCLE= 010020	3314#	3324	3331										
TSSDAT= 010106	13977#	13983											
TSSDU = 010021	3341#	3345	3352										
TSSHAR= 010102	13889#	13921											
TSSHW = 010000	1537#	1547											
TSSINI= 010016	3218#	3280	3287										
TSSMSG= 010012	2144#	2149	2153#	2158	2162#	2167	2171#	2176	2180#	2185	2189#	2197	2201#
	2209	2213#	2221	2225#	2233								
TSSPC = 000001	13975#	13985											
TSSPRO= 010015	3202#												
TSSPTA= 010105	13975#	13978	13979#										
TSSRPT= 010014	3180#	3184	3191										
TSSSEG= 010000	2397#	2435#	2441#	2452#	2460#	2515#	2523#	2552#	2556#	2624#	2628#	2678#	2740#
	2750#	2760#	2770#	2782#	2792#	2802#	2812#	2822#	2832#	2842#	2852#	2862#	2872#
	2882#	2892#	2911#	2921#	2931#	2942#	2962#	2972#	2982#	2993#	3011#	3021#	3030#
	3041#	3059#	3069#	3078#	3089#	3111#	3131#	3142#	3162#	3446#	3459#	3463#	3476#
	3495#	3509#	3513#	3527#	3548#	3557#	3578#	3591#	3595#	3608#	3627#	3641#	3645#
	3659#	3680#	3689#	3712#	3721#	3748#	3763#	3797#	3817#	3821#	3836#	3861#	3882#
	3887#	3903#	3930#	3949#	3978#	3997#	4023#	4043#	4048#	4063#	4089#	4109#	4114#
	4129#	4156#	4175#	4204#	4223#	4248#	4269#	4274#	4289#	4314#	4335#	4340#	4355#
	4381#	4399#	4428#	4453#	4487#	4534#	4538#	4558#	4590#	4637#	4641#	4661#	4696#
	4744#	4781#	4829#	4856#	4971#	5006#	5226#	5272#	5700#	5746#	6252#	6292#	6793#
	6823#	7295#	7325#	7456#	7491#	8149#	8199#	8946#	8985#	9215#	9242#	9564#	9596#
	9749#	9790#	10363#	10399#	10578#	10603#	11309#	11329#	11744#	11768#	12598#	12621#	13157#

T7	010746	G	1487	3674#															
T8	011016	G	1488	3706#															
T9	011062	G	1489	3742#															
UAM =	000200	G	1640#																
UNEXIN	002432	G	1894#	12701	12731	12753	12808	12909	13034	13085	13137								
UNITNB	002314	G	1837#	3248*	3254*	3256													
VDALRG	002537	G	1913#	2651	2675	3118	3128	3760	5100	5155	5191	5390	5448	5475	5547				
			5575	5667	5690	5864	5922	5955	6024	6057	6086	6120	6209	6234	6402				
			6446	6482	6525	6551	6605	6644	6666	6707	6738	6780	6905	6955	6978				
			7025	7057	7092	7135	7243	7292	7384	7414	7445	7600	7660	7689	7765				
			7797	7874	7903	7991	8021	8112	8138	8313	8371	8406	8478	8512	8543				
			8580	8658	8689	8777	8809	8901	8929	9077	9106	9132	9158	9184	9203				
			9512	9885	9946	9982	10015	10043	10185	10252	10723	10754	10781	10812	10844				
			10867	10890	10912	10950	10980	11001	11019	11047	11080	11116	11145	11174	11207				
			11242	11259	11284	11415	11447	11485	11502	11512	11556	11616	11664	11732	11847				
			11898	11936	11968	12000	12033	12072	12103	12131	12157	12185	12223	12248	12286				
			12332	12359	12394	12430	12496	12535	12587	13231	13369	13459	13505	13574					
VDALO =	000001	G	1726#	3744	3773	9506	10179	13225											
VDAL1 =	000002	G	1725#	3744	3773	13225													
VDAL10 =	002000	G	1716#	5469	5568	5949	6113	6660	6700	6774	6972	7683	7790	8400	8573				
			9100	9975	10036														
VDAL11 =	004000	G	1715#	5569	5684	6114	6228	6701	6773	10037									
VDAL12 =	010000	G	1714#	7791	7896	8574	8682	9126											
VDAL13 =	020000	G	1713#	7897	8014	8683	8802	9152											
VDAL14 =	040000	G	1712#	8015	8132	8803	8923	9178											
VDAL15 =	100000	G	1711#	5384	5858	5916	6113	7594	8307	8365	8573								
VDAL2 =	000004	G	1724#	2642	3112	3122	3744	3773	11234	11496	13225								
VDAL3 =	000010	G	1723#	10717	10775	10906	10974	11013	11074	11110	11168	11236	11253	11278					
VDAL4 =	000020	G	1722#	11892	11930	11993	12027	12097	12125	12151	12217	12242	12326	12353	12388				
			12424	12490	12529	12581													
VDAL5 =	000040	G	1721#	9940	9976	11409	11479	11658	11726	11929	11994	12216	12280	12489	12528				
VDAL6 =	000100	G	1720#	10246	10717	10775	10906	10974	11013	11041	11168	11236	11253	11278					
VDAL7 =	000200	G	1719#	3744	5065	5148	5399	5440	5856	5914	6519	6545	6731	6732	6899				
			7237	7378	7406	7609	7652	8305	8363	9021	9879	9938	11251	11828	11961				
			11962	13225	13453	13499													
VDAL8 =	000400	G	1718#	6051	8506														
VDAL9 =	001000	G	1717#	5094	5149	5442	5661	5916	6203	6638	6949	7129	7408	7654	8106				
			8365	8895	9071	9940	11277	11479	11658	11726	11929	13499	13741						
XBCLR	007606	G	3050#																
XBCLRH	007620	G	3050	3058#	4868	9616	10172												
XBCLRL	007652	G	3051	3077#	9727	10220													
XCAS	007376	G	2952#	5676	6218	6457	6594	6655	6693	6766	6967	7167	7433	8122	8911				
			9090	9116	9142	9168	9356	9432	9536	9965	11837	11877	12011	12081	12341				
XCASH	007410	G	2952	2961#	5461	5560	5939	6103	7673	7780	7886	8004	8388	8561	8670				
			8790	10028	10901	12113													
XCASL	007442	G	2953	2981#	5518	5634	6002	6174	7734	7842	7960	8077	8454	8624	8744				
			8864	10161	10880	12139													
XPI	007502	G	3002#	5523	5639	5698	6007	6179	6242	7425	7739	7847	7965	8082	8146				
			8459	8629	8749	8869	8937	9193	9991										
XPIH	007514	G	3002	3010#	9341	9426	9530	10095											
XPIL	007546	G	3003	3029#	9362	9438	9542	10165											
XRAS	007272	G	2901#	5083	5181	5431	5534	5653	6071	6193	6419	6538	6928	7003	7069				
			7110	7173	7218	7267	7400	7641	7750	7858	7976	8096	8526	8640	8760				
			8883	9060	9927	10002	11474	11543	11605	11652	11720	11911	11978	12052	12569				
			12741	12857	13073	13494													
XRASH	007304	G	2901	2910#	5901	8350	11008	11161	11270	12168	12314	12376	12474						

XRASL	007336 G	2902	2930#	6037	8491	10857	10989	1.160	11269	12230	12368	12452	12543
XSALWA=	000000	1368#											
XSALS=	000040	1368#											
XSOFFS=	000400	1368#											
XSTRJE=	000020	1368#											
\$PATCH	036456 G	13961#											
.	= 036554	1372#	1870#	2058#	2132#	3185	3281	3325	3346	3369	13935#	13962#	13977 13985

. ABS. 036554 000

ERRORS DETECTED: 0

CVCDCB.OBJ,CVCDCB./CRF:SYM/SOL/NL:TOC=SVC/ML,CVCDCB.P11
RUN-TIME: 63 73 4 SECONDS
RUN-TIME RATIO: 552/140=3.9
CORE USED: 17K (33 PAGES)